



ROBUSPIC

Public Workshop

Implementation of the LGBT Model

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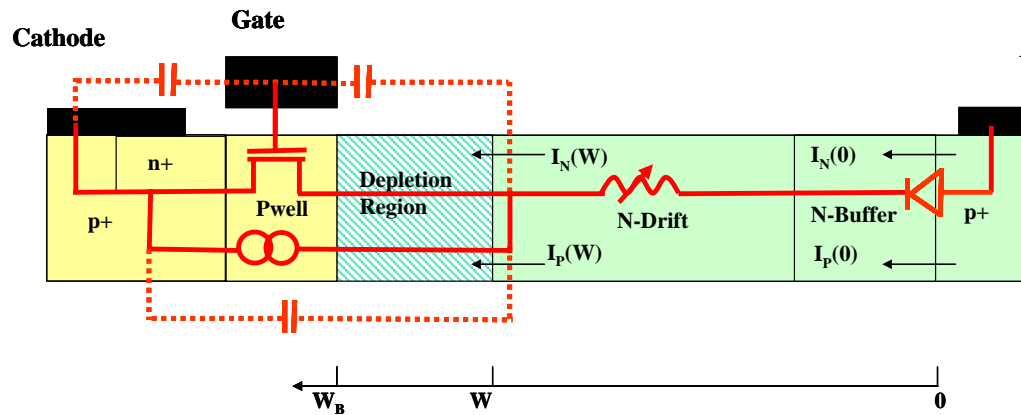
Introduction



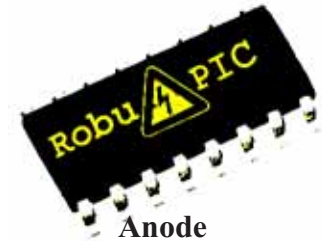
- The LIGBT model
- Verilog-A vs. SPICE
- Steady – State results
- Inductive switching
- Fly back circuit implementation
- Mixed signal simulation
- Electro-thermal simulations
- Conclusion



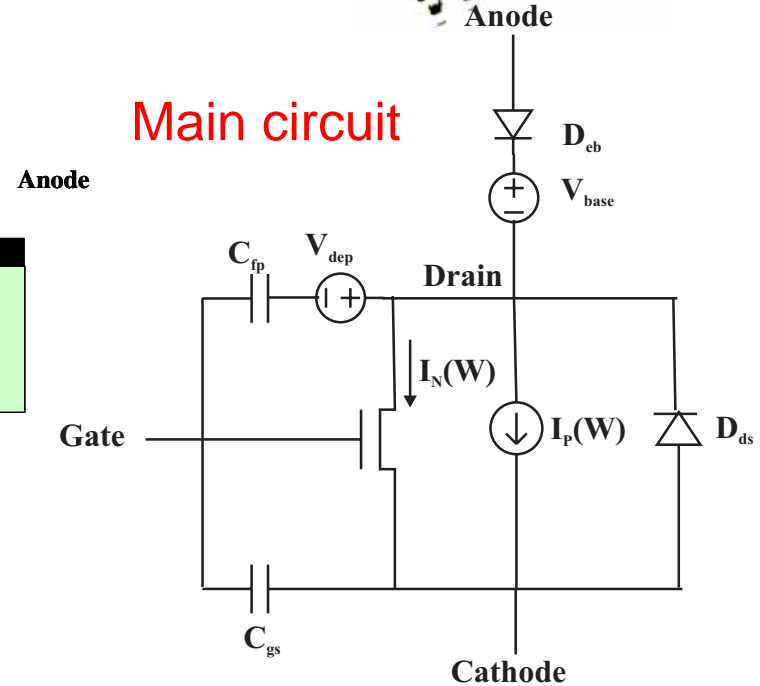
The IGBT model - Electrical



- Compact, physics based and scalable isothermal IGBT model was developed

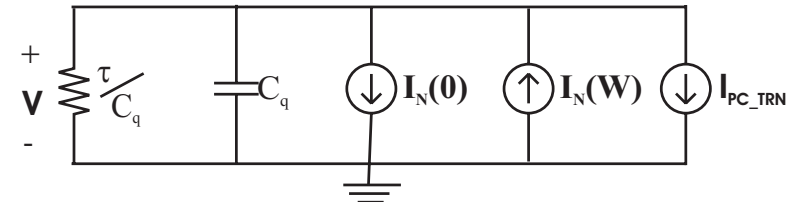


Main circuit



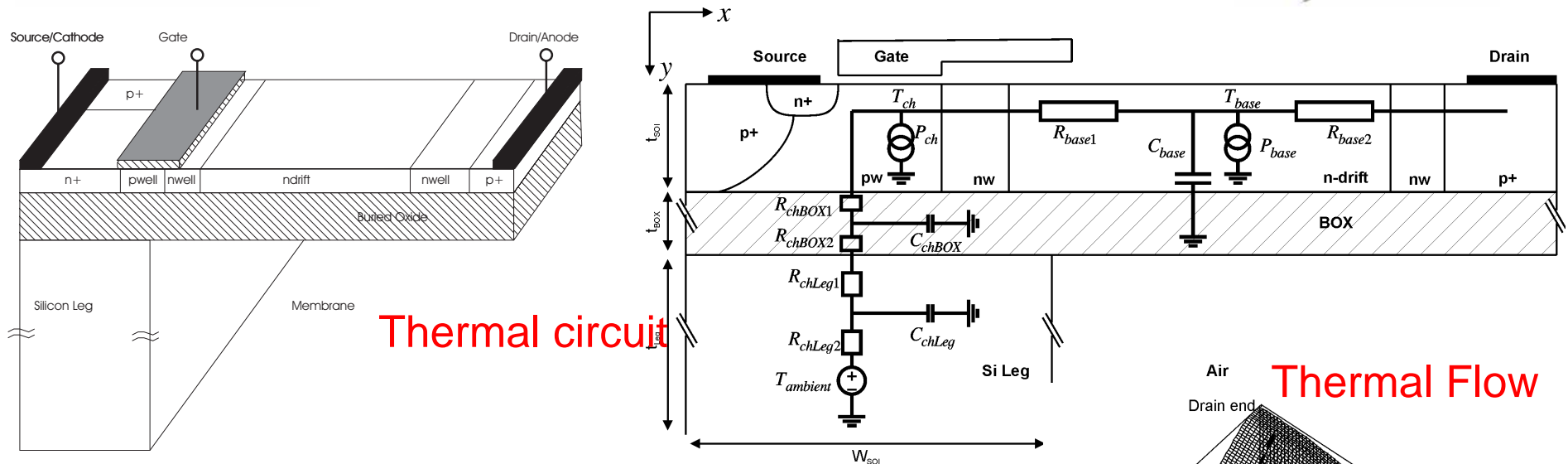
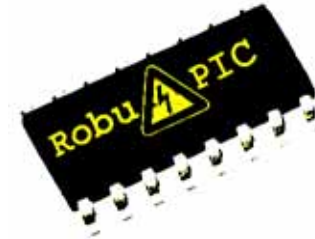
Base charge sub-circuit

$$Q = V * C_q$$





The IGBT model - Electro thermal



Thermal circuit

Thermal Flow

- The electrical model was extended to include thermal effects for Silicon-on-Membrane (SOM) devices
- Resulting in fully coupled electro thermal physics based scalable compact model



Implementation



- Initially implemented in SPICE
- Good matching was obtained for both steady –state and transient cases
- Verified against both simulations and measurements
- Then implemented in Verilog-A

Verilog-A

SPICE

Fully compliant with Cadence EDA tools; mainly IC design users	Manly stand alone circuit simulation; mainly application design users
Choice of optimised simulation engines; e.g. Sepctre, Utrasim	Fixed simulation engine
Versatile, powerful, stable and fast	Relatively slow, convergence issues
Expensive with simulation suits	Relatively low cost



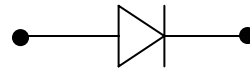


Implementation SPICE vs. Verilog A



- Both in the SPICE and Verilog-A, mathematical equations can be included as current or voltage sources

Verilog-A



SPICE

```
I(ano,cat) <+ Isne *
(exp(Vj / Vth) - 1);
```

Simple diode model

```
GDE ano cat VALUE
{MYDIODE(V(ano,cat))}
```

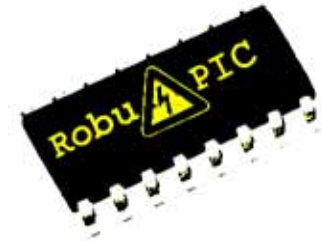
```
.FUNC MYDIODE(Vj)
{Isne*(exp(Vj/Vth)-1)}
```

- Both in the SPICE and Verilog-A, pre defined models can be included as netlists
- In our case SPICE implementation uses more pre-defined circuit level models and Verilog-A uses current/voltage source approach exclusively due to stability and compatibility

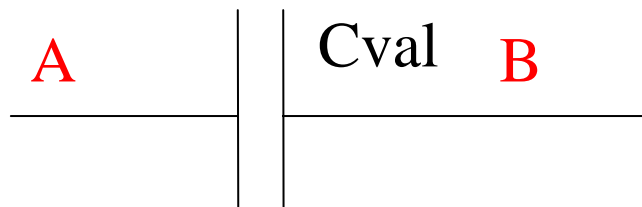




Differentiation in Verilog-A



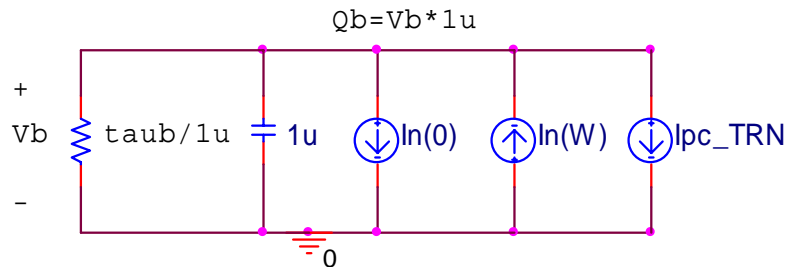
- Differentiation is often used in Verilog-A; especially for capacitors



- Can be implemented as

$$I(A,B) <+ ddt(Cval * V(A,B));$$

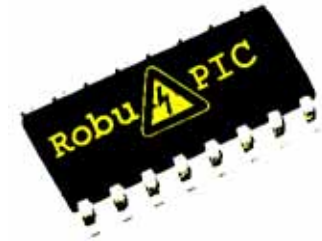
- Model example



$$V(b,grd) <+ Rq*(In(W)-In(0)-Ipc_TRN-`Cq*ddt(V(b,grd)));$$



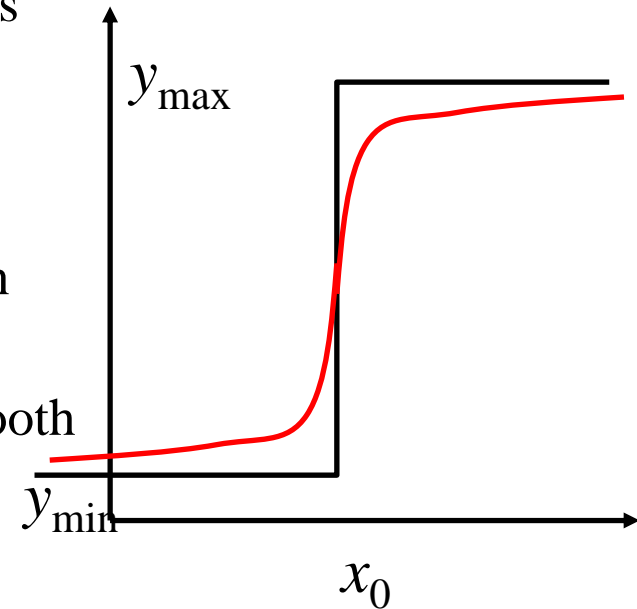
Discontinuity in Verilog-A



- Discontinuities such as `max()` `if.. else..` in Verilog-A can lead to convergence and speed problems
- We have developed a method to overcome this
- Lets assume there is a step in the signal

$$y = y_{min} \{1 - U(x - x_0)\} + y_{max} U(x - x_0)$$

- Since this is a sharp transition the differentiation gives a delta function leading to instability
- Hence approximate the step function with a smooth differentiable function



$$U(x - x_0) \approx \frac{1 + \tanh\{k(x - x_0)\}}{2}$$

- This gives

$$y = y_{min} \frac{1 - \tanh\{k(x - x_0)\}}{2} + y_{max} \frac{1 + \tanh\{k(x - x_0)\}}{2}$$



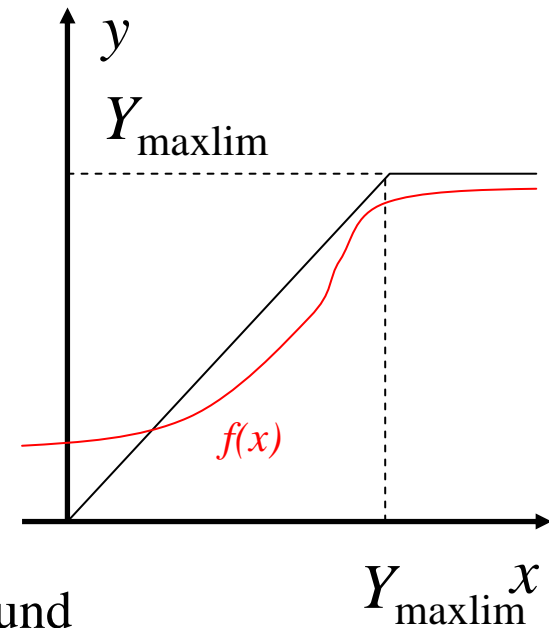
Discontinuity in Verilog-A Cont.



- Upper bound, lower bound and if...else can all be represented by this

$$y = y_{min} \frac{1 - \tanh\{k(x - x_0)\}}{2} + y_{max} \frac{1 + \tanh\{k(x - x_0)\}}{2}$$

$$= appStp(x; x_0, y_{min}, y_{max})$$



$x_0 = Y_{maxlim}, y_{min} = f(x), y_{max} = Y_{maxlim}$ gives upper bound

$x_0 = Y_{minlim}, y_{min} = Y_{minlim}, y_{max} = f(x)$ gives lower bound



Discontinuity in Verilog-A if...else



$$y = y_{min} \frac{1 - \tanh\{k(x - x_0)\}}{2} + y_{max} \frac{1 + \tanh\{k(x - x_0)\}}{2}$$

$$= appStp(x; x_0, y_{min}, y_{max})$$

$$y_1 = appStp(x; x_0 - tol, 0, 1)$$

$$y_2 = appStp(x; x_0 + tol, 1, 0)$$

$$y = y_1 y_2$$

$$z = y(Stmnt_1) + (1 - y)(Stmnt_2)$$

represents

```
cond=(x>x0-tol) && x<x0+tol1);
if (cond==1) Stmnt1;else Stmnt2;
```

$$y_1 = appStp(x; x_0, 0, 1)$$

$$y_2 = appStp(w; w_0, 0, 1)$$

$$y_3 = y_1 + y_2$$

$$y = appStp(y_3; 0.5, 0, 1)$$

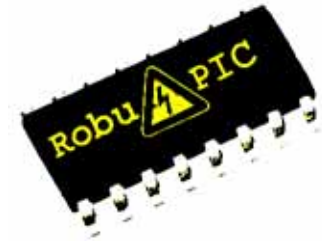
$$z = y(Stmnt_1) + (1 - y)(Stmnt_2)$$

represents

```
cond=((x>x0) || (w>w0)) ;
if (cond==1) Stmnt1;else Stmnt2;
```



Discontinuity in Verilog-A Model Example



The basic MOS equation of the LIGBT

$$\begin{aligned}
 I_{MOS} &= 0 & V_g < V_t \\
 I_{MOS} &= K_p (V_g - V_t - 0.5V_d) V_d & V_g \geq V_t \quad (V_g - V_t) > V_d \\
 I_{MOS} &= 0.5K_p (V_g - V_t)^2 & V_g \geq V_t \quad (V_g - V_t) \leq V_d
 \end{aligned}$$

Implemented in Verilog-A as

```

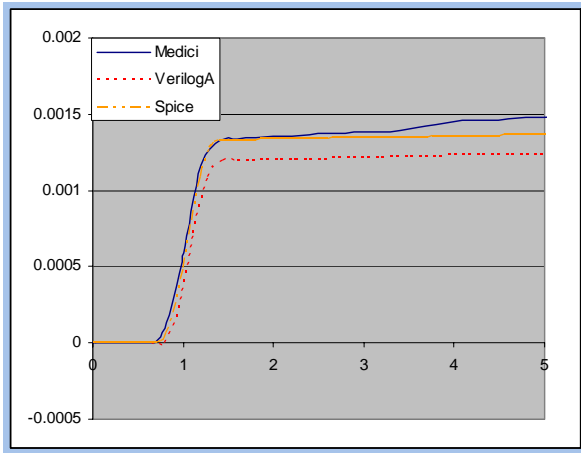
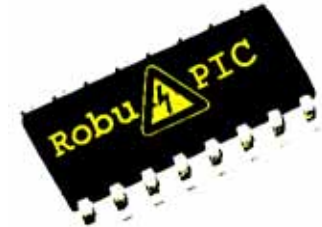
VD=V(D,S);VG=V(G,S);
IMOS_sat=0.5*Kp*pow((VG-Vt),2);
IMOS_lin=Kp*(VG-Vt-0.5*VD)*VD;
VGgtVt_cond=`appStp(VG,Vt,0,1); //assert else IMOS=0
IMOS_lin_sat=`appStp(VG-Vt,VD,IMOS_sat,IMOS_lin);
IMOS= VGgtVt_cond * IMOS_lin_sat; // + (1- VGgtVt_cond)*0
I(D,S) <+ IMOS;

```

e.g. Using appStp function speeded up the flyback simulation 25 times!!



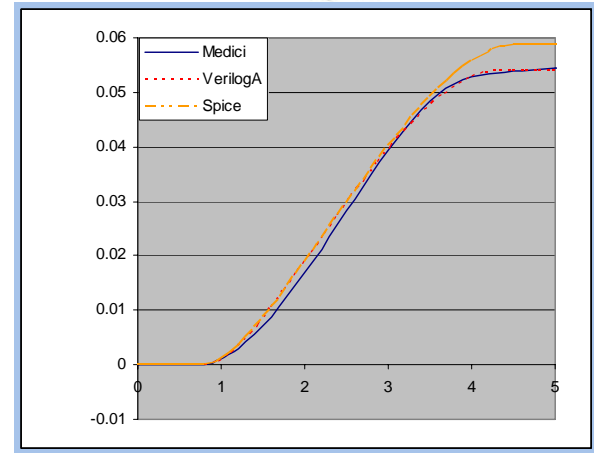
Steady – State Results



$V_G = 2\text{ V}$

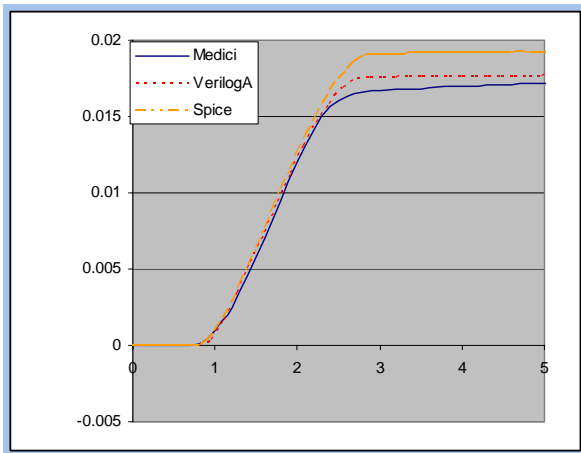
$V_G = 3\text{ V}$

On state curves

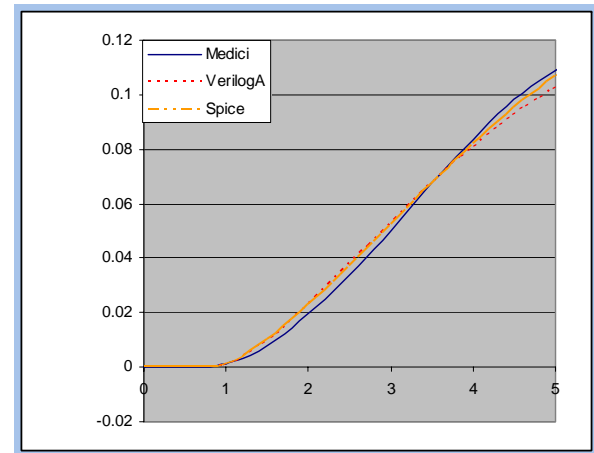


$V_G = 4\text{ V}$

$V_G = 5\text{ V}$

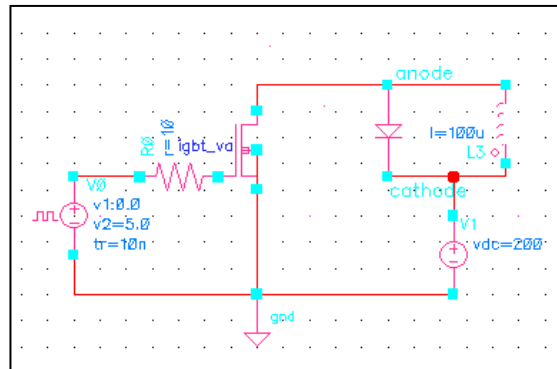


Medici
VerilogA
SPICE

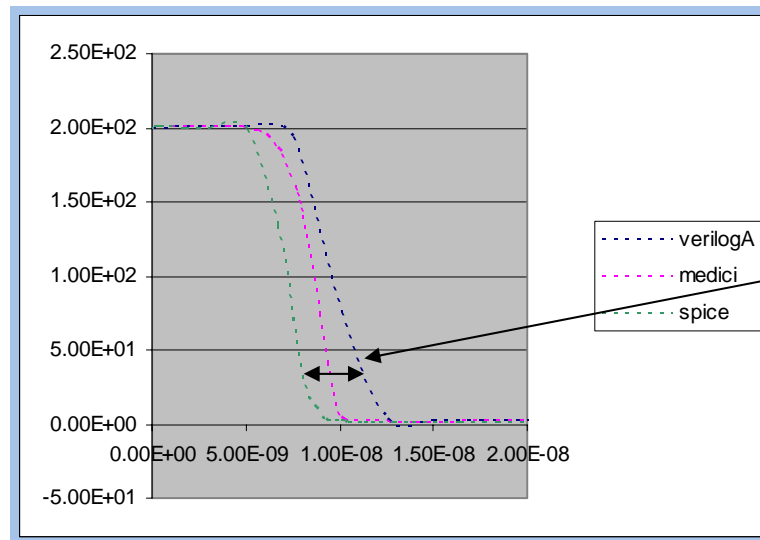




Transient Results – Turn On



Voltage (V)

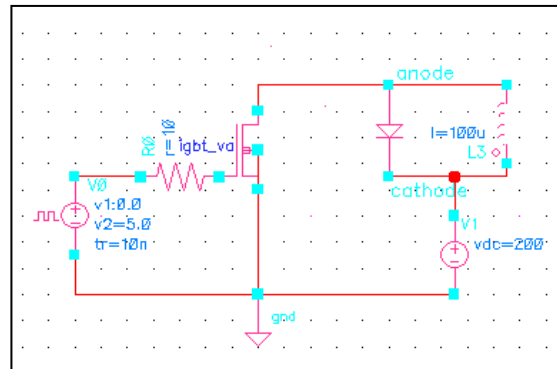


3 ns

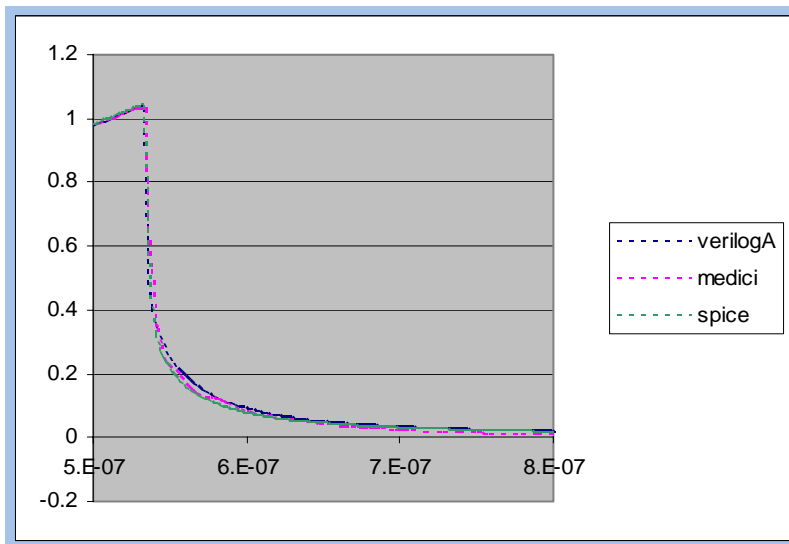
Really small difference



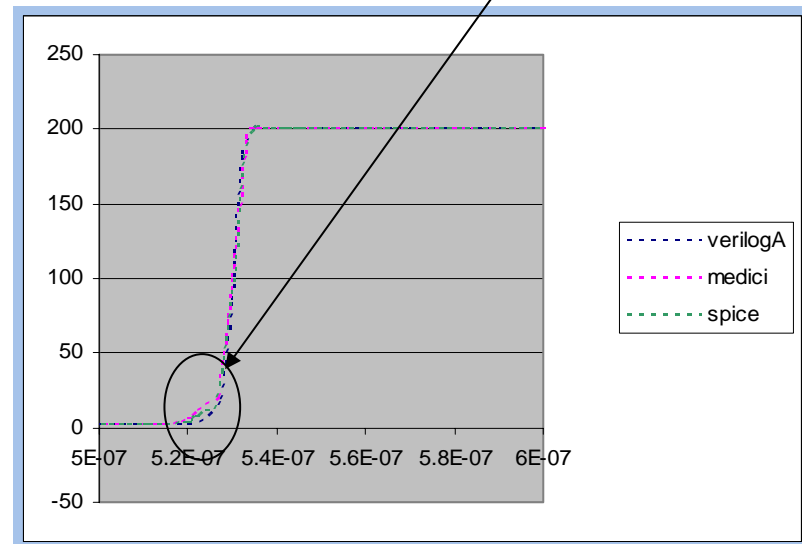
Transient Results – Turn Off



Field plate effect



Current (A)



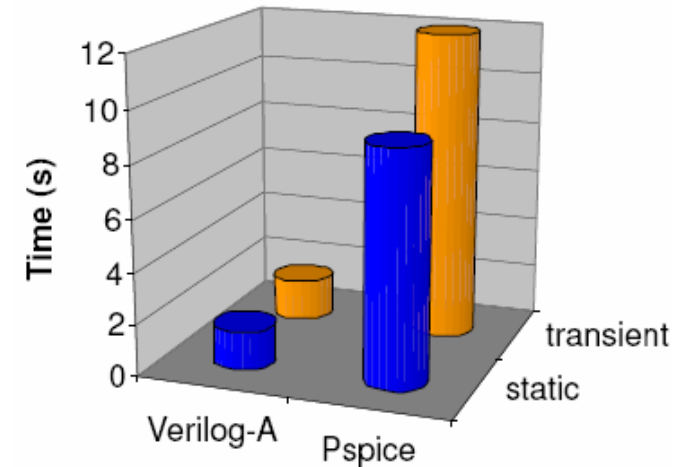
Voltage (V)



LIGBT simulation times



		Static	Transient
SPICE	Variable mobility	26s	32s
	Constant mobility	8s	9.5s
Spectre - VerilogA	Variable mobility (default)	4 gate voltages 1.71s	1.64s



Constant mobility

$$\mu_{nc} = 1400 \quad \mu_{pc} = 450$$

Variable mobility

$$1/\mu_c = [\delta p \ln(1 + \alpha_2 (\delta p)^{-2/3})] / \alpha_2$$

Shirahata mobility model

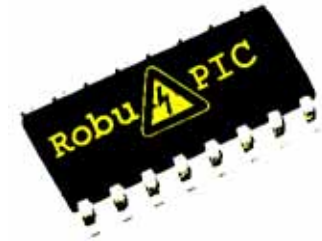
$$1/\mu_{nc} = 1/\mu_n + 1/\mu_c$$

$$1/\mu_{pc} = 1/\mu_p + 1/\mu_c$$



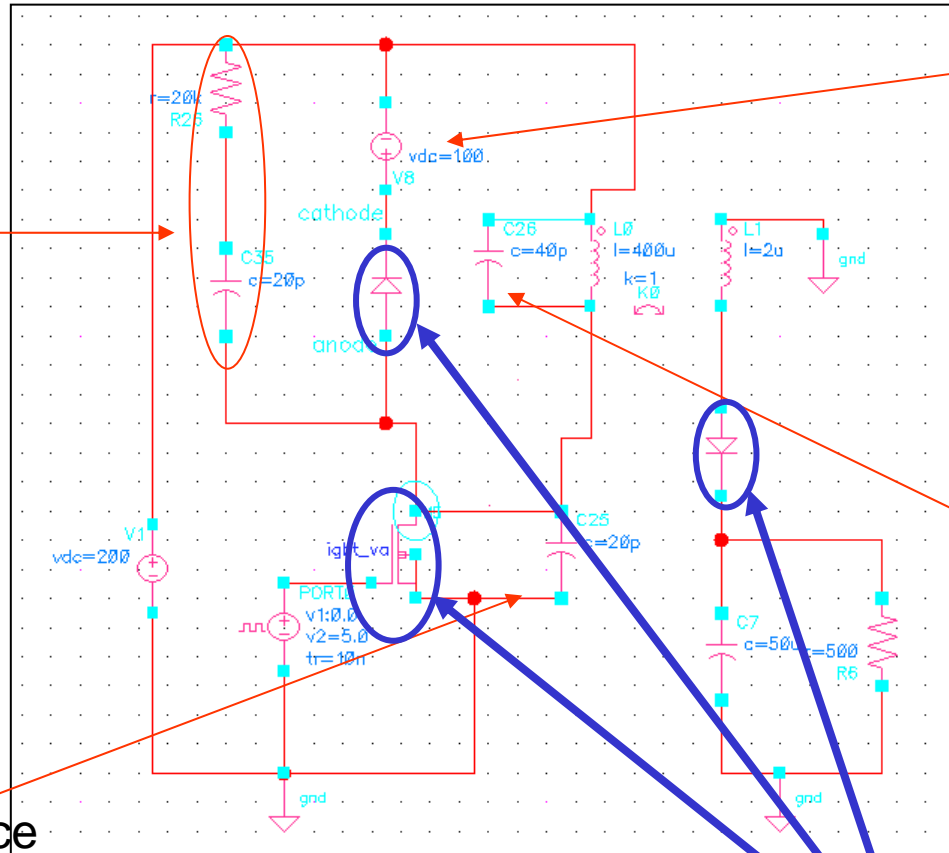


Flyback Circuit



Clamp voltage
Fixed to 300 V

Filter circuit



Leakage capacitance
of the primary
inductor

Leakage capacitance
due to the
Package
(Now include in the model)

Verilog A model

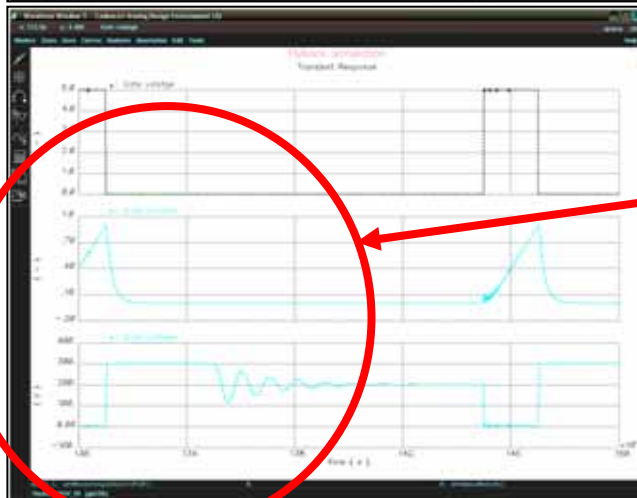
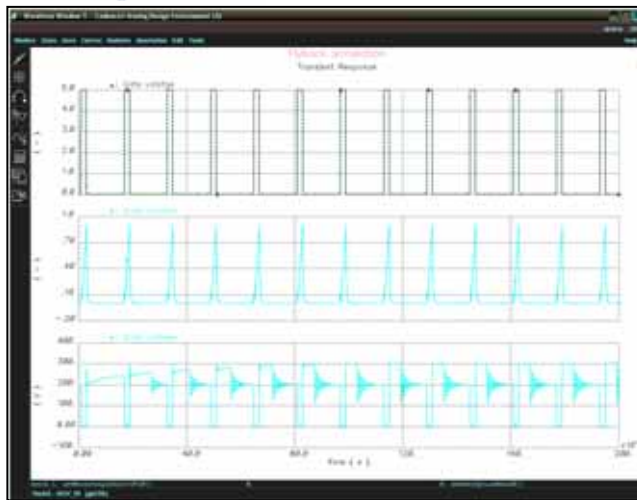




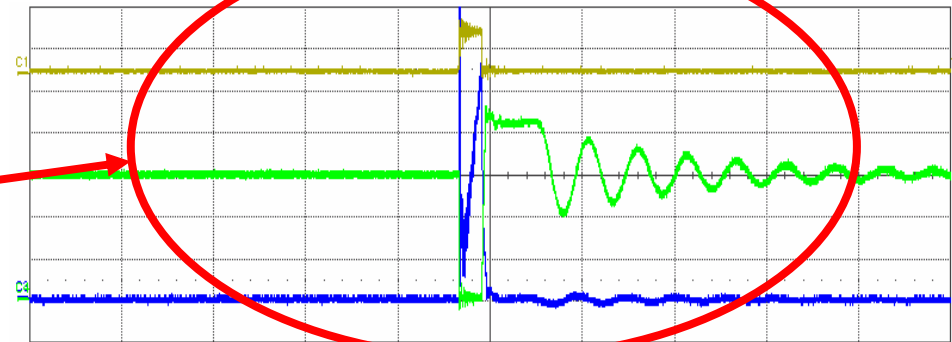
Flyback Simulation



Simulation with a leakage inductance in series with the primary of the transformer



Experimental results



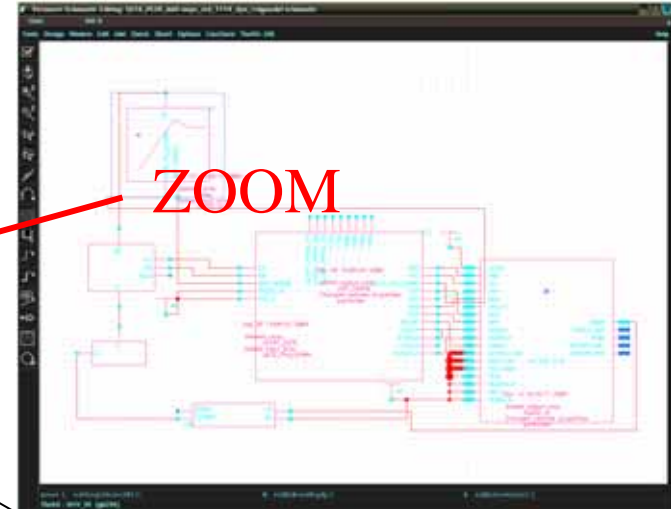
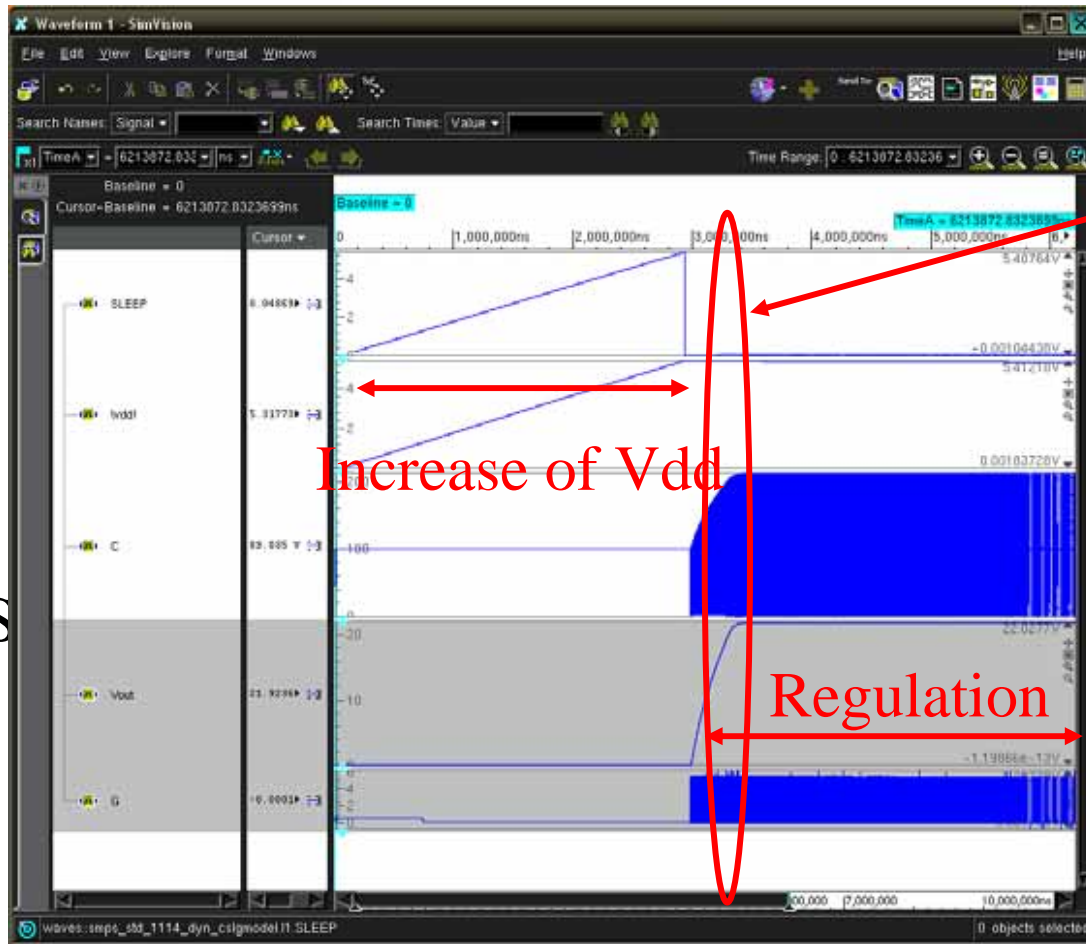
Measure	P1:---	P2:---	P3:---	P4:area(Pwr)	P5:area(Pwr)	P6:---	P7:---	P8:---
value								
status								
C1	5.00 V/div							
	12.00 V offset							
C3		100 mA/div						
		-293.0 mA ofst						
C4			100 V/div					
			-295.0 V offset					
Timebase	-680 ns		Trigger					
	2.00 μ s/div		Auto		1.75 V			
	100 kS		5.0 GS/s		Edge Positive			





Mixed Signal Simulations

Within Cadence AMSUltra Simulator



Increase of Vdd

Regulation

Vdd of the IC

Drain signal of the Power device

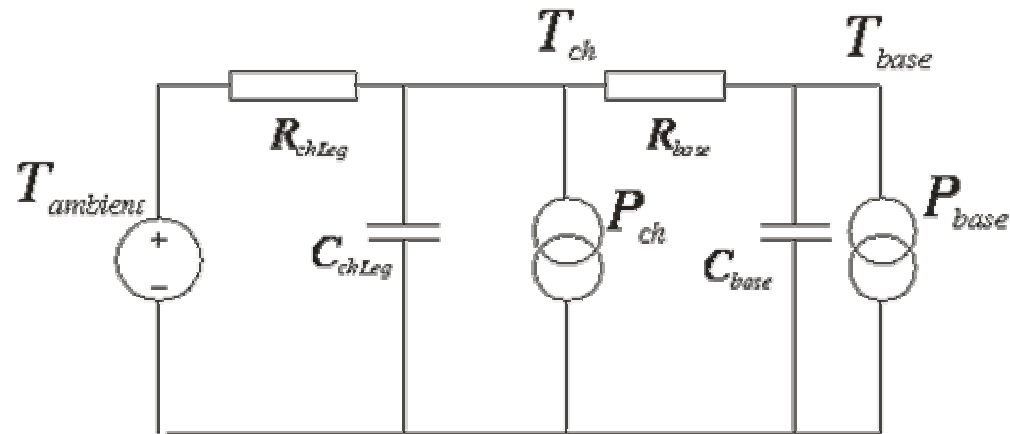
Output voltage

Gate signal of the Power device





Thermal Network



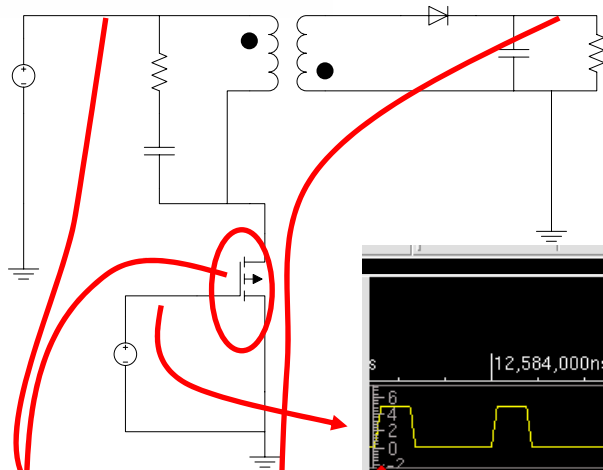
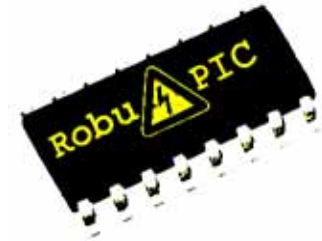
Verilog A implementation

```
Pbase=V(D,drain)*I(d,s);
I(NTbase,grdth)<+ -Pbase;
I(NTbase,grdth)<+ ddt(Cth_base*V(NTbase,grdth));
I(NTbase,NTch)<+ V(NTbase,NTch)/Rth_base;
```

```
Pch=V(drain,S)* I(d,s);
I(NTch,grdth)<+ -Pch;
I(NTch,grdth)<+ ddt(Cth_ch*V(NTch,grdth));
I(NTch,ambient) <+ V(NTch,ambient)/Rth_ch;
V(ambient,grdth)<+ `T0;
```

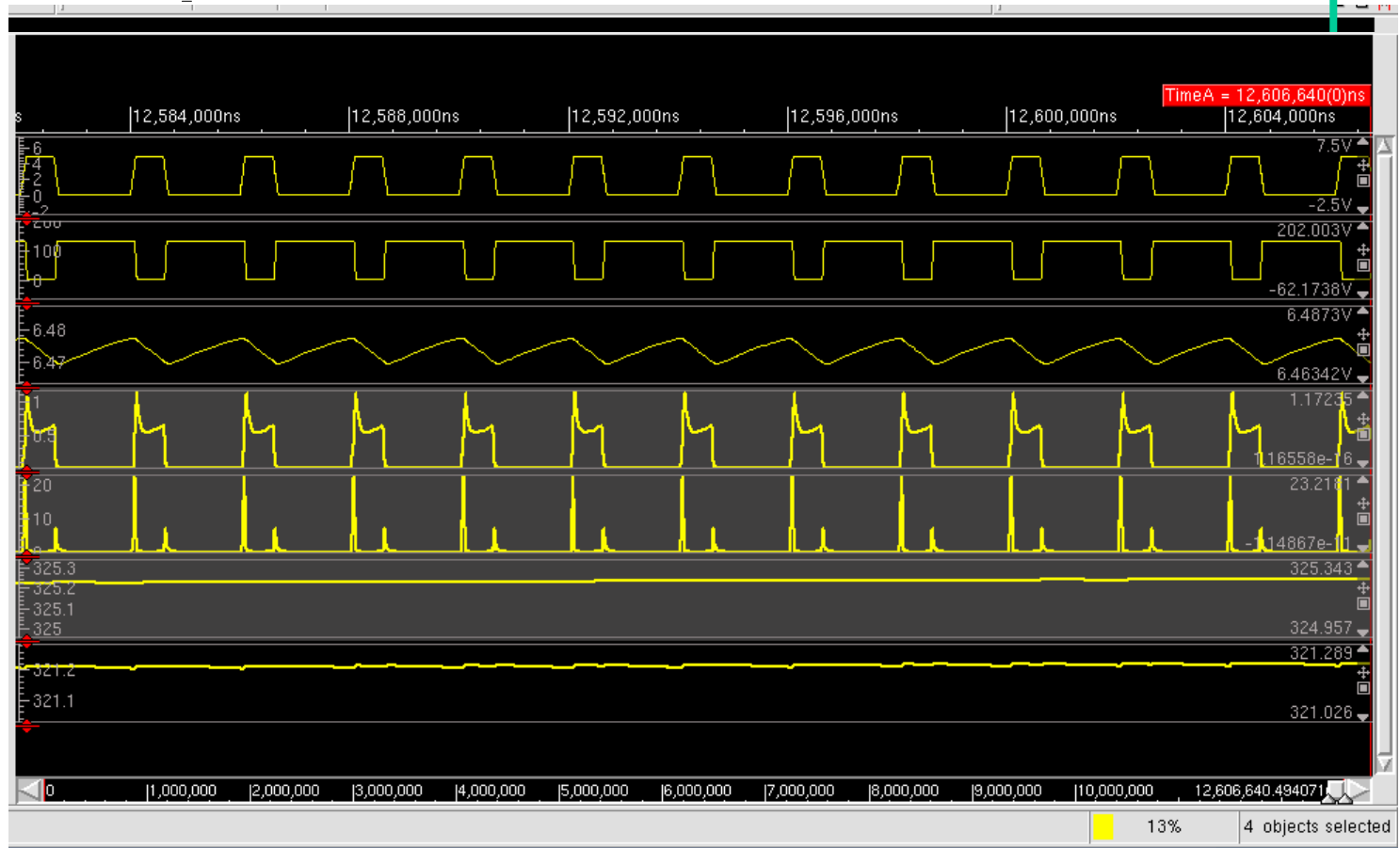


Flyback Self Heating Results



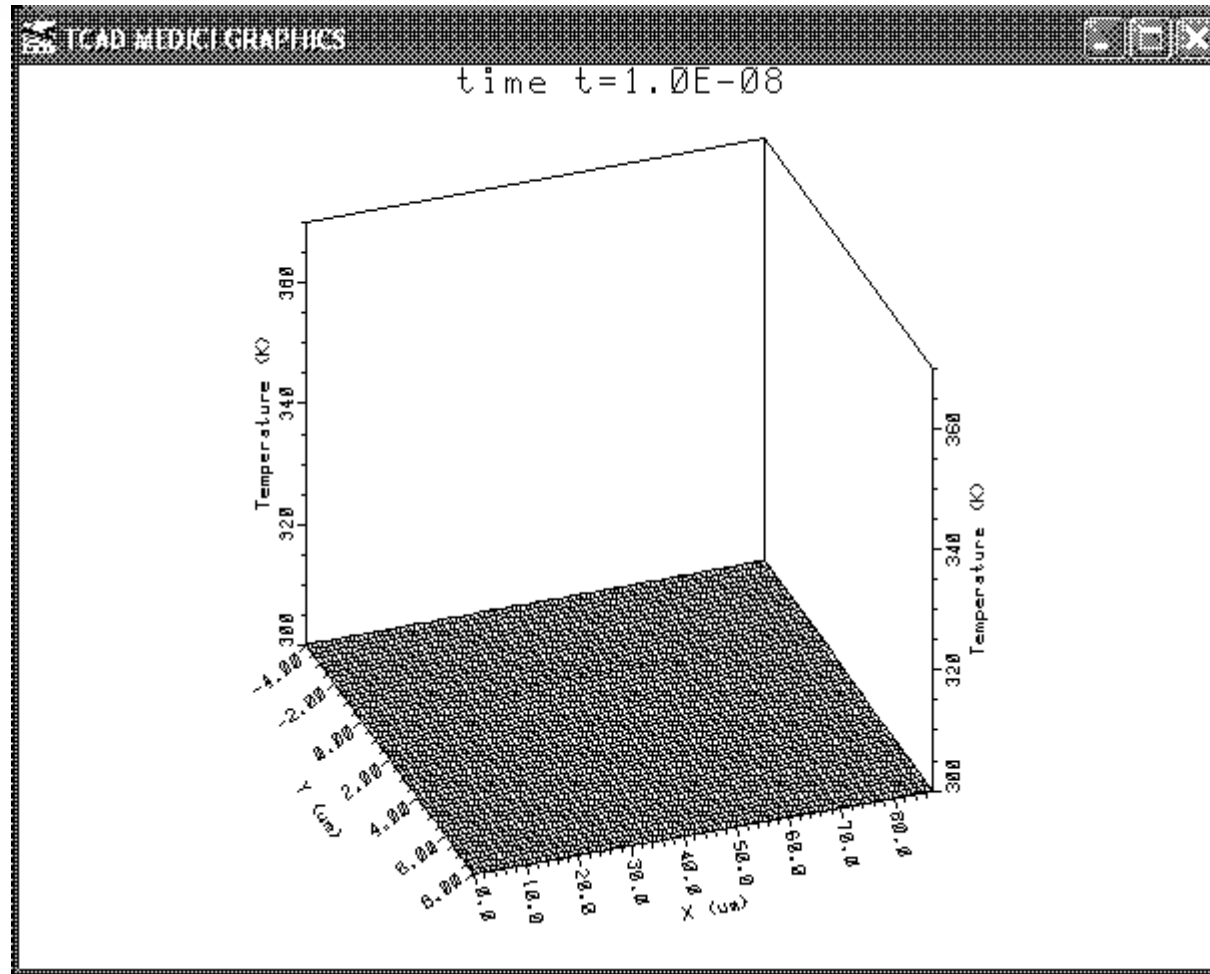
Zoom

Pbase
PChannel
Tbase
Tbase





Flyback Results





Conclusion



- The LIGBT model implemented in SPICE and Verilog-A
- On-state, Flyback, Mixed signal and electro-thermal circuits were simulated
- Verilog-A model improves the speed of the model – up to 30 times in some instances
- Stability has improved dramatically and now long term electro-thermal complex circuit simulations are tractable for the first time
- Fully coupled electro-thermal mixed signal chip simulations results will be presented in future