

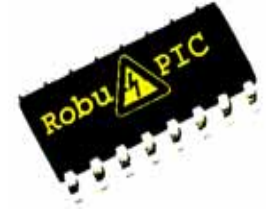
# A Compact Model for Circuit Simulation of High Voltage Lateral & Vertical DMOS Transistors

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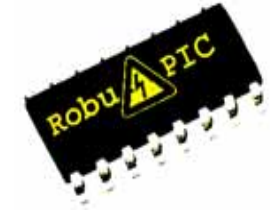
A. Baguenier  
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*University of Gent, Belgium*



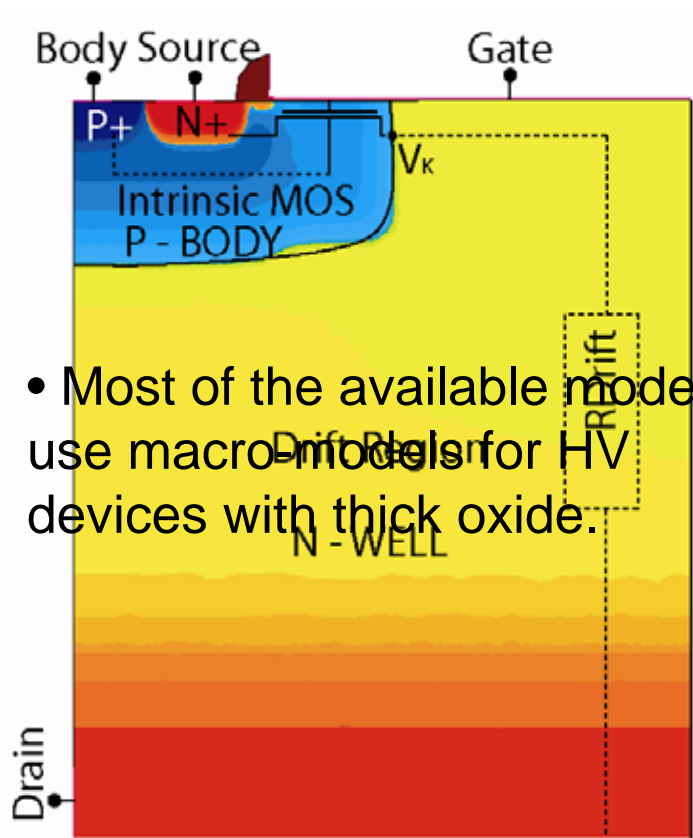
## Outline:

- Device Architectures and Modeling Strategy
  - Core – Low Voltage EKV MOSFET Model
  - Analytical bias dependent drift resistance
  - Strategy for charge evaluation based on  $V_K$
  
- Validation and Results : VDMOS & LDMOS
  - DC and AC operation : comparison with measurement
  
- Conclusion

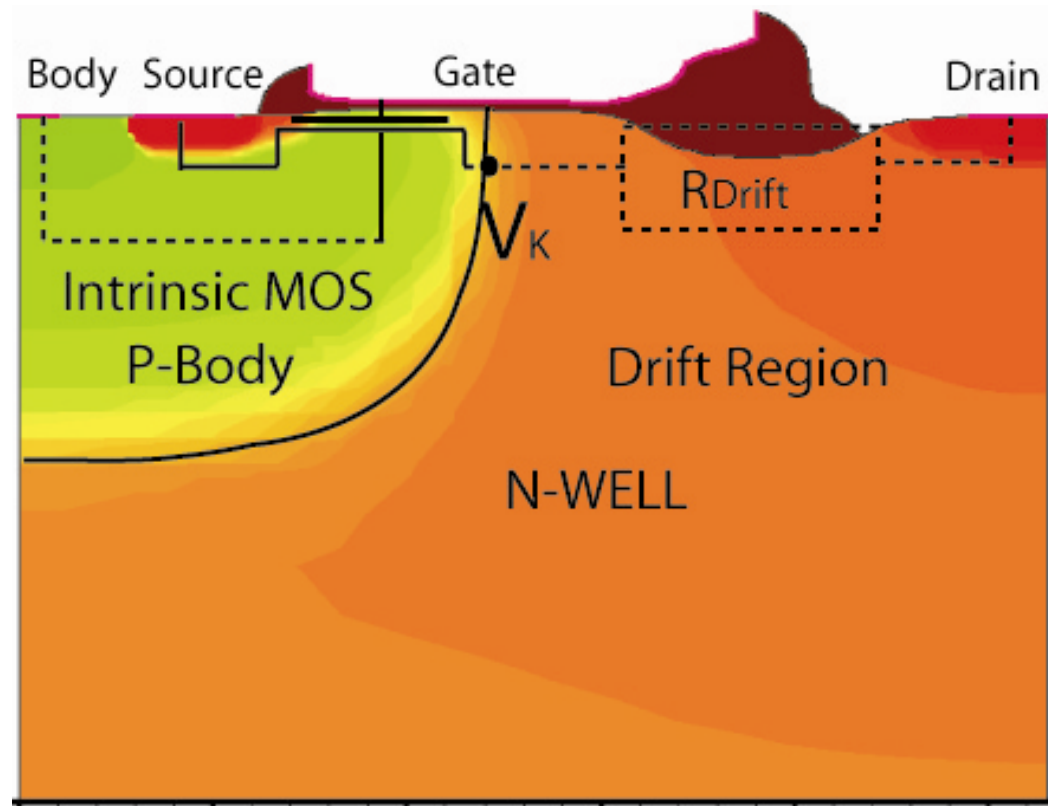


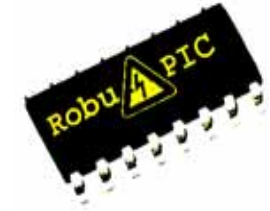
- **VDMOS :**  
 $V_{Dmax}=50V$ ,  $V_{Gmax}=3.3V$

- **LDMOS :**  
 $V_{Dmax}=40V$ ,  $V_{Gmax}=13V$



- Most of the available models use macro-models for HV devices with thick oxide.





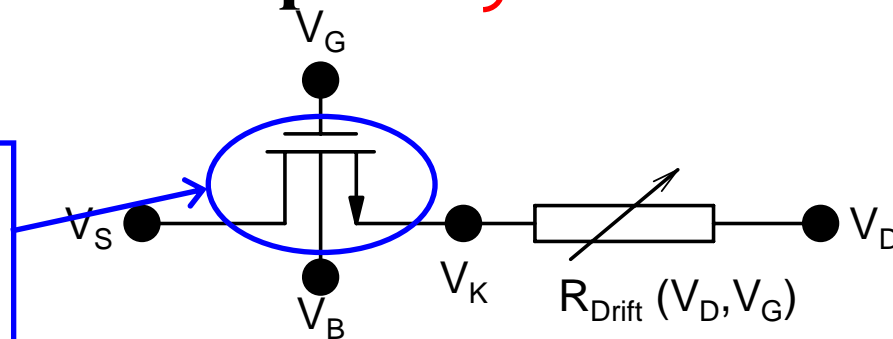
- **Why New model**

- Accuracy
- Compact physical model
- Convergence and speed

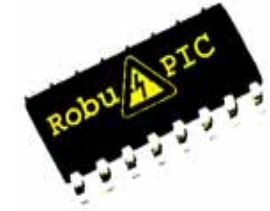
**IC design & simulation**

**EKV MOSFET Model**

**(constant doping)**

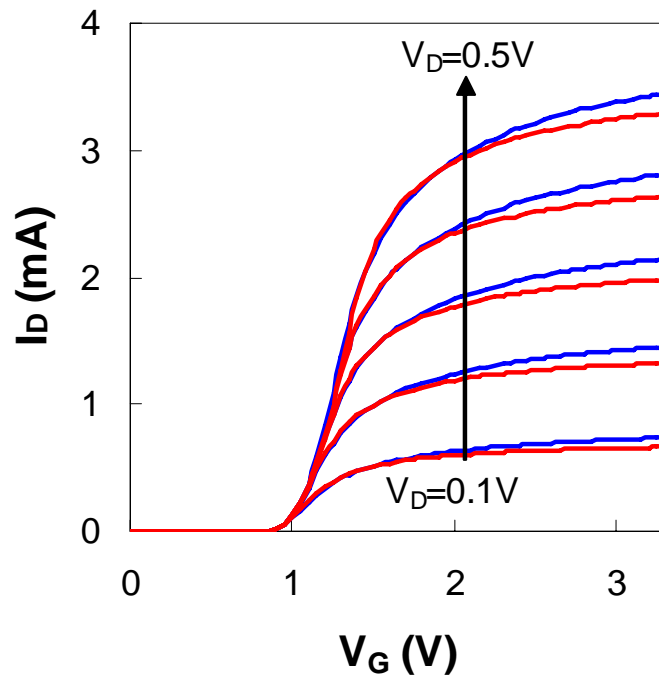


**EKV Model – Less parameters than BSIM**

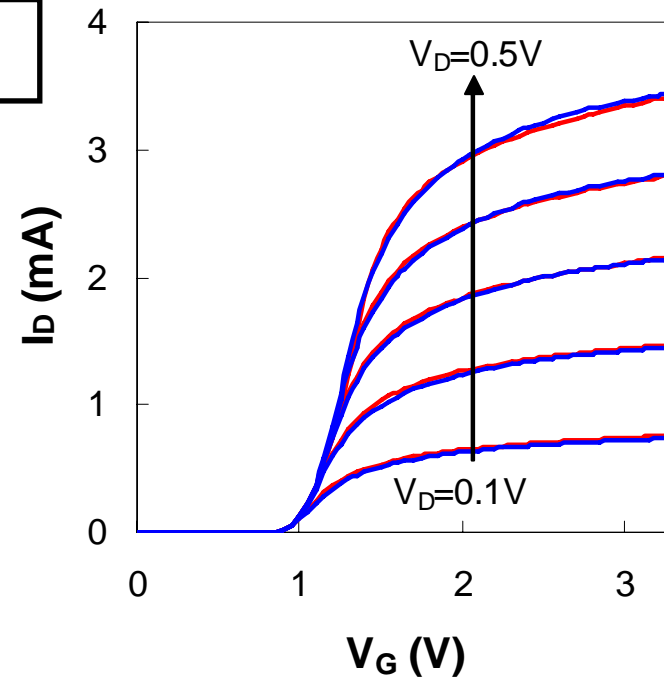


- Drift Resistance expression

**Why not?**  $R_{Drift} = R$



**Low  $V_D$**

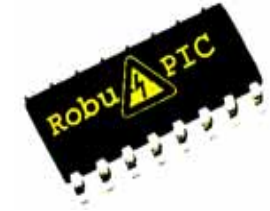


**Accumulation in Drift**

$$R_{Drift} = \frac{R_{Drift0}}{(1 + \theta_{Acc} \cdot V_G)}$$

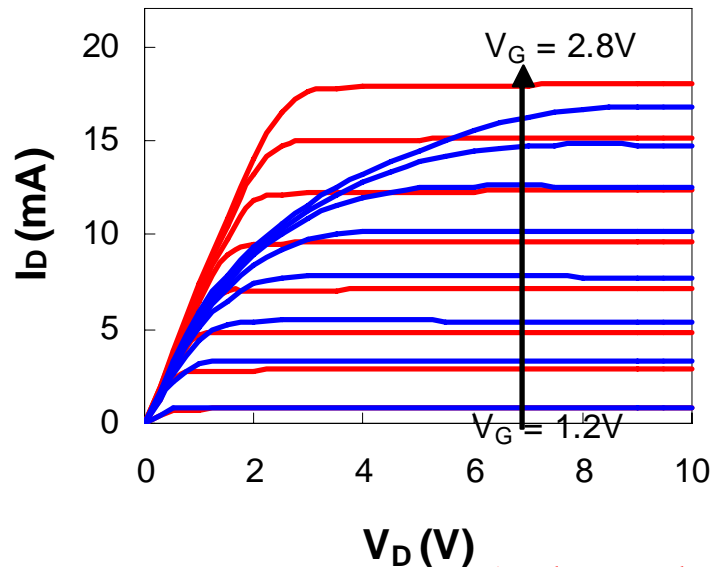
(red - model and blue - measurement)

# Modeling Strategy

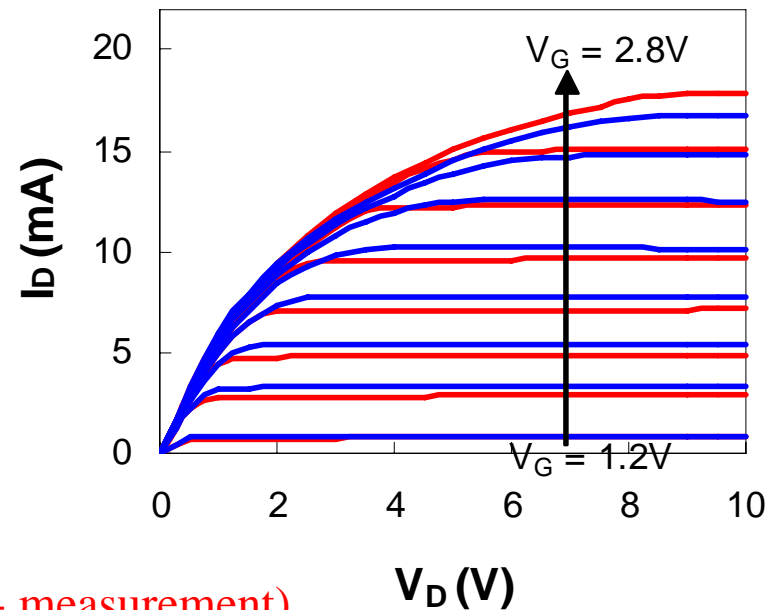


- Drift part only affects the linear region of the output characteristics.
- Delayed transition between linear and saturation regime at high  $V_G$  - **velocity saturation**

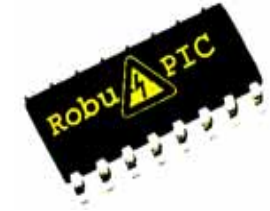
$$R_{Drift} = \frac{R_{Drift0}}{(1 + \theta_{Acc} \cdot V_G)} \quad \boxed{\text{High } V_D \text{ but linear region}} \quad R_{Drift} = R_{Drift0} \frac{\left[ 1 + \frac{(V_D - V_K)}{VSAT} \right]}{1 + \theta_{Acc} \cdot V_G}$$



(red - model and blue - measurement)



# Drift Resistance Expression

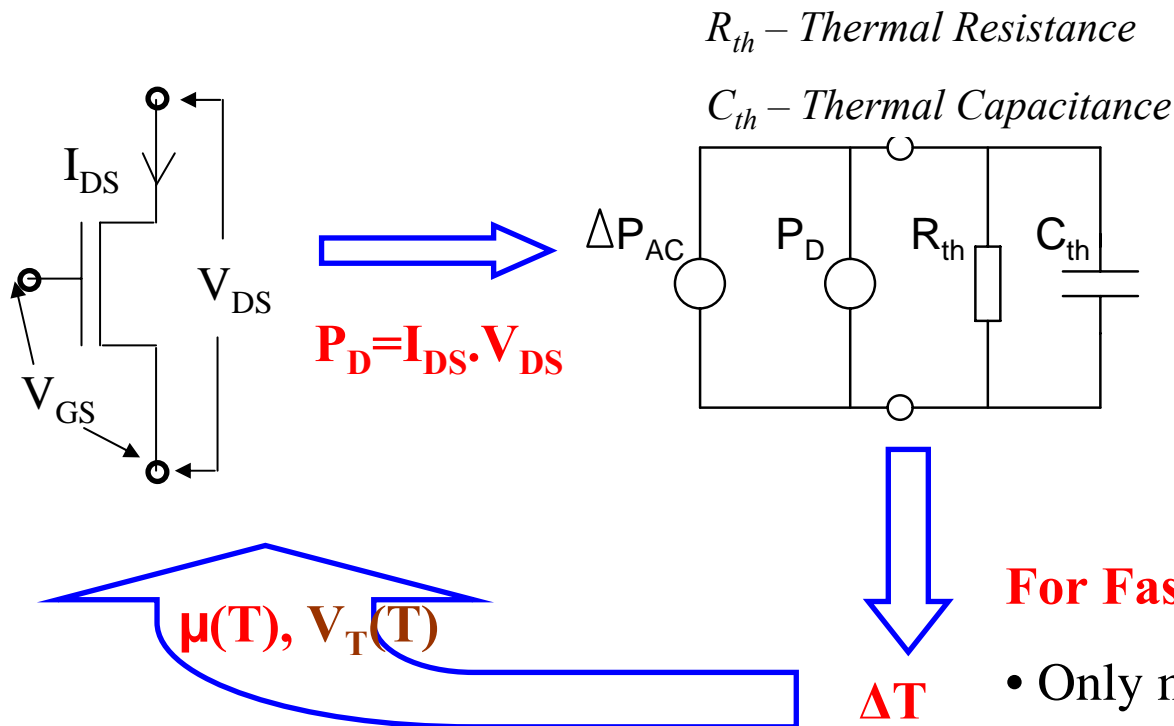
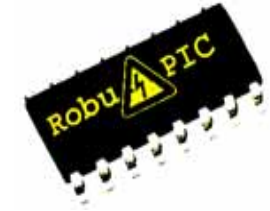


$$R_{Drift} = R_{Drift0} \frac{\left[ 1 + \frac{(V_D - V_K)}{VSAT} \right]}{(1 + \theta_{Acc} V_G)} \left( \frac{L_{DR}}{N(W + \Delta W)} \right) (1 + \alpha_T \cdot \Delta T)$$

Diagram illustrating the components of the Drift Resistance Expression:

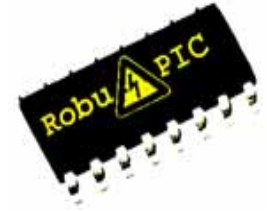
- Drift Length** (blue box) points to  $L_{DR}$ .
- Number of Fingers** (blue box) points to  $N$ .
- Width and Width Offset** (red box) points to  $(W + \Delta W)$ .
- Effect of Temperature** (red box) points to  $(1 + \alpha_T \cdot \Delta T)$ .

# Modeling of Self Heating Effect



## For Fast Convergence

- Only mobility is affected by SHE
- Threshold Voltage can be affected by SHE for better accuracy - Speed decreases



- Charges in MOSFET and Drift region

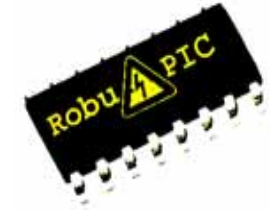
$$Q_G = Q_{EKV} + Q_{Drift} = Q_S + Q_K + Q_B + Q_{Drift}$$

$$Q_{Drift} = (V_G - V_{FB} - \psi_s) \cdot W \cdot L_{DR}^{gate} \cdot C_{ox}$$

Assumptions

- $\psi_s$  varies linearly across accumulation charge sheet

# AC Modeling



## $V_K$ behavior

- As mentioned earlier, Drift does not affect the transistor characteristics in saturation.
- $V_K$  obtained from Spice is valid for linear region. Many models use interpolation function for smooth  $V_K$  from linear to saturation.

Normalized reverse Current

$$i_r = \left[ \ln \left( 1 + e^{\frac{v_p - v_k}{2}} \right) \right]^2$$

Normalized charge density at  $V_K$  (EKV)

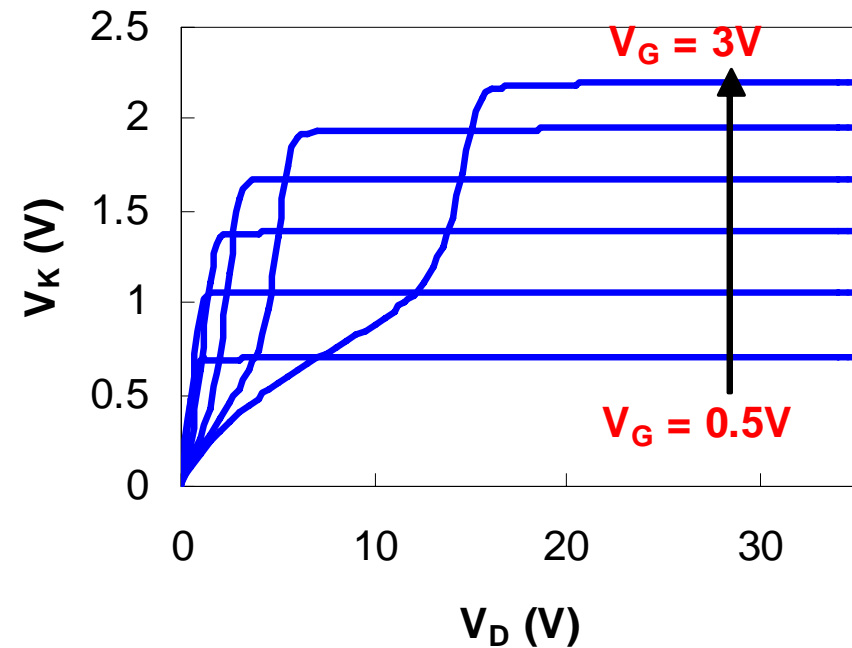
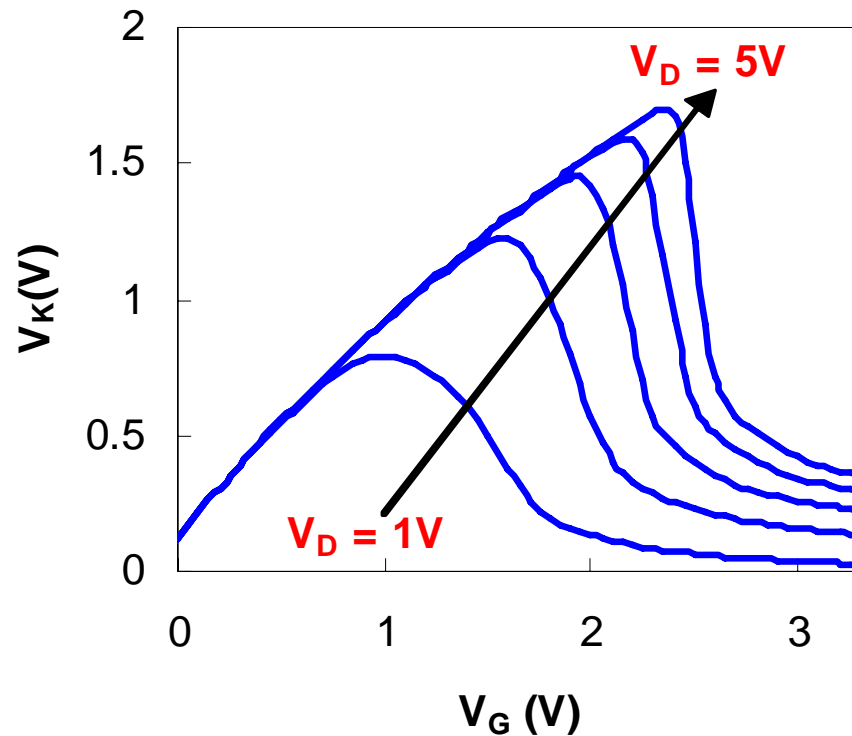
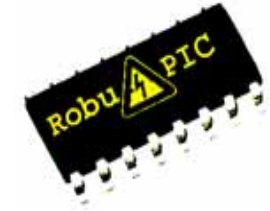
$$q_k = \sqrt{i_r + 0.25} - 0.5$$

Normalized  $v_k$  (EKV)

$$v_k = \frac{V_K}{U_T} = v_p - (2 \cdot q_k + \ln(q_k))$$

Ref: J.-M. Sallese et al., "Inversion charge linearization in MOSFET modeling and rigorous derivation of the EKV compact model", Solid-State Electronics, pp. 677-683, 2003

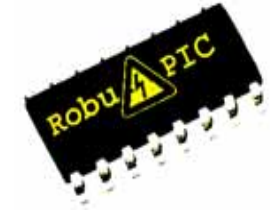
# $V_K$ vs. $V_G$ and $V_D$ for VDMOS



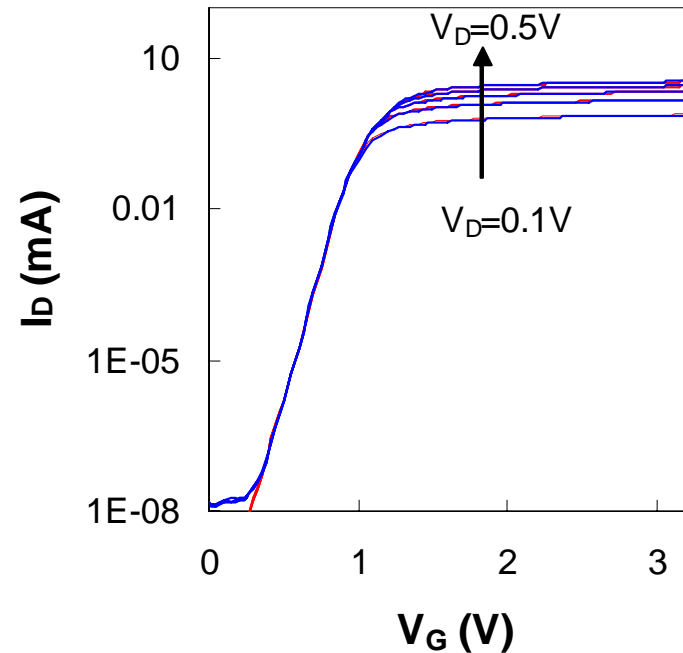
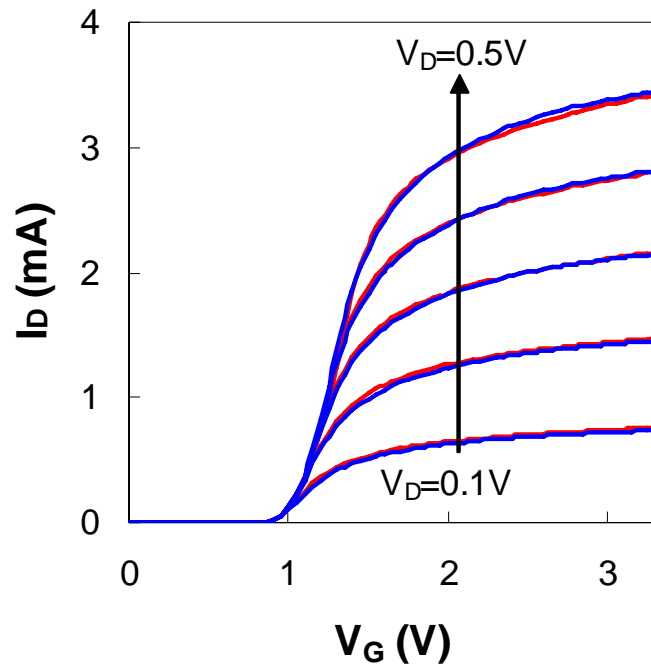
- Trend matches with device simulation and also reported with literature

Ref: C.H. Kreuzer et al., "Physically based description of quasi-saturation region of vertical DMOS power transistors", IEDM, pp. 489 - 492, 1996

# Model Validation on 50V AMIS VDMOS

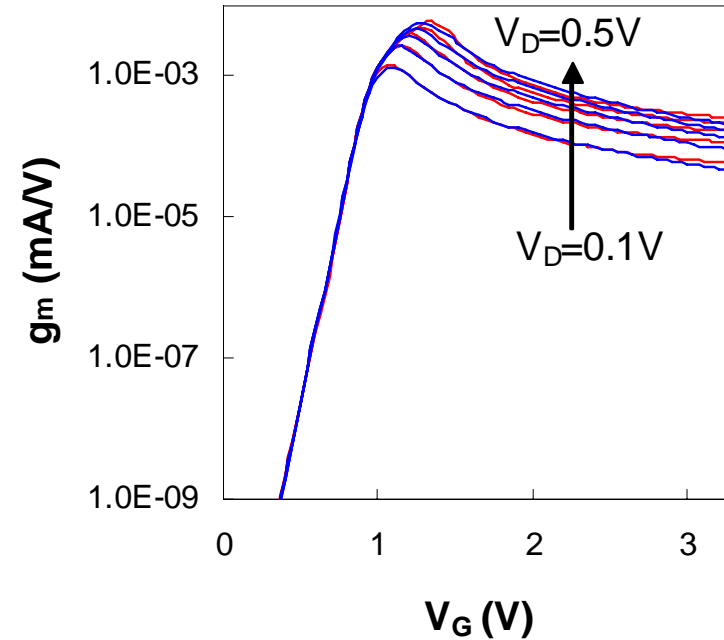
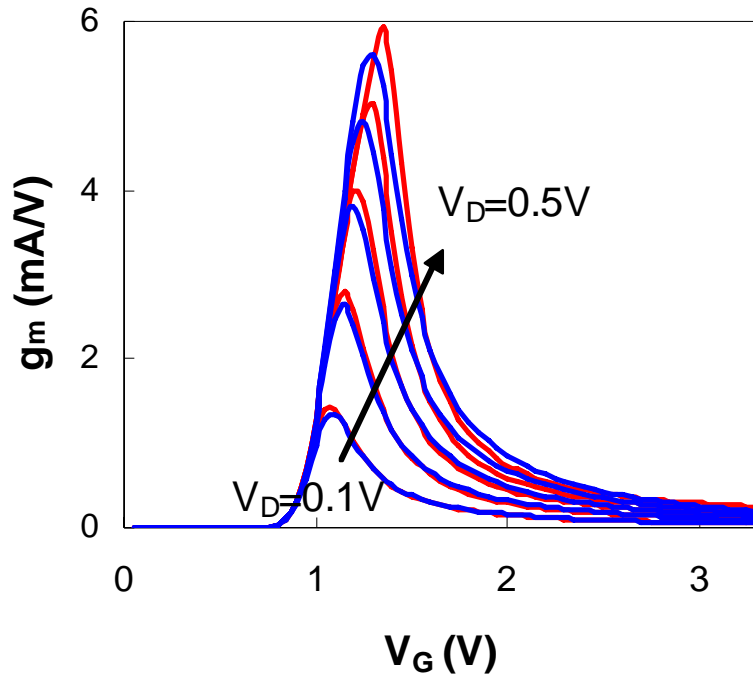


## Transfer Characteristics ( $I_D$ - $V_G$ ): $V_D=0.1$ to $0.5V$



- Subthreshold slope correctly matched
- Good accuracy

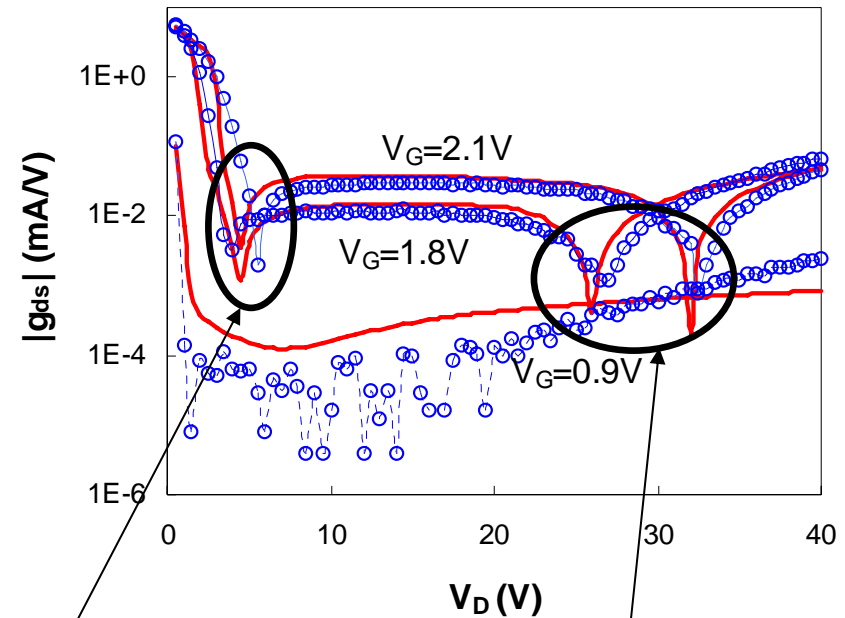
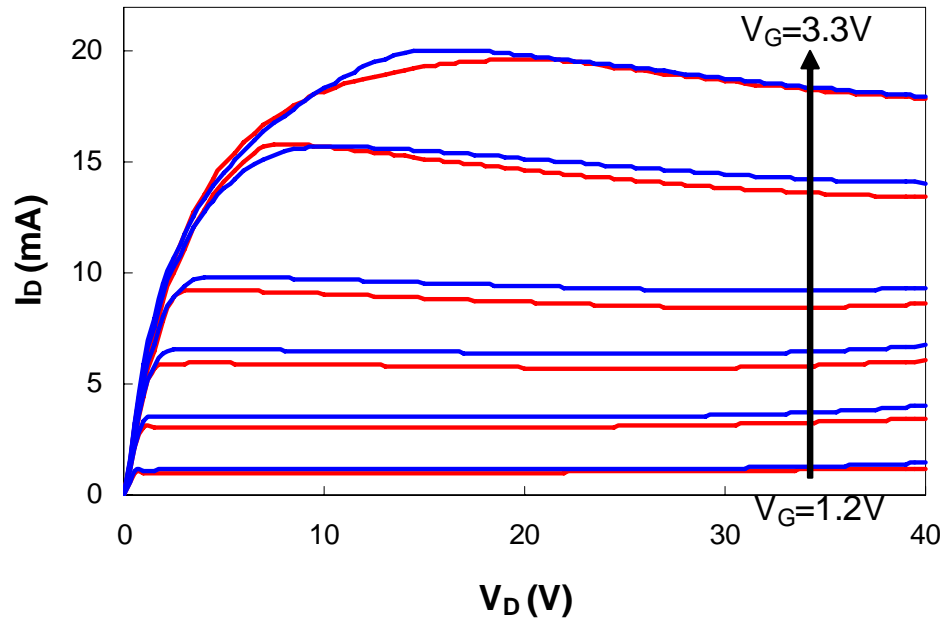
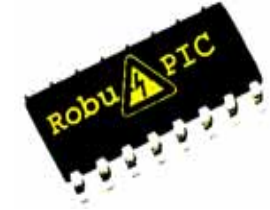
(red - model and blue - measurement)



- Subthreshold slope correctly matched
- descending slope – drift resistance
- peaks – mobility

(red - model and blue - measurement)

# Output Characteristics



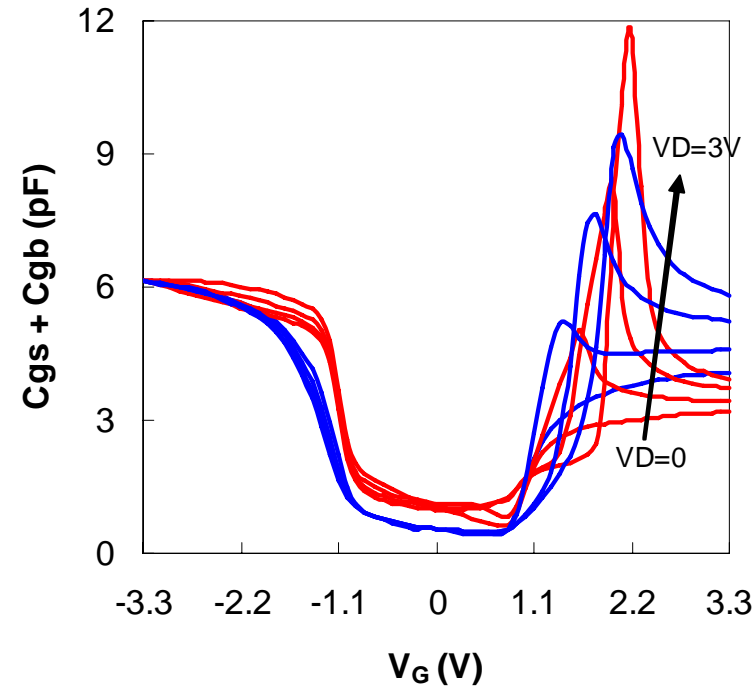
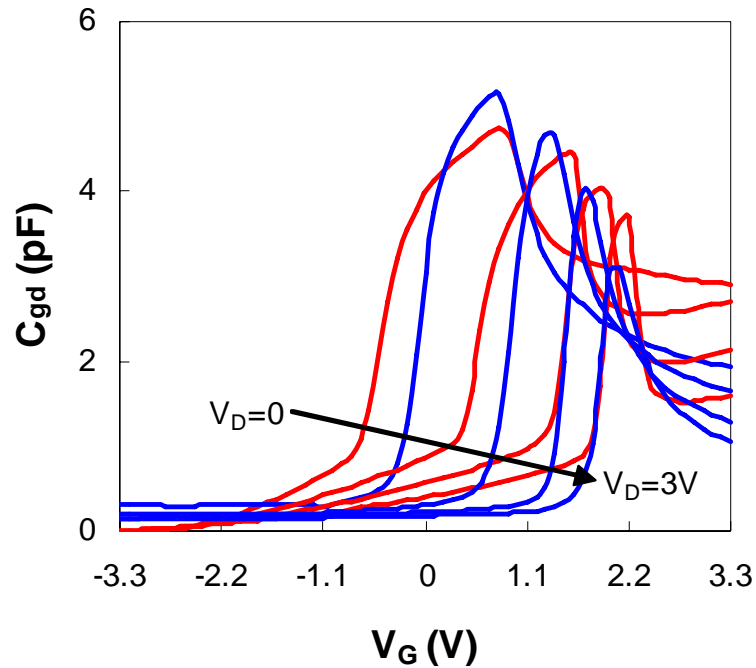
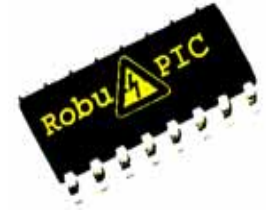
Self-Heating

Impact-Ionization

- Linear region correctly modeled by drift resistance
- Self Heating Effect
- Peaks on  $g_{ds}$

(red - model & blue - measurement)

# $C_{GD}$ and $C_{GS}+C_{GB}$ vs $V_G$ for $V_D=0-5V$



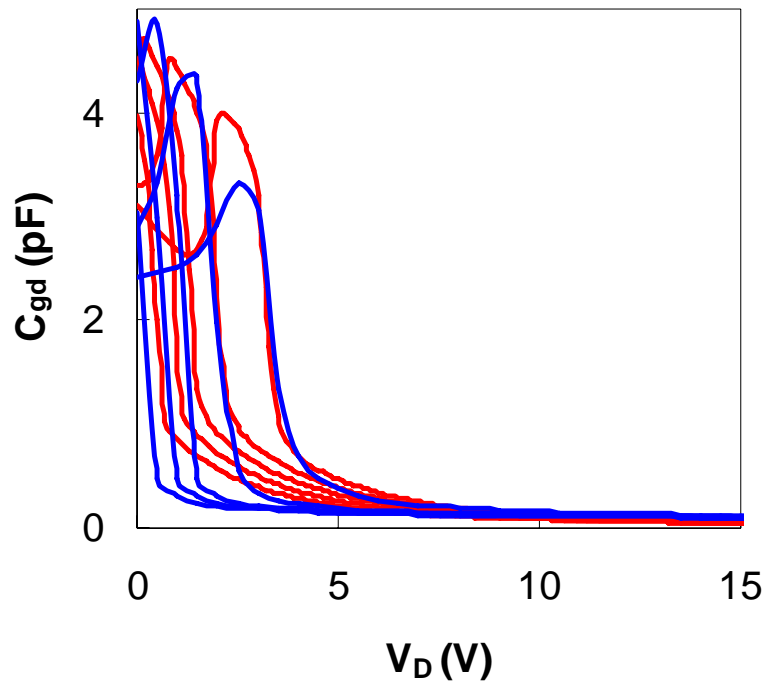
- Position of peaks and amplitude correctly matched @Low  $V_D$

(red - model and blue - measurement)

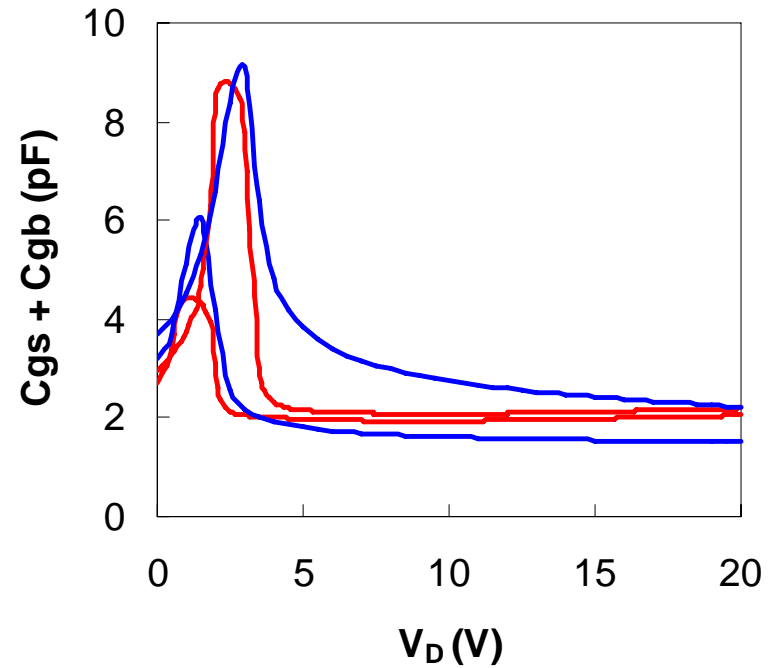
# $C_{GD}$ and $C_{GS}+C_{GB}$ vs $V_D$



$V_G=0-2V$

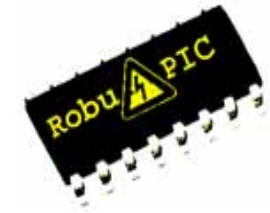


$V_G=1.5 \text{ \& } 2V$

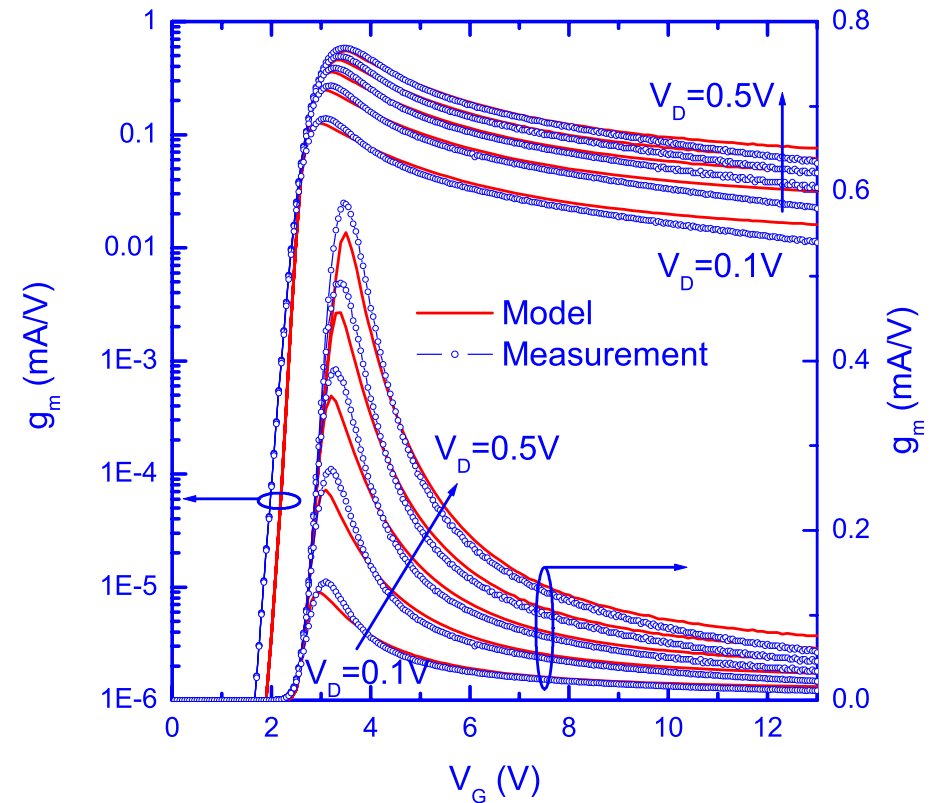
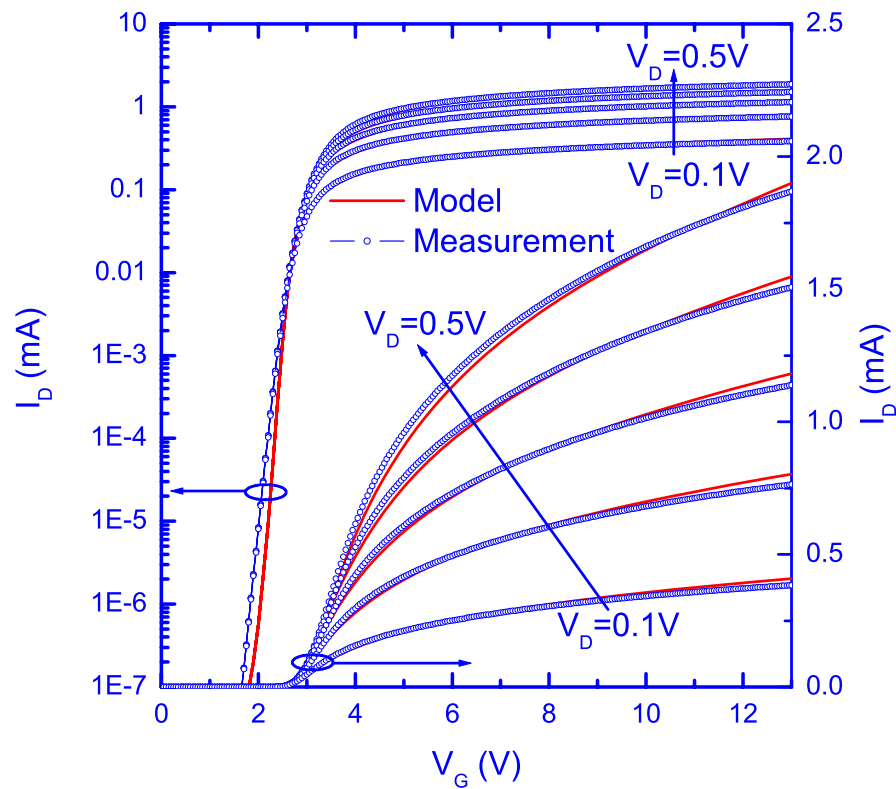


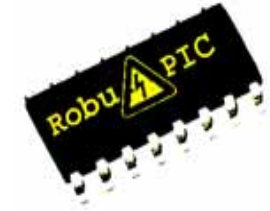
- **Position of peaks correctly matched.**

(red - model and blue - measurement)

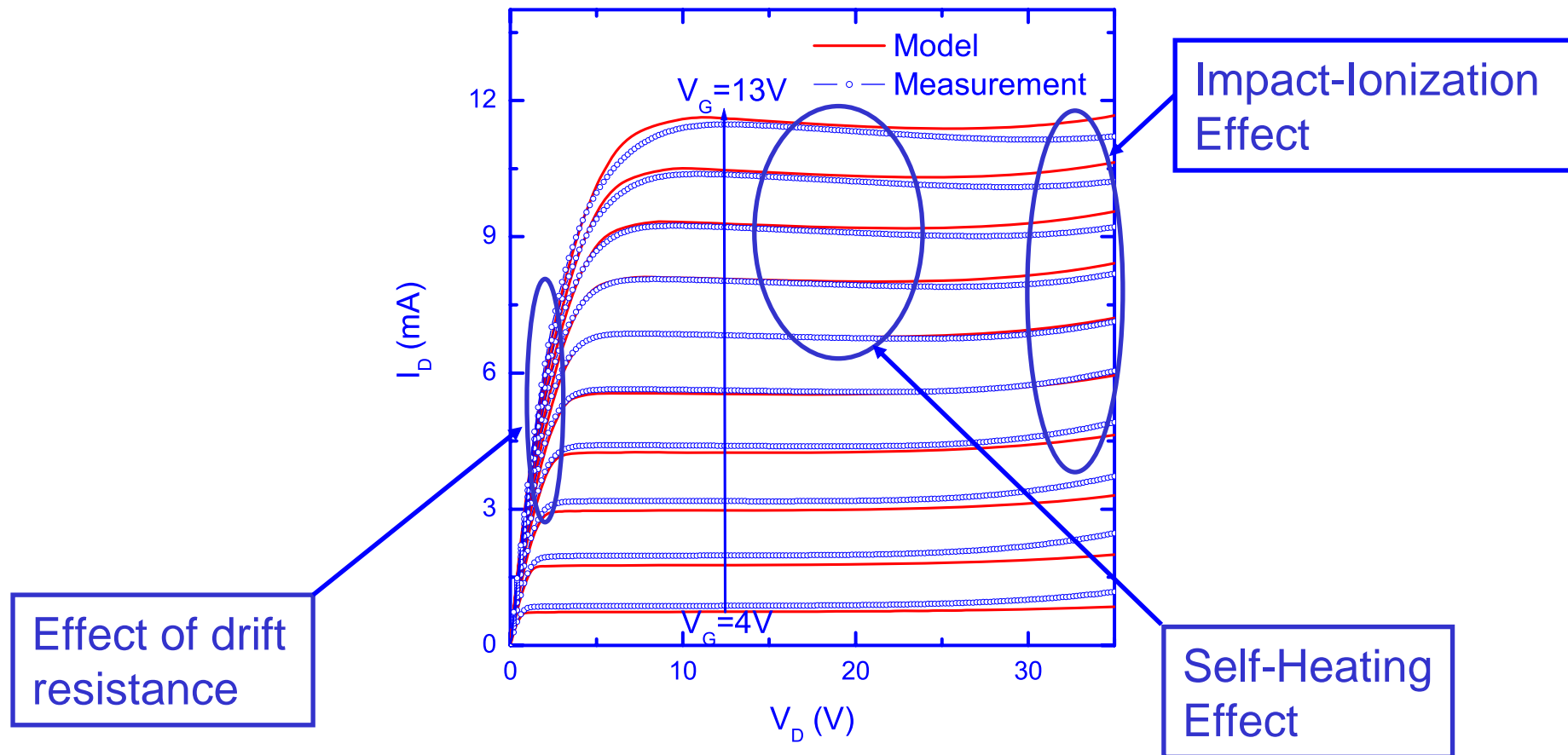


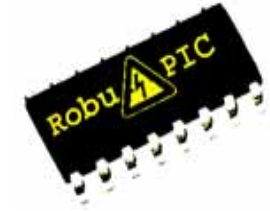
## Transfer Characteristics



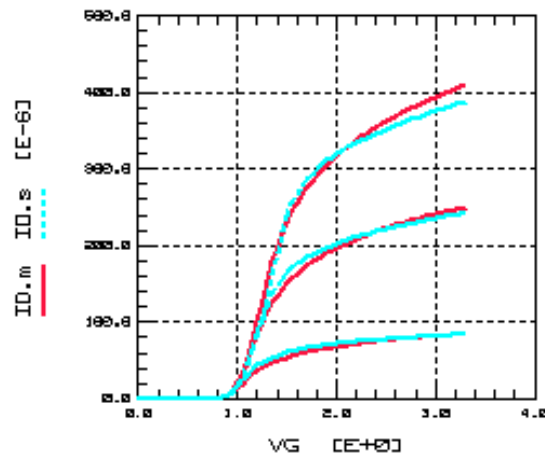


## Output Characteristics

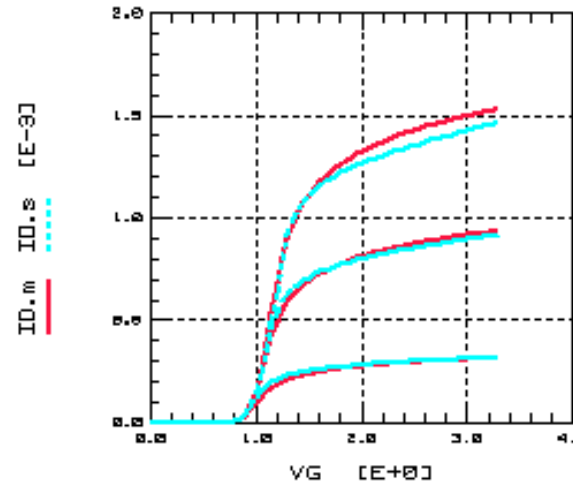




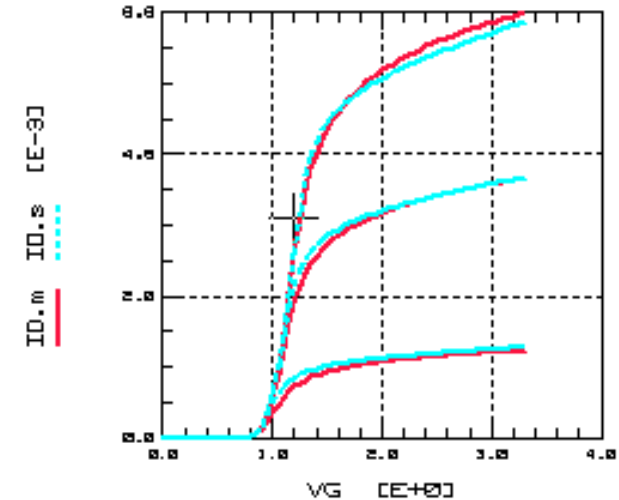
## Transfer Characteristics



(a)



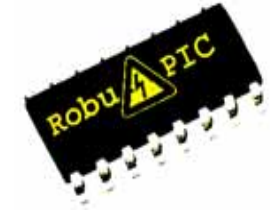
(b)



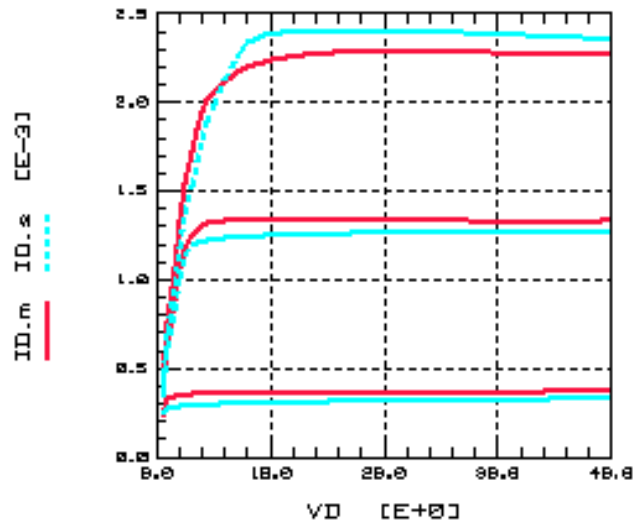
(c)

model (blue) & measurement (red):

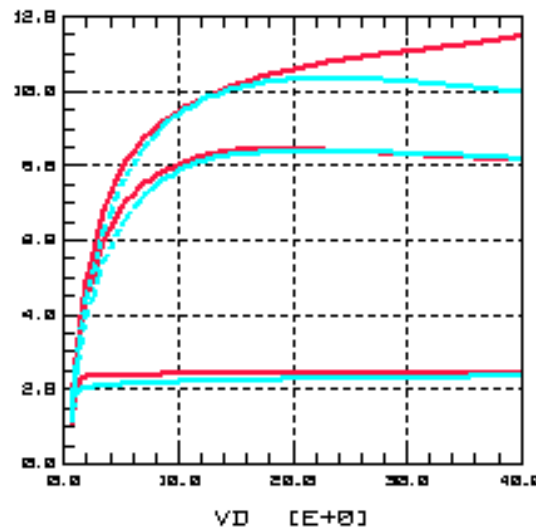
$I_D$  vs.  $V_G$  - a) minimum width, (b) medium width and (c) maximum width.



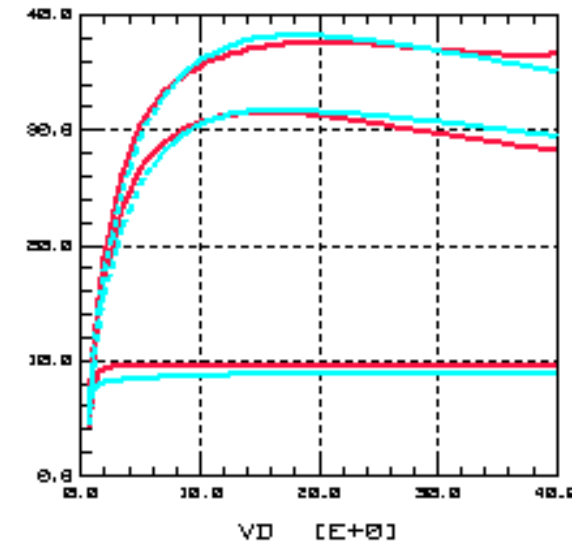
## Output Characteristics



(a)



(b)

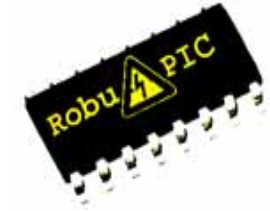


(c)

model (blue) & measurement (red):

$I_D$  vs.  $V_D$  for a) minimum width, (b) medium width and (c) maximum width.

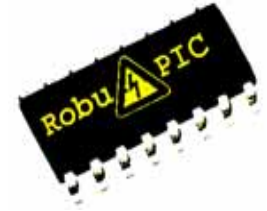
# Parameter Extraction and Model Calibration



- Required characteristics:
  - $I_D V_{G1}$  ( $I_D$  vs  $V_G$  for  $V_D = 0.1V-0.5V$ )
  - $I_D V_{G2}$  ( $I_D$  vs  $V_G$  for  $V_D = 1V-5V$ )
  - $I_D V_D$  ( $I_D$  vs  $V_D$  for entire  $V_G$ )
  - $C_{GD} V_G @ V_D = 0V$

<b>EKV Parameters</b>	<b>DC – 10</b>
<b>Drift Parameters</b>	<b>DC – 8</b>
<b>Fitting Parameters</b>	<b>AC – 3</b>
<b>SHE</b>	<b>3</b>

# Parameter Extraction and Model Calibration



- Extract  $V_{T0}$  and  $U_0$  at low  $V_D$  (50-100mV)

## Comments on $V_{T0}$ extraction

- Standard MOSFET extraction procedure provides reasonably good values
- For accurate extraction procedure
  - Our EDL paper, “[New Method for Threshold Voltage extraction of High Voltage MOSFETs Based on Gate-to-Drain Capacitance Measurement](#)”, expected to appear in July issue.

# Parameter Extraction and Model Calibration



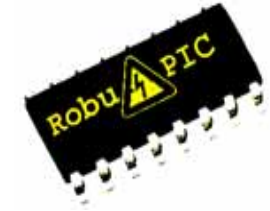
## DC Model Calibration procedure:

1.  $I_D V_{G1}$  – calibrate  $V_{T0}$ ,  $PHI$  and  $GAMMA$  for sub-threshold slope
2.  $I_D V_D$  – calibrate  $PHI$ ,  $GAMMA$ ,  $KP(= U0.COX)$ ,  $E0$ ,  $UCRIT$  and  $LAMBDA$  for saturation current
3.  $I_D V_{G1}$  and  $I_D V_{G2}$  – calibrate Drift parameters:  $\rho_{Drift}$ ,  $\theta_{Acc}$  for medium-high  $V_G$
4.  $I_D V_D$  – calibrate Drift parameters:  $VSAT$ ,  $\alpha_{vsat}$  for linear to saturation regime transition.
5. The rest of the EKV parameters – default values

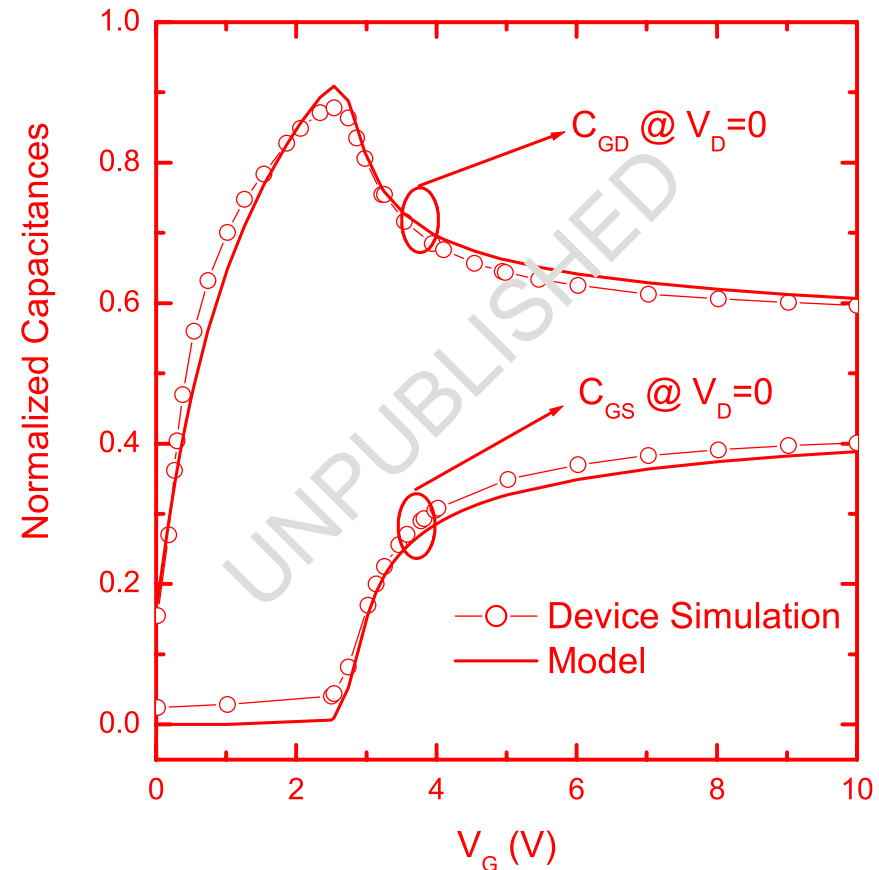
## AC Model Calibration procedure:

1. 3 fitting parameters - transition from inversion to accumulation on  $C_{GD}$  vs  $V_G$

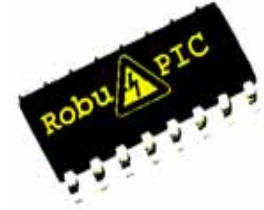
# Modeling of Lateral Non-uniform Doping in Intrinsic MOSFET



- A charge based analytical compact model developed
- Very Good results for DC and AC especially *peaks* on Capacitances



# Conclusion



- **A new model for L- & VDMOS devices is proposed**
- **Good performance in DC and AC operations**
  - Error ( $I_{DS}$ )  $\sim 5\%$
  - Error ( $g_m$ )  $\sim 5\%$
  - Error (*Capacitance*)  $\sim 25\%$
- **Tested for transient operations**
  
- **Model validated on industrial devices**
- **Excellent convergence and scalability**
- **Self-Heating effect included – No ill convergence**
- **Implemented in *Verilog-A* – Platform independent**
- **Tested on *ELDO*, *SABER*, *UltraSim* simulators**