Smart-power IC’s present many technical challenges both in their design and manufacturing. Design tools and methodologies constantly evolve to enable engineers to meet tougher requirements in terms of functionality, robustness, quality and cost. The ROBUSPIC project participates in this effort, by developing tools and methodologies to support the design of robust smart-power IC’s, with a special attention to system-level aspects.

The objective of the workshop is to describe recent advances in the field of simulation at system-level for smart-power applications. The workshop consists in a mix of invited papers and presentations by the ROBUSPIC project partners, covering:

- Two complementary approaches to system-level simulation: fast-spice and black-box behavioural modelling;
- Electro-thermal simulation at system-level;
- Accuracy of EMC simulations;
- Reliability requirements and simulation tools for Smart-power IC’s.

The workshop is intended for an audience of design engineers and researchers having an interest in the field of smart-power circuits and systems.

9:05 – 9:45 DC-DC Converter Design Phase Acceleration with Virtuoso® UltraSim Simulator
Invited talk by Mr Bouhamame and Depreeuw, Philips Semiconductors;

This paper describes the advantages of using the Virtuoso® UltraSim full-chip simulator during the design phase: time and accuracy comparisons with Virtuoso Spectre® Circuit Simulator for the simulation of a Smart Power IC, a DC-DC converter to tune RF filters. It uses a novel approach to decrease the output voltage by cascading two Dickson charge pumps. DC-DC converters represent a well-known challenge for analogue simulators, due to the very different time-constants involved in the switching clock and in the output power waveform. A typical simulation can last for 15 hours on a standard simulator like SPECTRE. Fast-Spice solvers, on the other hand, are quite successful in speeding up digital simulations, but the analogue simulation of smart-power IC’s represents a different challenge with requirements to handle combinations of very small (micro-volts, pico-amperes) or very large voltages and currents (hundred volts, several amperes). The DC-DC converter presented in this paper is the first one that we are able to simulate with a real accuracy and a speedup in simulation more than 300%, on a LINUX workstation. We explain how such simulation acceleration has been achieved.
9:45 – 10:15 **Full-chip simulation in smart-power IC’s**
Presentation by the project partners: Cadence, Bosch, AMI Semiconductors.

This paper describes the challenges facing designers of mixed-signal system-on-chip or system-in-the-package, and shows how third-generation circuit simulators as UltraSim address them. The advanced features of third-generation simulators are explained and put in the perspective of previous generations. Several examples of simulations which the newest generation handles particularly well are presented, and the talk concludes on a series of practical tips for mixed-signal simulation in large-scale systems.

10:45 – 11:15 **Behavioural models as an effective mean to speed up system-level simulations without sacrificing accuracy.**
Presentation by D. Schreurs, H. Taher, B. Nauwelaers from TELEMIC, KU Leuven, project partner.

Behavioural modelling is a powerful and universal technique to represent a device’s or circuit’s behaviour by an efficient model that only keeps the relevant dynamics. As a consequence, the major benefit of this modelling technique is the huge reduction in simulation time, enabling faster prototyping. The theory of this promising state-space modelling approach will be explained, and illustrated by various examples ranging from transistors (e.g., LDMOS) to circuits (e.g., op-amp).

11:15 – 11:55 **Full-chip transient temperature analysis.**
Invited talk by R. Chandra, Gradient Design Automation

To accurately predict circuit behaviour under varying temperature conditions it is necessary to account for the respective temperatures of individual circuit components during circuit simulation; otherwise the effects of electro-thermal coupling cannot be modelled. In complex mixed-signal designs like those in modern day smart power applications for automotive, mobile communications and avionics, full chip electro-thermal analysis is becoming increasingly important. Existing methods for transient temperature analysis do not effectively scale to the full chip level. This paper describes the objectives, requirements and a software capability for fully automated full chip level transient temperature analysis which is integrated with electrical simulation.
13:00 – 13:30 *Predicting the results of conducted EMC tests : critical factors determining accuracy.*

Presentation by project partners : Univ. of Zagreb and AMI Semiconductors.

It is very important to accurately estimate electromagnetic compatibility (EMC) of a circuit being designed. This presentation describes the extraction of the circuit models for conducted EMC simulations and identifies critical factors that determine the accuracy of the EMC simulations. The simulations and measurements are based on the standard IEC 61967-4 for conducted electromagnetic emissions (EME) and the standard IEC 62132-4 for electromagnetic immunity (EMI).

13:30 – 14:10 *Design Requirements for Automotive Reliability*

Invited talk by Mr. Von Tils from Robert Bosch

The presentation gives an overview of the evolution of automotive electronics. Customer expectation will be discussed, which lead to a reliability level for electronics in the car. A break down structure will demonstrate how the tough defect levels for semiconductors are being derived. Beside the requirement to aim for zero defect, some examples for increasing requirements to the robustness of electronic components will be shown. Diagnostic capability and integrated control logic may protect power semiconductors against overstress conditions. Examples will be given.

14:10 – 14:40 *Dynamic aging simulation of Smart Power circuits*

Presentation by project partners from R. Bosch, AMI Semiconductor and Cadence.

Operational conditions are increasingly challenging in Smart Power designs. Dynamic aging simulation allows to identify weak spots in the circuit and predict shift of design specifications, induced by wear-out mechanisms. This presentation describes the implementation process for dynamic aging simulation of hot carrier effects in DMOS device. A continuous model for the aging of the device is provided. Next, an extraction method to model the effect of hot carriers on model parameters is explained. Finally, the implementation in the analog design environment and the use model are presented.