

ROBUSPIC

Robust Mixed-Signal Design Methodologies for Smart Power IC's

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University of Zagreb

AMI Semiconductor

Robert Bosch

Contents

1 Introduction.....	3
2 Design flow and EMC	4
3 Netlisting strategies.....	5
3.1 Parasitics extraction	7
3.1.1 Technology overview.....	10
3.1.2 Assura – RC extraction	10
3.1.3 Full-wave 3D EM parasitics extraction – HFSS and Q3D	12
3.2 Simulations	13
3.2.1 DC analysis	14
3.2.2 Transient analysis.....	14
3.2.3 S–parameter analysis.....	16
3.3 S–parameter modeling	18
4 EMC models	20
4.1 IBIS and ICEM models.....	20
4.2 EMI current source ANN modeling.....	21
5 Conclusion	24
6 References.....	25

Original description of task:

Task 4.4: Electro-magnetic compatibility simulations

The purpose of this task is to develop models, (tools) and methodologies for realizing full-chip Electro-Magnetic Compatibility (EMC) analyses on Smart-Power ICs. AMIS, Bosh and University of Zagreb will work on formulating appropriate models of EM interference (EMI) sources and system components which are key for analyzing susceptibility to EMI. Extraction tools and simulation methodologies will be set-up to guarantee EMC of Smart-Power ICs.

1 Introduction

During the design process it is very important to estimate the EM behavior of the circuit being designed. Not only that electronic equipment producers are bounded by EMC standards but ICs are root causes of disturbances in electronic equipment and systems. Standards regarding EME (Electromagnetic Emission) and EMI (Electromagnetic Immunity) have to be simulated as the first step towards EM compliance.

Appropriate netlisting strategies and usable EMC models have to be determined to enable prefabrication EMC evaluation. The netlisting strategy implies the simplification of the netlist according to EMC demands and reasonable simulation time. It is very difficult to perform transistor level simulations for chip level EMC tests, for they are complex and require long simulation time. Therefore suitable models and their usability must be determined.

In Section 2 EMC task in design flow is outlined. Section 3 gives suggestions how to successfully create netlists for EMC simulations. It also addresses parasitic extraction (RC and full wave EM) and comments various simulation strategies. Section 4 describes some of the EMC models. Also, the usage of artificial neural network for EMI current source modeling is shown. Section 5 brings conclusion.

2 Design flow and EMC

To assure EMC compliance, a place for EMC in the overall design flow must be determined. Figure 1 shows a design flow that includes the EMC simulations.

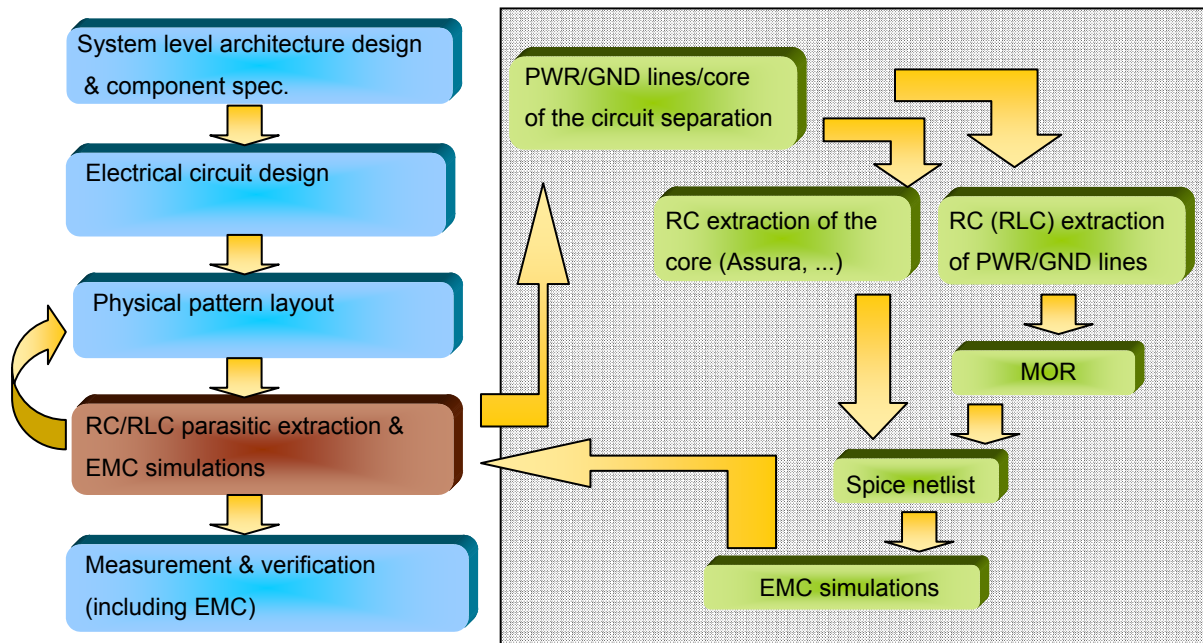


Figure 1 : Design flow with EMC requirements.

In the following sections it is shown that EMC simulations are firmly related to parasitics extraction. Even more, it is not possible to ensure EMC compliance without accurate parasitics extraction. Thus, the EMC simulations take part after parasitics extraction is performed. To facilitate EMC simulations, the original layout is separated into two parts: a part containing power and ground lines, and a part containing the core of the circuit. After both the circuit core and supply system parasitics are extracted, EMC simulations are carried out on the joined netlist.

3 Netlisting strategies

As shown in Figure 2, a modular approach is used for EMC analysis. The C/C++ code is developed that supports input of GDSII format. It enables separation of supply network from the core of the cell. Once the GDSII file of the design circuit is read in, the user can define set of nodes to be analyzed. The code extracts the objects (rectangles, polygons and vias) associated with the defined nodes and saves these objects into the first GDSII output file. All other objects from the input GDSII file are saved into the second GDSII output file. In such way a separate simulation or extraction of parasitics can be performed on only one part of the initial design and consequently, each part of the design can be treated with different simulation/extraction tool.

Figure 3 shows the irregular PWR/GND structure used to demonstrate the proposed method. The XOR cell (3 inverters, 2 AND and 1 OR circuit) is connected at the right end of the PWR/GND structure.

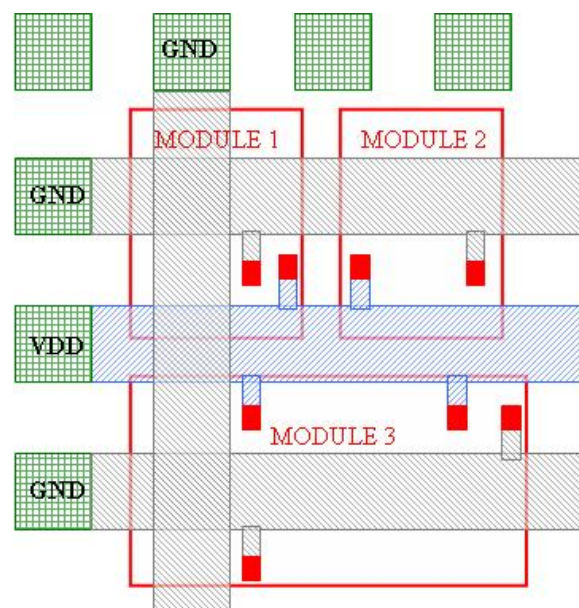


Figure 2 : Modular approach used for EMC analysis.

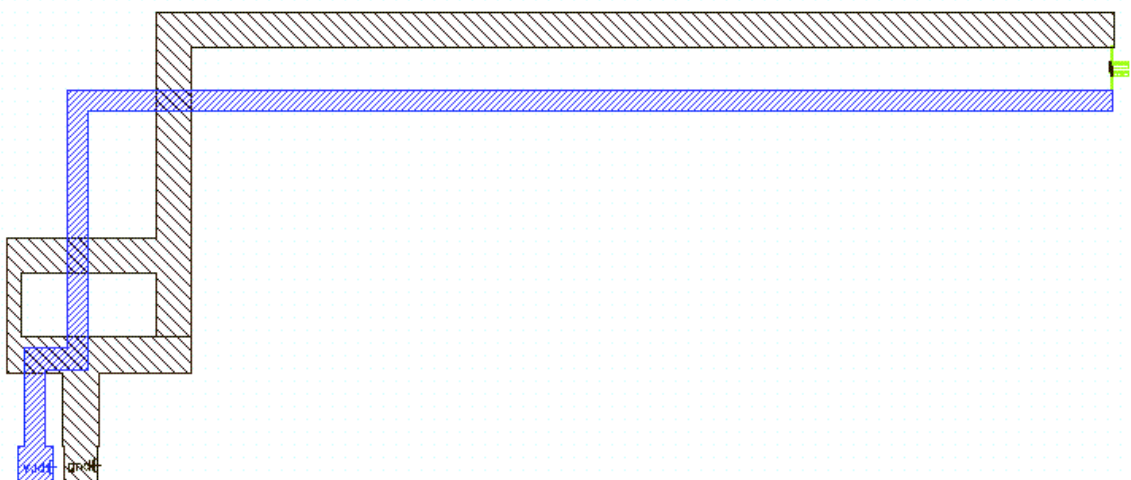


Figure 3 : Layout of the irregular PWR/GND structure.

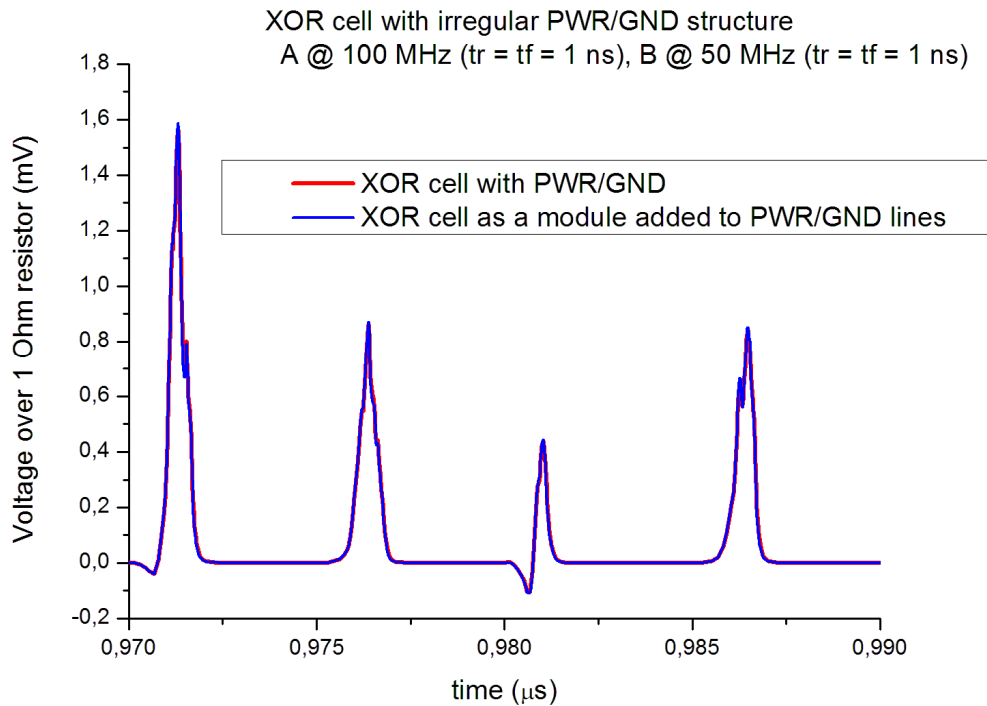


Figure 4 : Simulations of the whole circuit (red line) and the simulations obtained by joining the netlists (blue line).

Firstly, the whole structure together with the circuit is extracted by Assura (RC extraction). Secondly, the XOR cell is extracted by Assura and the PWR/GND structure also by Assura, but separately from the XOR cell. Then, the two netlists are combined into one netlist. As expected, the same results are obtained by both approaches (see Figure 4).

Assura extracts RC parasitics of the PWR/GND structure. However, the EM behavior of the structure is more complex. Figure 5 shows the XOR cell extracted by Assura with the PWR/GND structure extracted by Q3D, the quasi-static RLC extractor.

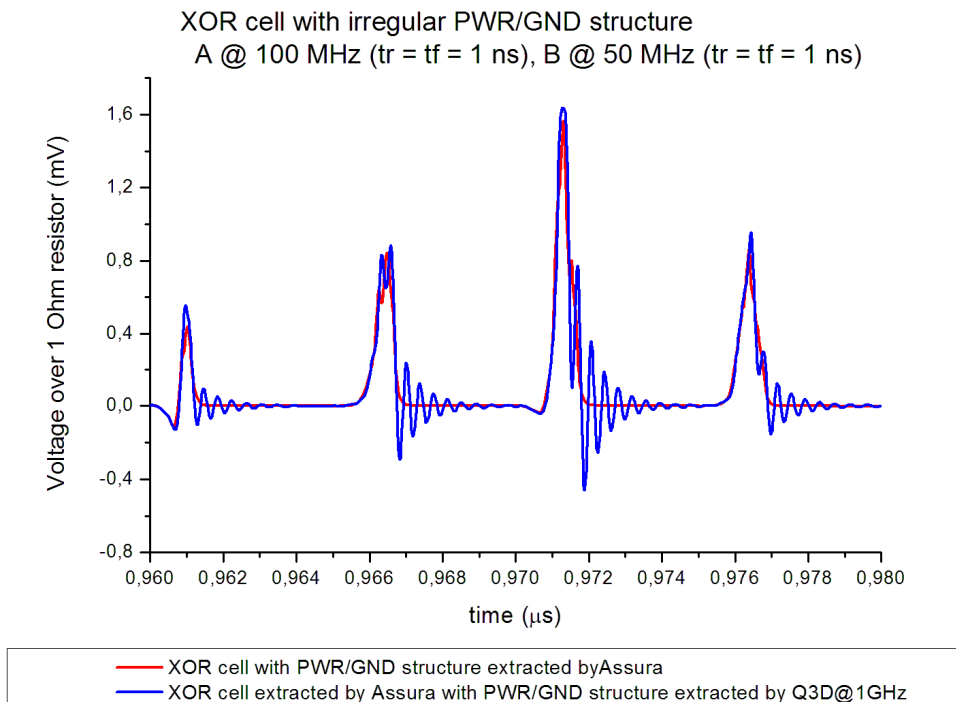


Figure 5 : Voltage over 1 Ohm resistor: Assura extracted PWR/GND lines (red) and Q3D extracted PWR/GND lines (blue).

3.1 Parasitics extraction

It is important to determine the influence of the parasitics on the EMC. For that reason, three different parasitics extractors are used:

Cadence Assura RC extractor [1],

Ansoft HFSS [2],

Ansoft Q3D extractor [3].

Cadence Assura is used to extract parasitic resistances and capacitances. Ansoft's tools are used to calculate S-parameter and parasitic resistance, capacitance and inductance from 3D EM simulations.

To determine the influence of the PWR/GND parasitics on the emission levels according to the IEC 61967-4 standard [4], the inverter cell with long power and ground lines is simulated (inverter connected to 1500 μm long and 1 μm wide PWR/GND lines, with 11 μm spacing between them).

Firstly, just for the sake of simplicity, RC extraction by Assura is used to determine the influence of PWR/GND parasitics. The influence of PWR/GND parasitics on the voltage over 1 Ohm resistor can be seen in Figure 6 and the influence on the emission levels is shown in Figure 7. When the parasitics are included, the dynamic current through the GND line is filtered (the change of the current is slower and the delay is introduced).

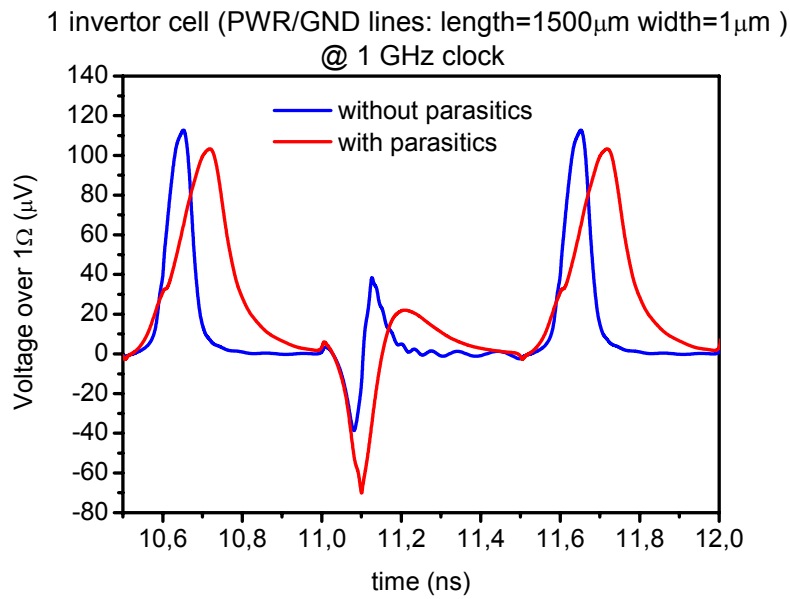


Figure 6 : Influence of PWR/GND parasitics on the voltage over 1 Ohm for the long inverter cell (parasitics extracted by Assura).

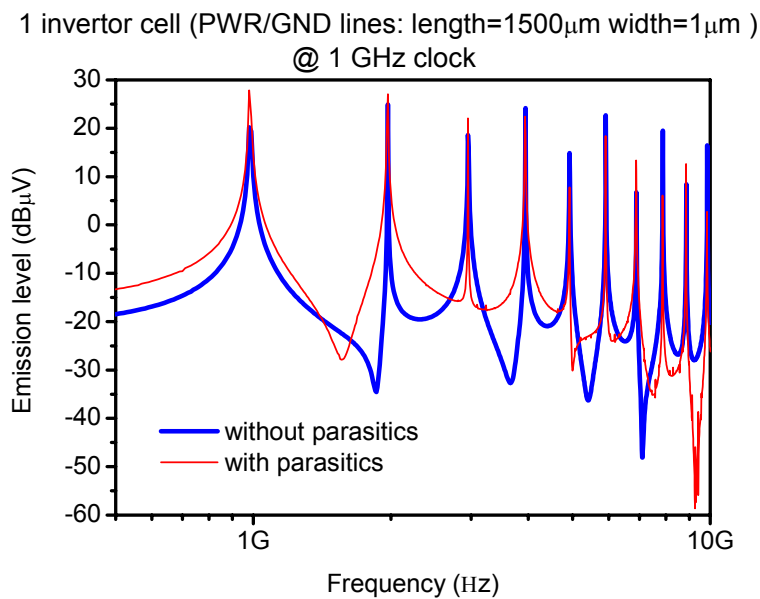


Figure 7 : Influence of PWR/GND parasitics on the emission levels for the long inverter cell (parasitics extracted by Assura).

Figures 8 and 9 show the voltage over 1 Ohm resistor and emission levels for the line widths $w = 1 \mu\text{m}$ and $w = 5 \mu\text{m}$. The narrower lines represent higher impedance which results in lower

switching currents. The example clearly shows that over-design (the usage of wider lines) does not necessarily result in better EMC performance.

More complicated circuits are also simulated. Circuit with 31 inverter cells is analyzed. Results can be seen in Figures 11 and 12 in Section 3.1.2.

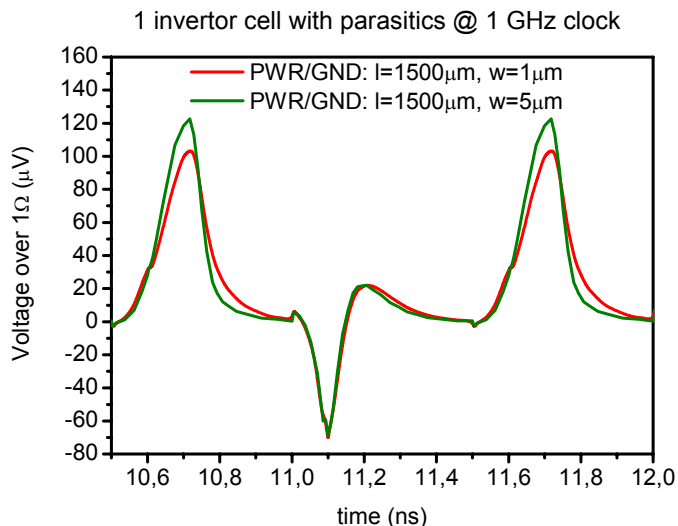


Figure 8 : Influence of PWR/GND parasitics on the voltage over 1 Ohm for different PWR/GND lines width (parasitics extracted by Assura).

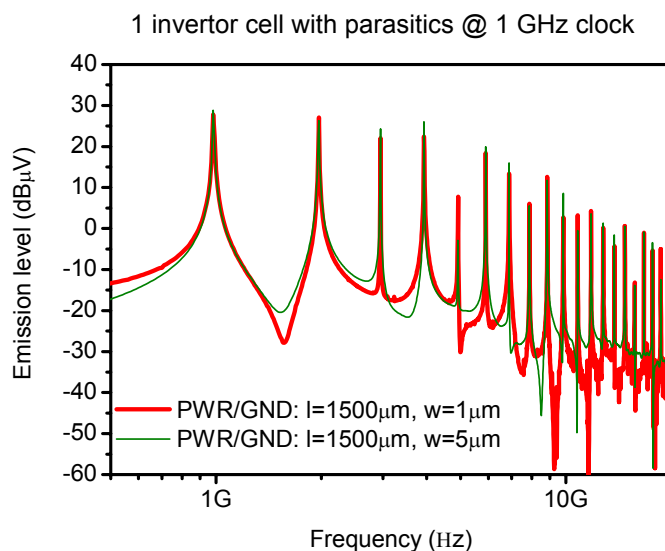


Figure 9: Influence of PWR/GND parasitics on the emission levels for different PWR/GND lines width (parasitics extracted by Assura).

3.1.1 Technology overview

All parasitic element extractor tools, as well as full wave 3D EM extractors such as Ansoft's HFSS and Q3D, use a set of technology parameters. Figure 10 shows a wafer cross – section for the CMOS 0.35 um technology (not all details are shown).

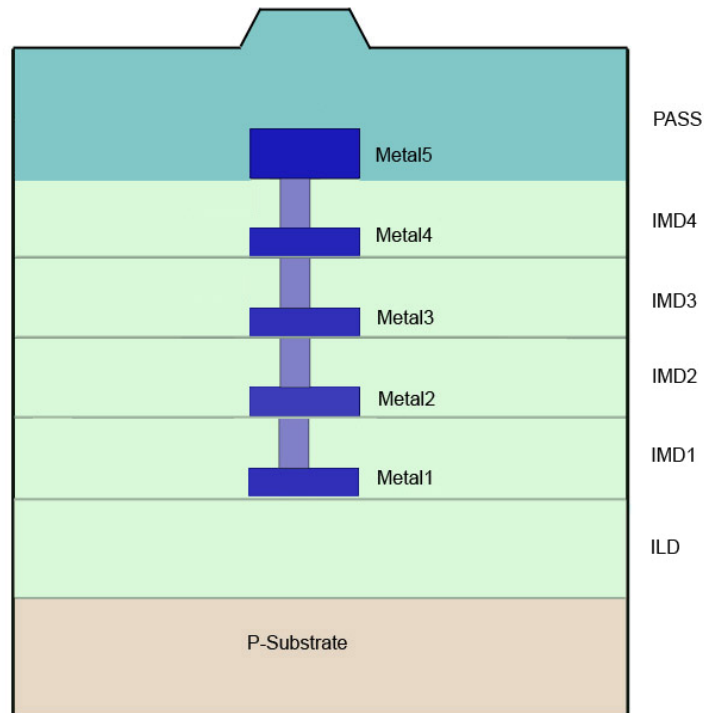


Figure 10 : Wafer cross – section for the used technology.

Both geometrical and electrical parameters have to be defined for full wave 3D EM simulations. Each material is defined by its name, conductivity and/or relative permittivity and thickness. 3D EM solvers usually support GDSII import.

3.1.2 Assura – RC extraction

Cadence Assura extractor is commonly used tool and existing design flows incorporate Assura parasitic extraction.

Assura RC extractor may be used to extract the parasitics of the core circuit, as well as parasitics of the PWR/GND lines. Also, in Sections 3.2.2 and 3.2.3, Assura RC extractor is compared with 3D EM field solver to determine the influence of parasitic self and mutual inductance.

To address the importance of parasitic extraction, the circuit with 31 inverter cells is simulated (see Figures 11 and 12). Also, in this example, Assura extracted RC parasitics of the PWR/GND lines act as filter, lowering the current amplitude and introducing delay.

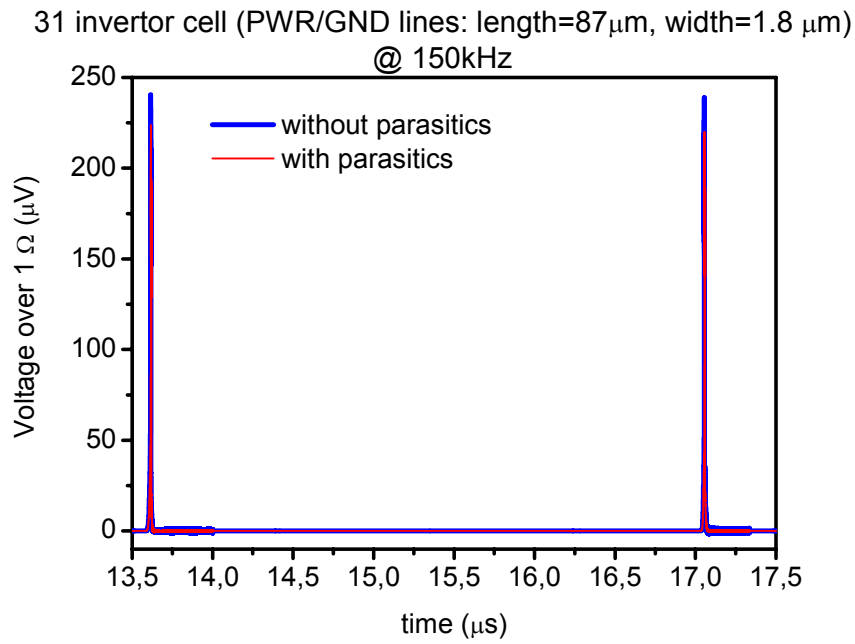


Figure 11 : Influence of PWR/GND line width on the voltage over 1 Ohm for 31 inverter cell (parasitics extracted by Assura).

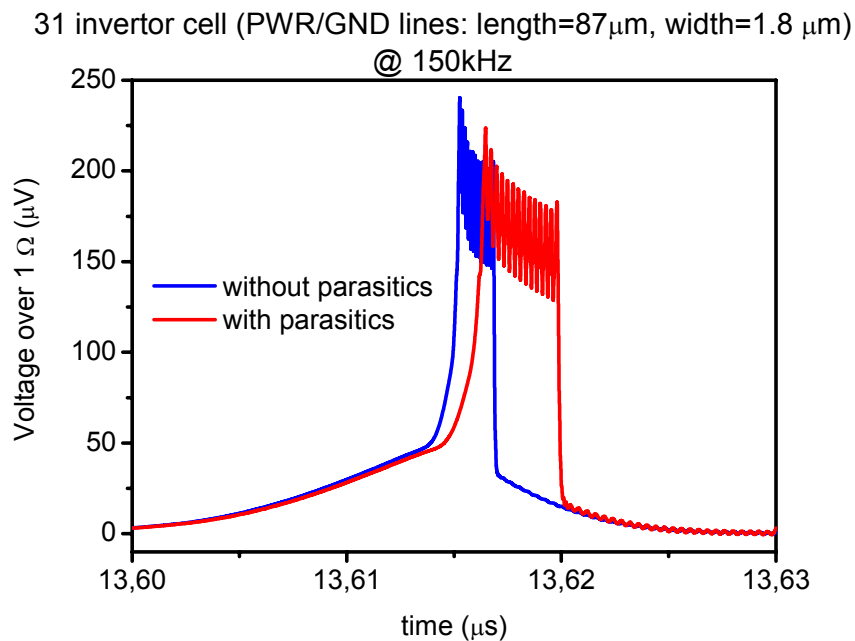


Figure 12 : Influence of PWR/GND line width on the voltage over 1 Ohm for 31 inverter cell (parasitics extracted by Assura).

3.1.3 Full-wave 3D EM parasitics extraction – HFSS and Q3D

3D EM parasitics extraction is performed by two different software packages. Both of them use finite element method.

HFSS calculates electromagnetic behavior of a structure and represents it in the form of scattering parameters (S-parameters). It is possible to specify whether to solve the problem at one specific frequency or at a range of frequencies. It is suitable for problems in high-frequency domain. HFSS is a full-wave EM simulator.

Q3D Extractor is 3D quasi-static EM solver that can be used to electrically characterize 3D interconnect structures. The output of Q3D is lumped equivalent circuit model in several SPICE formats.

Both HFSS and Q3D have 3D Modeler which can import GDSII files. After the GDSII file is imported and 3D model with proper material characteristics are generated, they can be used in both HFSS and Q3D. So, creating a model in HFSS and Q3D is equal, but defining ports and performing simulations is not. The ports in HFSS can either be “wave” or “lumped” ports, and the ports in Q3D are sources and sinks.

In HFSS, for simulations concerning chip level parasitics, the most appropriate are lumped ports and the procedure is as follows. After the 3D model is created, the boundaries (power plane, radiation etc.) and excitations (lumped ports) are defined. The lumped ports are placed at points where appropriate core cells are detached and at points where probes will be placed. After the solution frequency or frequency range are defined, automatic mesh generation and subsequently simulations are performed. The results are S-parameters which describe the PWR/GND structure. S-parameters are then exported to Touchstone file which is compatible with Spectre.

Q3D Extractor on the other hand is simpler tool for extraction of chip level parasitics. When 3D model in Q3D is constructed, appropriate sources and sinks are attached. The sources are attached where probes will be placed and the sinks are connected at the places where the core cell will be connected. Q3D is capable of automatically identifying the nets. The solution frequency must be defined and mesh generation and the solver are started. The results can be exported to a netlist containing subcircuit which describes power and ground parasitics in the form of lumped elements. Spectre and PSPICE netlist formats are among supported types.

To address the inductance issue, the inductor cell with long supply lines is extracted in HFSS as well. Figure 13 gives the comparison of the results obtained by Assura and HFSS.

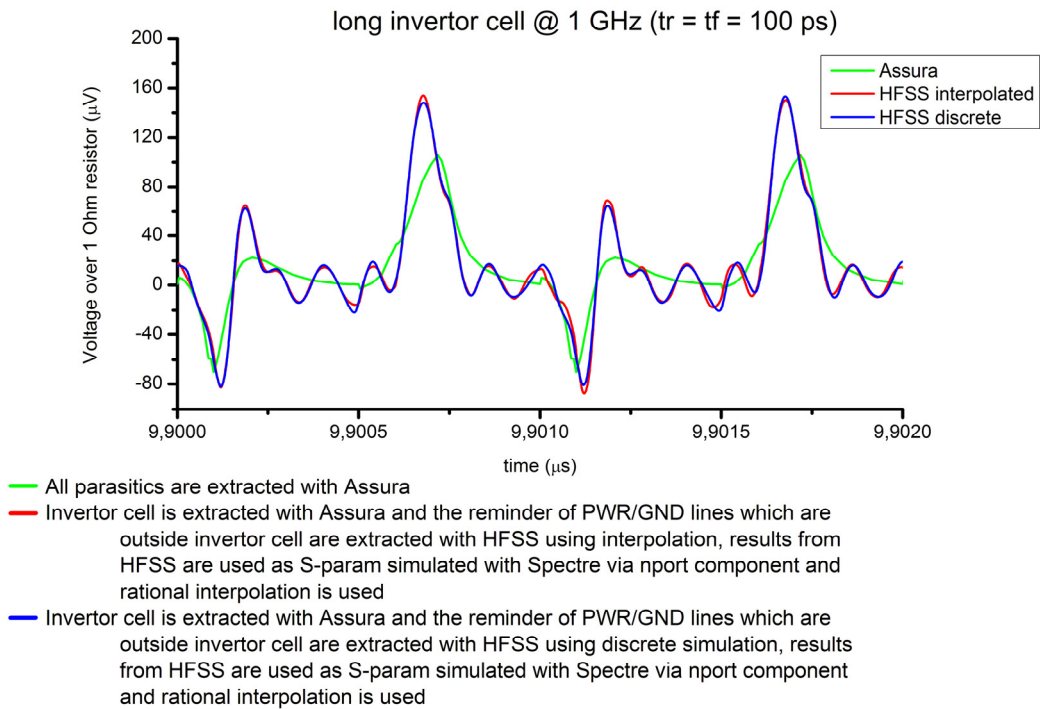


Figure 13 : Influence of PWR/GND parasitics on the voltage over 1 Ohm for the long inverter cell.

Assura was used as RC parasitic extractor. The long PWR/GND lines represent RC filter and they smoothen high frequency components. HFSS, however, describes all parasitic elements (inductance also) through 3D EM simulations. In this case PWR/GND lines are relatively long, narrow and the spacing between them is rather small. Because of that, the inductive effect can not be ignored. It can be seen as oscillations.

In Figure 13 HFSS is used in two ways:

- a) Extraction for specified set of frequencies;
- b) Interpolated extraction for specified frequency range.

If there is enough frequencies defined in the specified set of frequencies, as in this case, then there is no difference compared to the results for interpolated extraction. Interpolated extraction is much faster than the extraction obtained for the specified set of frequencies. In interpolated extraction HFSS finds characteristic frequencies by itself and converges much faster.

3.2 Simulations

Depending on the extractor used, output can be either in the form of subcircuit Spectre netlist or in form of S-parameters. The core of the cell extracted by Assura is in the form of subcircuit Spectre netlist, but PWR/GND structure can be available both in the form of S-parameters and subcircuit Spectre netlist.

In Spectre, S-parameters are simulated via S-parameter subcircuit (nport component). Linear, cubic spline or rational fitting can be used. Although linear and spline interpolations are less time consuming, they can result in active behavior of the model, i.e. oscillations. When using rational fitting, the data is interpolated and extrapolated using a rational function fit.

When the S-parameter data is complicated, rational fitting can be quite time consuming so the reduced order model (ROM) should be stored for future re-use. The order of the model can be either specified or automatically determined. Unfortunately ROM procedure can result in serious stability problems. This suggests that lumped R-L-C models of S-parameters representing supply networks should be developed. In Section 3.3 RLC cascade is used to model S-parameters.

3.2.1 DC analysis

DC analysis is used to verify the DC solution obtained from full-wave 3D EM solver. High-frequency field solvers usually extrapolate DC solution, therefore it is reasonable to perform DC analysis to check the results.

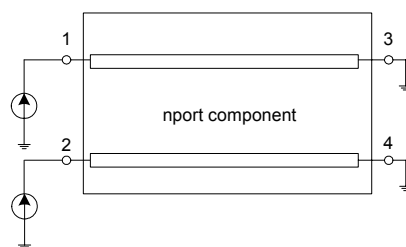


Figure 14 : Setup used to examine DC solution.

In Figure 14 setup used to test the DC solution obtained from EM solver is presented. The current sources produce 1 A so the voltage at ports '1' and '2' of the lines equals the resistance of the lines at DC.

HFSS was used to extract S-parameters for two parallel lines with spacing of 11 μm , 1500 μm long and 1 μm wide. When S-parameters were analyzed via nport component in Spectre, according to Figure 13 the resulting resistance was 101.317 Ohm.

The resistance was also calculated from the sheet resistance. The calculated resistance of the line was 101.630 Ohm, which is very good agreement.

3.2.2 Transient analysis

Transient analysis is performed to determine emission levels. Emission levels are determined in the following way. When the parasitics for the whole design are extracted and backannotated, transient analysis is performed to determine voltage over 1 Ohm resistor according to IEC 61967-4 [4]. Using the fast Fourier transform, the signal is then analyzed in frequency domain and emission levels are determined.

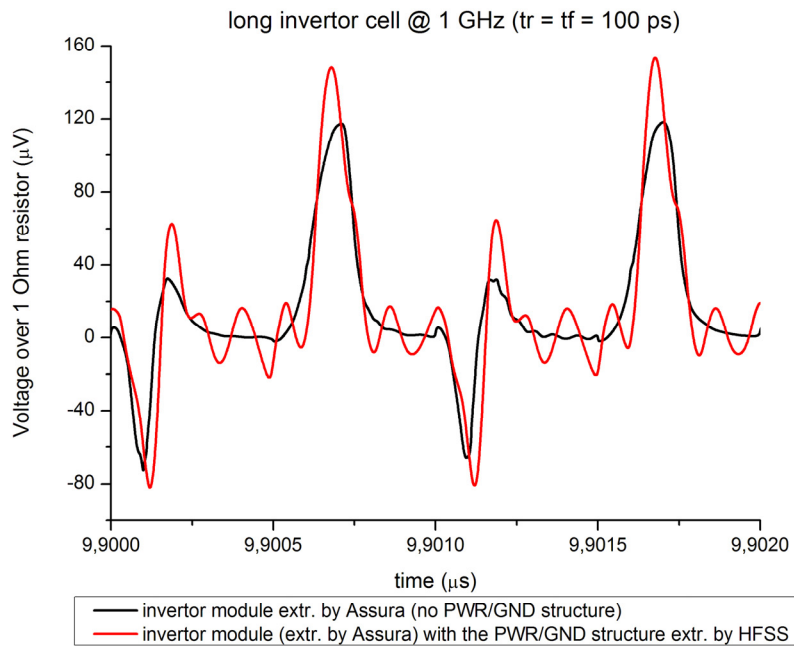


Figure 15 : Voltage over 1 Ohm resistor: inverter cell without PWR/GND structure (black line), and inverter cell with HFSS extracted PWR/GND lines (red line).

In Figure 15 one inverter module is compared to one inverter module with added HFSS extracted PWR/GND lines. It can be seen that oscillations occur after the PWR/GND netlist obtained by HFSS is joined with the inverter netlist.

The simulation of S-parameters in the time domain can be unstable. DC level is often affected. Figure 16 shows the voltage over 1 Ohm resistor when Assura, HFSS and Q3D are used. The simulation of the circuit with HFSS S-parameters of the PWR/GND structure shows a small shift in DC level.

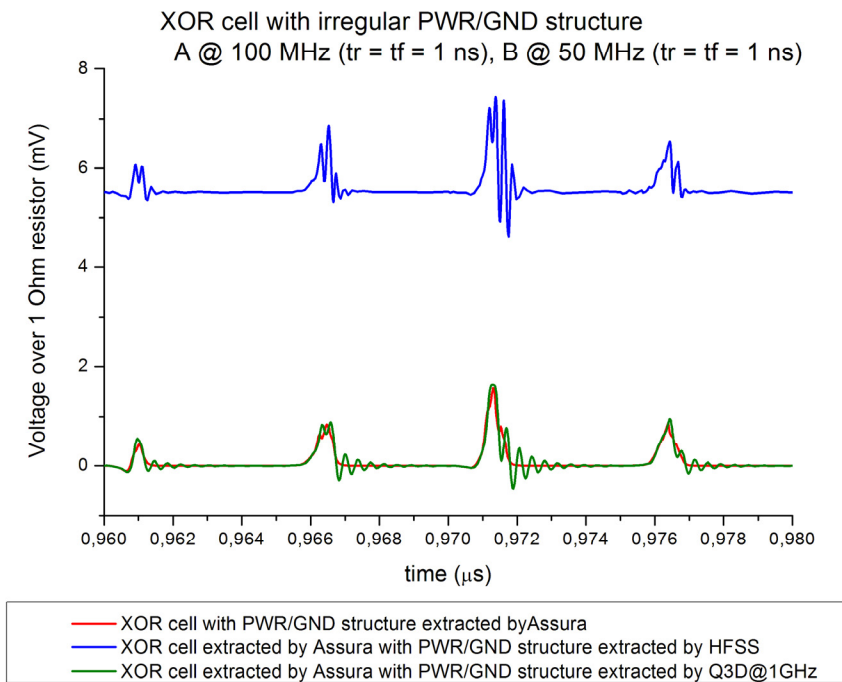


Figure 16 : Voltage over 1 Ohm resistor for XOR cell with irregular PWR/GND structure.

3.2.3 S-parameter analysis

The S-parameters of the PWR/ GND structure obtained by 3D EM simulator HFSS can be used as the reference result. The various methods for parasitic extraction can be compared by comparing the corresponding S-parameters in the frequency domain. As mentioned before, HFSS gives results in the form of S-parameters, but Assura and Q3D produce the lumped element subcircuit. These subcircuits are then analyzed with S-parameter analysis in Spectre. Spectre writes the results in Touchstone file.

The comparison of S-parameters for the irregular PWR/GND structure (see Figure 3) is shown in Figures 17 and 18. Figure 17 shows the comparison of the magnitudes, and Figure 18 compares the angle. The parameter S24 represents the transmission between the input and output port of the GND line.

Up to 1 GHz, the difference is less than 1 dB for the magnitude, and then it gradually increases to less than 2 dB up to the first resonant frequency at approximately 8.5 GHz.

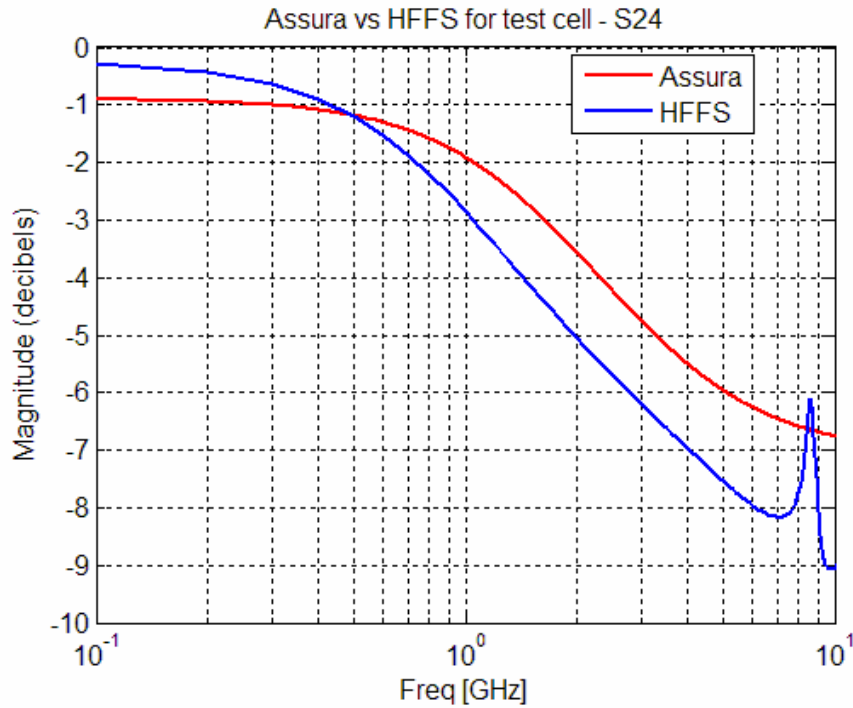


Figure 17 : Magnitude of S24: comparison between RC and full wave 3D EM solver for irregular PWR/GND structure.

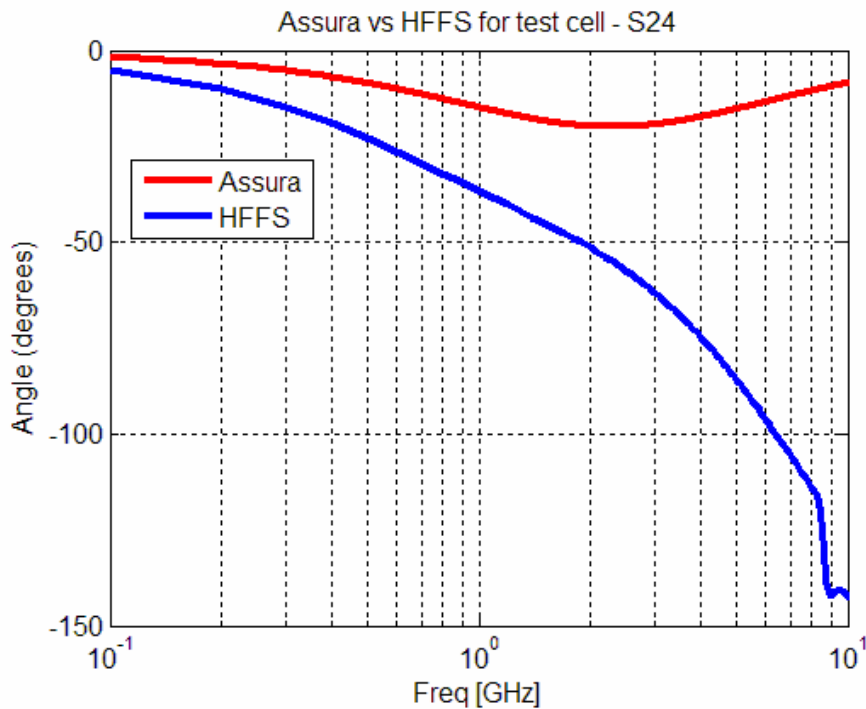


Figure 18 : Angle of S24: comparison between RC and full wave 3D EM solver for irregular PWR/GND structure.

3.3 S-parameter modeling

Although it is possible to simulate the design when PWR/GND lines are in the form of S-parameters, the problems with stability may occur. Lumped elements are more appropriate for circuit analysis. Metaheuristic approaches for S-parameter data modeling have been explored in literature. Some of them use genetic algorithms [5] and some use particle swarm intelligence [6].

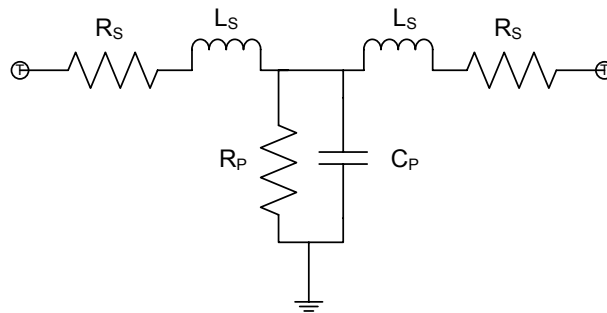


Figure 19 : T-network used to model S-parameter data.

The T-network shown in Figure 19 is used to model the S-parameter data for the PWR/GND line. The number of cascades used to model the net is determined according to the number of slopes in S-parameter data. Three different approaches are used to find the values of the parameters for the T-network:

- a) direct pattern search;
- b) genetic algorithms (GA);
- c) particle swarm optimization (PSO).

The simulated examples show that for data that can be described by one T-network direct pattern search is the best method. It converges very fast.

On the other hand, if the S-parameter dataset is more complex, direct pattern search has convergence problems. Metaheuristic approaches such as genetic algorithms and particle swarm optimization show promising results. Additional work should be performed to find the best types of genetic algorithms and PSO models.

Figure 20 shows the S-parameter magnitude for irregular PWR/GND structure. In this example, S-parameters from the Q3D extracted netlist are modeled. The model consists of two T-networks shown in Figure 19. The modeling is done by direct pattern search. It takes approximately 45 min at P4 (3.2 GHz, 512 MB) using the Matlab toolbox.

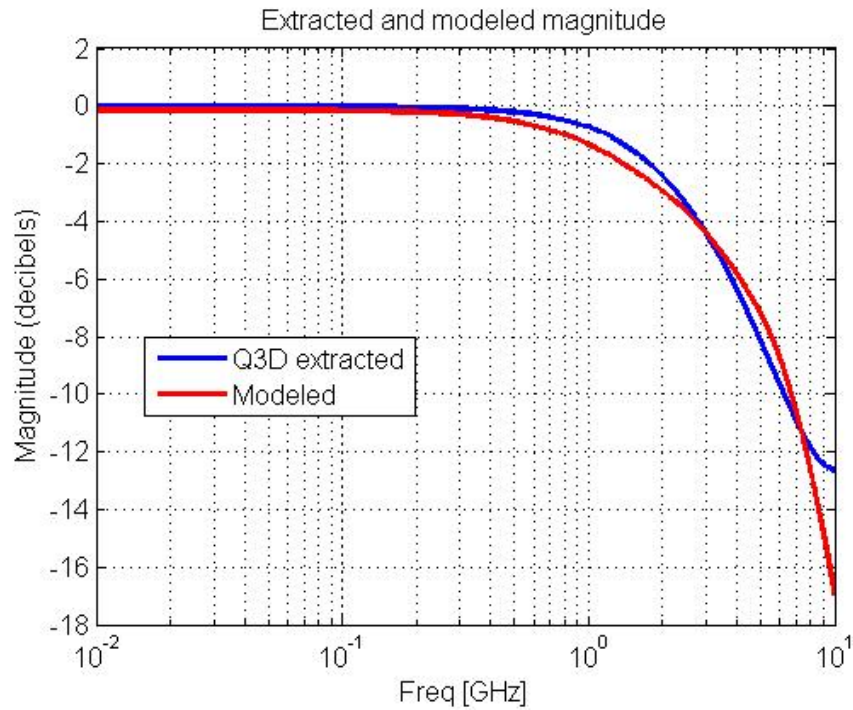


Figure 20 : Magnitude of S24: comparison between Q3D and T-network model for the irregular PWR/GND structure.

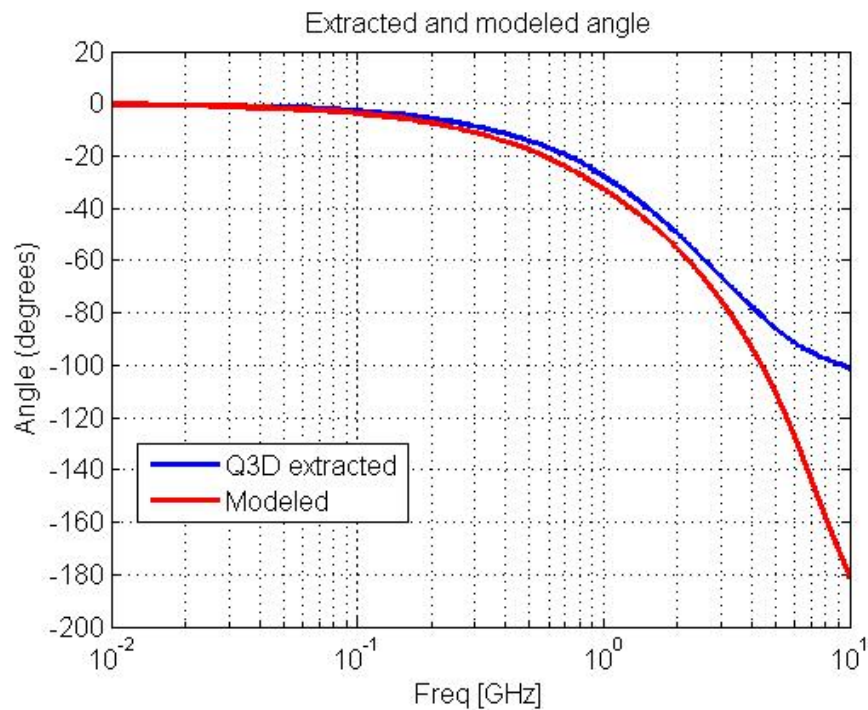


Figure 21 : Angle of S24: comparison between Q3D and T-network model for the irregular PWR/GND structure.

4 EMC models

4.1 IBIS and ICEM models

The objective of the ICEM model (Integrated Circuit Electromagnetic Model) is to propose electrical modeling for conducted and radiation emission prediction. ICEM model consists of two sub-models:

- The PDN sub-model stands for Distribution Network sub-model,
- The IA sub-model stands for Internal Activity sub-model.

The PDN sub-model models the power network of the IC and the IA sub-model models the IC activity as a current generator. The basic architecture of the ICEM model is shown in Figure 22.

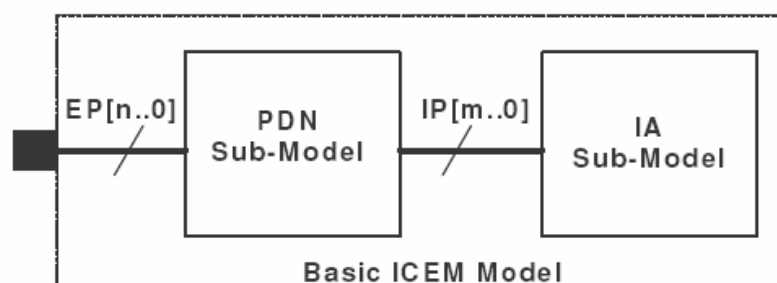


Figure 22 : Basic architecture of the ICEM model [7].

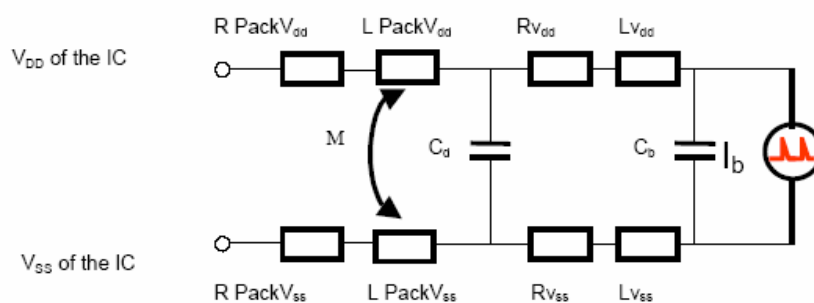


Figure 23 : Simple ICEM IC model [8].

A simple ICEM IC model is presented in Figure 23. Two methods can be used to model the power network of the IC. The first one is based on the extraction of the parasitic elements during the design phase (silicon lay-out, package, bond wires, ...). The second one is based on measurements.

A maximum frequency of the model should be defined. Above this maximum frequency, the level of harmonics should be low enough not to influence the level of conducted and radiated emissions.

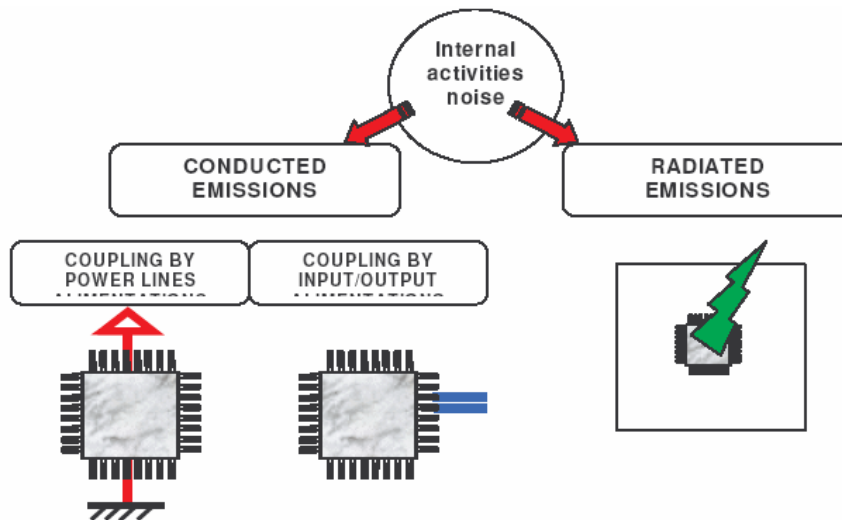


Figure 24 : Coupling mechanisms covered by ICEM [7].

The following coupling mechanisms of the internal activities for conducted emission (see Figure 24) are proposed in the ICEM model:

- a) Conducted emissions through supply lines,

The current spikes created inside the die are partially reduced thanks to the on-chip decoupling capacitance. Anyhow, a significant portion of the current spikes is present at the power-supply pins of the chip. This current could be measured according to the IEC 61967 standard.

- b) Conducted emissions through input/output lines,

The internal voltage drops generated by the current spikes create noise on the I/Os through direct connection, parasitic capacitive and inductive couplings and/or through common impedance. The PCB wires connected to the I/O can act as antennas and propagate electromagnetic emissions. The measurement set-up is done according to IEC 61967 standard.

ICM 1.0 [9] contains a specification for general purpose interconnects modeling in an IBIS (I/O Buffer Information Specification) compatible format. It was written to provide means for modeling all electrical interconnect types, including connectors, cables, packages, and printed circuit boards. IBIS is a fast and accurate Behavioral method of modeling I/O buffers based on V/I curve data derived from measurements or full circuit simulation.

4.2 EMI current source ANN modeling

A simple and efficient method of modeling IC EMI current sources using artificial neural networks is presented. The behavioral modeling approach is presently the major method for system simulation in industrial applications. The universal approximation property of ANN provides a basis for representing the analog, nonlinear, dynamic circuit, overcoming the accuracy limitations in conventional behavioral models.

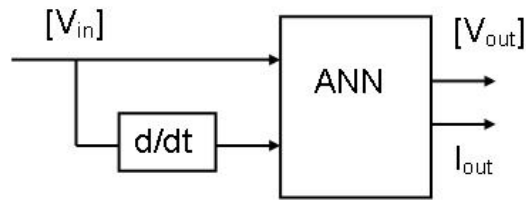


Figure 25 : Inputs and outputs of the ANN used to model EMI current source.

The input of the ANN is the input voltage and derivations of the input voltage. The output of the ANN is the output voltage and current that flows through the circuit as show in the Figure 25. This ANN can approximate the behavior of the circuit and its power lines. The main difference from the ICEM model is that the behavior of the circuit is also modeled. In this way, the switching/transition states of the circuits can be accurately modeled. Each of these submodels can therefore be connected in one (large and accurate) model as shown in the Figure 26.

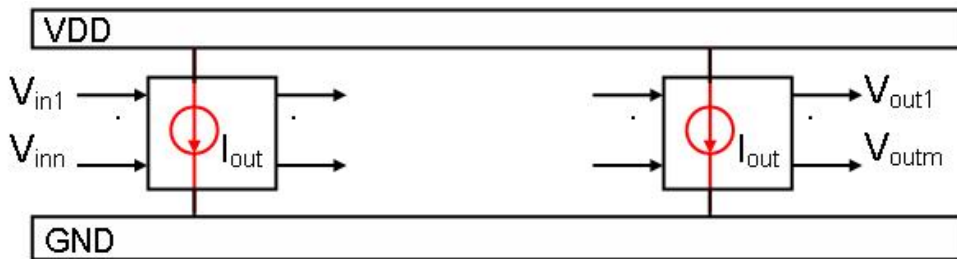


Figure 26 : Diagram of the proposed modular modeling.

A training data set is generated by applying the frequency modulated sinusoid to the input and measuring (or simulating) the voltage at the output and current through the circuit. The frequency range of the frequency modulated sinusoid must be sufficient to cover the standard behavior of the circuit. The accuracy of the model can be adjusted by adding neurons into ANN.

A simple example of the IC EMI current source modeling is presented in Figures 27 and 28. Figure 27 and 28 show the comparison between device-level and ANN model of the EMI current source simulations for inverter cell. For the training, frequency modulated sinusoid with duration of 1 μ s, amplitude from GND to VDD and frequency from 0 to 4 GHz, is used.

The model yields reasonable results for situations not specified in the learning data set because of the generalization property of artificial neural networks and it is suitable for modeling based on measurements.

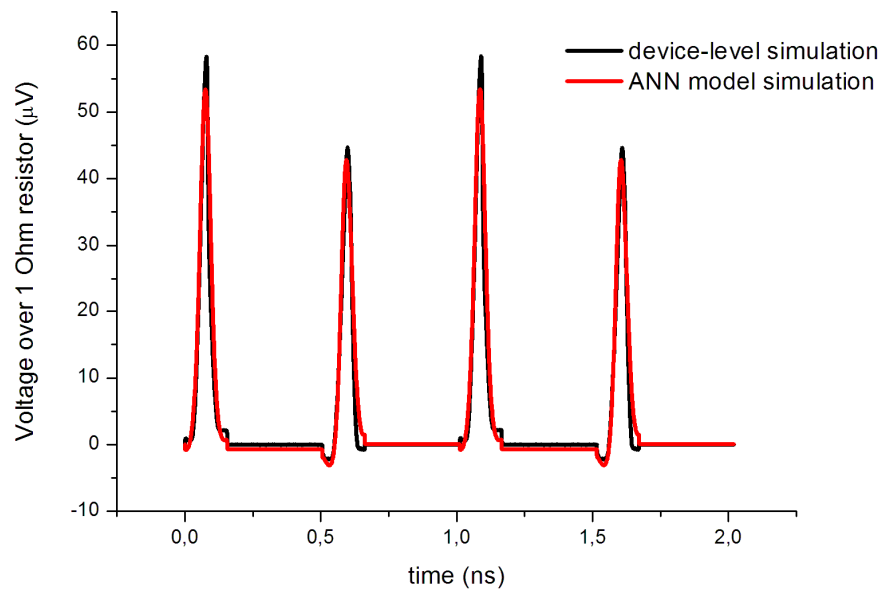


Figure 27 : Voltage over 1 Ohm resistor: device-level and EMI current source ANN model simulations for inverter cell.

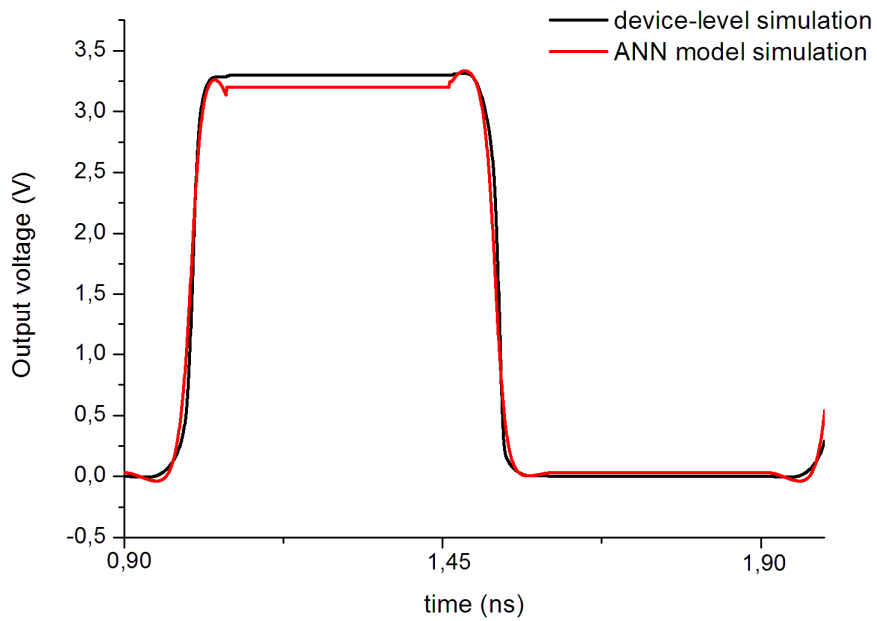


Figure 28 : Output voltage of the inverter cell: device-level and ANN model simulations.

5 Conclusion

This report describes the role of EMC simulations in the IC design flow. It emphasizes the importance of accurate parasitics extraction. The parasitics of both the circuit and the power/ground supply lines have to be accurately determined. It is shown that over-designing (e.g. using wider power lines) is not necessarily beneficial with respect to the EMC aspect of the design.

Various netlisting strategies are demonstrated on a simple and on irregular power supply network. Either a simple inverter, 31 inverter cells or an XOR cell has been investigated.

The circuit simulations have been performed within the Cadence design environment. The parasitics extraction of the power supply network has been performed by Cadence Assura or Ansoft tools HFSS or Q3D, and the results have been compared. DC, transient and S-parameter simulations have been run.

Modeling of the power supply network by a cascade of T-networks and modeling of the EMI current source has been demonstrated.

6 References

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