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EKV based DMOS Model extension for V-DMOS

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1. Introduction –

A new compact model for DC and AC circuit simulation of high voltage VDMOS transistor is presented. The modeling strategy is based on the core of the EKV physical MOSFET model for the intrinsic MOS while the drift segment is separately modeled. Self-heating effect is included by an equivalent electro-thermal circuit approach. The model is verified with both TCAD simulations and measured data and very good accuracy is observed for the DC component. The charge based AC compact modeling is valid for a wide range of gate and drain voltage. The special gate-to-source and gate-to-drain capacitance characteristics of VDMOS are accurately predicted. This model provides excellent trade-off between speed, convergence and accuracy, being suitable for circuit simulation in any regime of operation of HV MOSFETs including self-heating and impact ionization effect.

2. DC Compact Model –

The cross section of the VDMOS device is shown in fig.1 (a). In order to keep the parasitic BJT off, the source and body are tied in the measurements of these devices. Only half of the device is considered as it is symmetric along middle of the drift region (see dashed line in fig. 1(b)). It has been shown in [1] that the intrinsic drain voltage ($V_K$) always remains at low values for entire bias domain and the intrinsic MOS part can be accurately modeled using low voltage MOSFET model. Based on the concept of intrinsic drain voltage, we consider our device divided into an intrinsic MOSFET region and a drift region as shown in fig. 1(b). The intrinsic transistor part is modeled using low voltage EKV model [2, 3]. The model has charge-based description and a small number of parameters. The drift region is modeled using bias a dependent resistance, which provides accuracy and also fast convergence.
2.1. Intrinsic MOSFET Modeling

For intrinsic MOS part, we use EKV MOSFET model (version 2.6) [2]. The MOSFET drain current ($V_K$ to $V_S$ in our model) in the EKV model is expressed as:

$$I_{KS} = I_S \cdot (i_f - i_r)$$  \hspace{1cm} \text{Eq. (1)}

Where $I_S$ is the specific current. $i_f$ and $i_r$ are the forward and reverse normalized current respectively and given below:

$$i_f = \left[ \ln(1 + e^{\frac{v_p - v_s}{2}}) \right]^2$$  \hspace{1cm} \text{Eq. (2)}

$$i_r = \left[ \ln(1 + e^{\frac{v_p - v_k}{2}}) \right]^2$$  \hspace{1cm} \text{Eq. (3)}

Where $v_p$, $v_s$, and $v_k$ are the normalized pinch-off voltage, source voltage and intrinsic drain voltage respectively as defined in EKV model [2].

2.2. Drift Resistance Modeling

The modeling of the drift resistance is carried out using a bias dependent resistance, i.e. drift resistance is a function of node voltages.

2.3. Modeling of the Impact Ionization Current

The Impact Ionization current (or avalanche current) in the drift part is given by:
\[ I_{av} = (M - 1) I_{DS} \]  
Eq. (4)

Where \( I_{DS} \) is the drain-to-source current and \( M \) is called as Multiplication factor. An approximate expression is used to obtain \( M \) from impact ionization integral assuming low multiplication level.

### 2.4. Modeling of the Self-Heating Effect

A special target in this project is related to the simulation of the self-heating effect. Fig. 2 presents the equivalent sub-circuit used for the self-heating representation [4]. This already classical representation can be used for the combined DC/AC simulation of the device in some critical regimes (other than analog operation). Moreover, we have already demonstrated that this representation is suitable for further improvements of the model, in which the thermal parasitic components depend on the internal temperature of the device.

![Fig.2](a) Representation of the parasitic electro-thermal circuit for SHE simulation, (b) Frequency response of the electro-thermal circuit.

### 3. AC Compact Model

The total gate charge is the sum of gate charge associated with the intrinsic MOS and the drift region. The MOS gate charge can be expressed as:

\[ Q_G = Q_K + Q_S + Q_B \]  
Eq. (5)

Where \( Q_K, Q_S \) and \( Q_B \) are the charges related to intrinsic-drain \((V_K)\), Source and Body node respectively. These charges are obtained as a function of normalized forward current \( i_f \) and normalized reverse current \( i_r \) as given in [5] and also used in EKV model [2]. The normalized accumulation charge \( q_{Drift} \) can be expressed by using a simple approximation as:

\[ q_{Drift} = (V_G - V_{FB} - \Psi_S)C_{ox} \]  
Eq. (6)

Where \( V_G, V_{FB} \) are the gate voltage and flat band potential of drift respectively, \( \Psi_S \) is the surface potential and \( C_{ox} \) is the oxide capacitance per unit area of drift region. The total accumulation charge \( Q_{Drift} \) is calculated by integrating \( q_{Drift} \) (eq.6) over drift length. The total gate charge can be written as:

\[ Q_G = Q_K + Q_S + Q_B + Q_{Drift} \]  
Eq. (7)

### 4. Results –

This model is calibrated on the simulated and measured characteristics of VFNDM50 (a 50V device from I3T100 technology with channel length \( L=0.6\mu m \) and oxide thickness \( t_{ox}=7\text{nm} \)) provided by AMI Semiconductor. The DC calibration on VFNDM50 was performed for width
$W=40\mu m$ and Number of fingers=2. The AC calibration was performed for width $W=40\mu m$ and Number of fingers=12.

This model was also calibrated on the measured characteristics of a 40V VDMOS power device provided by Robert Bosch. The DC calibration on this device was performed for minimum sized device. The AC calibration was performed for minimum size device with large number of source cells.

4.1. Model results for DC characteristics

4.1.1. Model results for \textit{AMIS} VDMOS device

4.1.1.1. Results against numerical simulation for DC characteristics

Fig.3. Transfer characteristics for $V_D = 0.1 – 0.5 V$, $T=27^\circ C$, $W=40\mu m$, model (red) vs. simulation (black): (a) and (b) $I_D$ vs. $V_G$ in lin-lin and log-lin scales, (c) and (d) $g_m$ vs. $V_G$ in lin-lin and log-lin scales.
Fig. 4. Transfer characteristics for $V_D = 1 – 5\text{V}$, $T=27^\circ\text{C}$, $W=40\mu\text{m}$, model (red) vs. simulation (black): a) and (b) $I_D$ vs. $V_G$ in lin-lin and log-lin scales, (c) and (d) $g_m$ vs. $V_G$ in lin-lin and log-lin scales.

Fig. 5. Output characteristics for $V_G = 0.6–3\text{V}$, $T=27^\circ\text{C}$, $W=40\mu\text{m}$, model (red) vs. simulation (black): a) $I_D$ vs. $V_D$, (b) $g_{ds}$ vs. $V_D$. 

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Fig. 6. Output characteristics ($I_D$ vs. $V_D$) including impact ionization current, model (red) vs. simulation (black).

Fig. 7. Body Current ($I_B$) vs. Gate bias ($V_G$) for $V_D$=10V-40V with step of 10V, model (red) vs. simulation (black).

4.1.1.2. Results against measurements for DC characteristics
Fig. 8. Transfer characteristics for $V_D = 0.1 - 0.5V$, $T=27^\circ C$, $W=40\mu m$, model (red) vs. measurement (black): a) and (b) $I_D$ vs. $V_G$ in lin-lin and log-lin scales, (c) and (d) $g_m$ vs. $V_G$ in lin-lin and log-lin scales.

Fig. 9. Output characteristics for $V_G = 1 - 3V$, $T=27^\circ C$, $W=40\mu m$, model (red) vs. measurement (black): a) $I_D$ vs. $V_D$, (b) and (c) $g_ds$ vs. $V_D$ in lin-lin and log-lin scales.
Fig. 10. Output characteristics ($I_D$ vs. $V_D$) including self-heating effect implementation and impact ionization for $V_G = 1 – 3V$, $T=27^\circ C$, $W=40\mu m$, model (red) vs. measurement (black).

4.1.2. Model results against measurements for Robert Bosch VDMOS device
Fig. 11. Transfer characteristics for $V_D = 0.1 – 0.5V$, $T=27^\circ C$, model (red) vs. measurement (black): a) and (b) $I_D$ vs. $V_G$ in lin-lin and log-lin scales, (c) and (d) $g_m$ vs. $V_G$ in lin-lin and log-lin scales.
4.2. Model results for AC characteristics

4.2.1. Model results for AMIS VDMOS device

4.2.1.1. Results against numerical simulation for AC characteristics –

Fig. 12. Output characteristics for $V_G = 2 – 8\, \text{V}$, $T=27^\circ\text{C}$, model (red) vs. measurement (black): a) $I_D$ vs. $V_D$, (b) and (c) $g_{ds}$ vs. $V_D$ in lin-lin and log-lin scales.

Fig. 13. Gate-to-Drain Capacitance ($C_{gd}$) vs. $V_G$ for $V_D=0 – 5\, \text{V}$ (red - model and black – simulation).
Fig. 14. Gate-to-Source and Gate-to-Body Capacitance ($C_{gs} + C_{gb}$) vs. $V_G$ for $V_D=0–5V$ (red - model and black - simulation).

Fig. 15. Gate-to-Gate Capacitance ($C_{gg}$) vs. $V_G$ for $V_D=0–5V$ (red - model and black – simulation).

Fig. 16. Gate-to-Drain Capacitance ($C_{gd}$) vs. $V_D$ for $V_G=0 - 3V$ (red - model and black – simulation).
4.2.1.2. Results against measurements for AC characteristics –

(a) $V_G = 0\text{V}$

(b) $V_G = 0.5\text{V}$

(c) $V_G = 1\text{V}$

(d) $V_G = 1.5\text{V}$

(e) $V_G = 2\text{V}$

(f) $V_G = 2.5\text{V}$
Fig. 17. Gate-to-Drain Capacitance ($C_{gd}$) vs. $V_D$ for (a) $V_G=0V$, (b) $V_G=0.5V$, (c) $V_G=1V$, (d) $V_G=1.5V$, (e) $V_G=2V$, (f) $V_G=2.5V$, (g) $V_G=3V$, (h) $V_G=3.5V$ (red - model and black – measurement).
Fig. 18. Gate-to-Source and Gate-to-Body Capacitance ($C_{gs} + C_{gb}$) vs. $V_D$ for (a) $VG=0V$, (b) $VG=0.5V$, (c) $VG=1V$, (d) $VG=1.5V$, (e) $VG=2V$, (f) $VG=2.5V$, (g) $VG=3V$, (h) $VG=3.5V$ (red - model and black - measurement).
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(a) $V_D = 0V$

(b) $V_D = 1V$

(c) $V_D = 2V$

(d) $V_D = 3V$
Fig. 19. Gate-to-Drain Capacitance ($C_{gd}$) vs. $V_G$ for (a) $V_D=0V$, (b) $V_D=1V$, (c) $V_D=2V$, (d) $V_D=3V$, (e) $V_D=4V$, (f) $V_D=5V$ (red - model and black – measurement).
Fig. 20. Gate-to-Source and Gate-to-Body Capacitance ($C_{gs} + C_{gb}$) vs. $V_G$ for (a) $V_D=0V$, (b) $V_D=1V$, (c) $V_D=2V$, (d) $V_D=3V$, (e) $V_D=4V$, (f) $V_D=5V$ (red - model and black – measurement).
4.2.2. Model results against measurements for **Robert Bosch** VDMOS device
4.3. Model accuracy: achievements versus targets

According to the initial Robuspic accuracy targets, the developed model has been evaluated in terms of accuracy over all the operation regimes, and essentially in linear, quasi-linear and saturation region of operation.

The typical errors obtained for the DC and AC characteristics are presented in table 1. It is remarkable that this model is able to provide RMS errors that are typically lower than 10% over all operation regions for DC part and the maximum error obtained is close to 20%. Extremely accurate
results are obtained for $g_m$ (about 10% RMS), which demonstrate the fact that the value of the intrinsic channel mobility is physical and accurate.

Table 1. Maximum and RMS error obtained using the analytical model including Self-Heating and Impact Ionization effect

<table>
<thead>
<tr>
<th>Region</th>
<th>Parameter</th>
<th>Target</th>
<th>VDMOS Max error</th>
<th>VDMOS RMS Error</th>
</tr>
</thead>
</table>
| $I_D V_G$  
($V_D =0.1V-0.5V$) | $I_D$ | Better than 10% | 11.30 | 4.79 |
| $g_m$ | Better than 20% | 23.33 | 10.62 |
| $I_D V_D$  
(without SH* and II* effect) | $I_D$ | Better than 10% | 20.08 | 10.48 |
| $g_{ds}$ | Better than 20% | 199.16 | 99.09 |
| $I_D V_D$  
(with SH* and II* effect) | $I_D$ | Better than 10% | 18.91 | 9.79 |
| $g_{ds}$ | Better than 20% | 199.54 | 68.80 |
| $C_{gg} V_G$  
($V_D =0-5V$) | $C_{gg}$ | Better than 20% | 55.08 | 24.80 |
| $C_{gd} V_G$  
($V_D =0-5V$) | $C_{gd}$ | Better than 20% | 89.62 | 40.50 |
| $C_{gs} + C_{gb} V_G$  
($V_D =0-5V$) | $C_{gs} + C_{gb}$ | Better than 20% | 50.15 | 28.37 |

*SH- Self Heating, II- Impact Ionization.
5. Scalability of the Model against Physical Parameters

The scalability of the model against device width and temperature was performed. Scalability of the model against physical parameters device width, temperature and number of source cells was tested.

5.1. Scalability against Device Width

The scalability of the model against device width was tested on measurement data of AMIS-VFNMDM50 device. The results are as shown below.

![Fig. 24. Width Scaling: (a) \( I_D-V_G \) and \( g_m-V_G \), and (b) \( I_D-V_D \) for different widths and \( N_F=2 \) at \( T=30^\circ C \) (circles-model and solid black lines- measurement).](image)

5.2. Scalability against Temperature

The scalability of the model against temperature was tested on measurement data of AMIS-VFNMDM50 device. The results are as shown below.

![Fig. 25. Temperature scaling: (a) \( I_D-V_G \) and \( g_m-V_G \), and (b) \( I_D-V_D \) for \( W=40\mu m \) and \( N_F=2 \) (circles-model and solid black lines- measurement).](image)
Fig. 26. $R_{ON}$ with temperature for $N_f=2$ and $W=20\mu m$, $40\mu m$, $160\mu m$ and $320\mu m$ at $V_G=3.3V$ and $V_D=0.5V$ (blue - model and black - measurement).

5.3. Scalability against Number of Fingers

The scalability of $R_{Drift}$ with number of fingers was included using an empirical formula. Fig. 27 shows the behavior of $R_{ON}$ with number of fingers on AMIS-VFNDM50 and fig. 28 shows the relative $R_{ON}$ with number of fingers on BOSCH device.

Fig. 27. $R_{ON}$ with Number of fingers for $W=40\mu m$ and $W*N_f=5000\mu m$ at $V_G=3.3V$ and $V_D=0.5V$ (circles- model and black lines- measurement).
6. Temperature Dependence of Parameters

Following intrinsic MOS (EKV) parameters are affected by temperature [3]:

\[ VTO(T) = VTO - TCV(T - T_{\text{nom}}) \]

\[ KP(T) = KP \left( \frac{T}{T_{\text{nom}}} \right)^{BEX} \]

\[ UCRIT(T) = UCRIT \left( \frac{T}{T_{\text{nom}}} \right)^{BEX} \]

\[ PHI(T) = PHI \left( \frac{T}{T_{\text{nom}}} \right) - 3V' \ln \left( \frac{T}{T_{\text{nom}}} \right) - E_g(T_{\text{nom}}) \left( \frac{T}{T_{\text{nom}}} \right) + E_g(T) \]
References:


