Solid State Devices

4B6

Lecture 6 – TFT technology

Daping Chu

Lent 2016

Macroelectronics for large areas

Larger size
Faster speed
Higher current

EPSON 40in OLED TV, reported by NHK Oct 2004
Macroelectronics for large areas

Traditional microelectronics:
Silicon wafer (12in) based
MOSFETs

Objectives:
- Smaller geometry
- Higher speed
- Higher device density
  DRAM, Flash, FRAM, ...
- Lower power consumption

Large area macroelectronics:
Alternative substrate (3m) based
Thin-film transistors (TFTs)

Objectives:
- Larger area
- Higher speed and higher current
- Higher resolution
  VGA (640x480), ..., to
  UXGA (1600x1200, 4:3), ...
  WUXGA (1920x1200, 16:9), ...
- Lower power consumption

Generations of glass panel for LCD panels.

Oct 2009, Sharp Gen-10 (2850x3050mm²) production. Fab costs US$4.25b.
Macroelectronics for large areas

Full HDTV 42" 1080p (1920x1080 pixels) ➔ >31m TFTs on a Gen-10 substrate

Automated optical inspection tool for LCD panels

• Two faulty pixels ➔ 2nd Grade panel.
• Strong requirement on the production yield of the TFTs for uniformity and reliability.
TFT history

J. Lilienfeld    O. Heil
TFT Invention 1933-34

W.E. Spear    P.G. LeComber
a-Si TFT 1970's

Organic TFT 1990's

1960's
First TFT (CdS)
P.K. Weimer (RCA Labs)

1980's
Poly-Si TFT

2000's
Transparent metal oxide TFT

Silicon MOSFET vs Silicon TFT

Silicon MOSFET

Silicon wafer

Doped channel.
Potential profile fixed by biases.

SiO₂

Silicon TFT

a-Si or poly-Si

Glass substrate

Undoped channel.
Floating body effect at transient.
(speed can be limited by this, especially for long channel devices.)
Alumino-silicate thin sheet glass prepared by ion-exchange process for high strength and reliability.

Materials

Crystalline SiO$_2$

Amorphous SiO$_2$

Materials

Amorphous  Polycrystalline  Crystalline

nm  µm  mm

amorphous  nanocryst.  polycrystalline  single crystal
Materials

Traditional method to grow poly-Si films:

Low Pressure Chemical Vapour Deposition (LPCVD), SiH$_4$, 625°C

\[
\text{SiH}_4 \xleftrightarrow{625\, ^\circ\text{C}} \text{Si} + 2\text{H}_2
\]

Low pressure: 0.5-1 torr;
Material too defective, electron mobility < 5 cm$^2$/Vs

Low pressure: 0.01-0.04 torr;
Improved material, electron mobility 15-30 cm$^2$/Vs
(Meakin et al., GEC, 1986; Miyasaka et al. Epson, 1991)

Materials

Normal TEM
LPCVD, Deposition Pressure 0.5torr.
Materials

Cross section TEM
LPCVD, Deposition Pressure 0.5torr.

Cross section TEM
LPCVD, Deposition Pressure 0.04torr.

Materials

LPCVD, Deposition Pressure 0.5torr.
Significant lattice distortion.

LPCVD, Deposition Pressure 0.04torr.
Minimum lattice distortion.
Materials

Correlation between microtwinning and lattice parameter distortion: (Meakin et al., GEC, 1986)

LPCVD poly-Si deposited at normal pressure (0.5 torr):
- many microtwins;
- large lattice parameter distortion; (~3%);
- Poor TFT performance.

LPCVD poly-Si deposited at reduced pressure (<0.04 torr):
- fewer microtwins
- no lattice parameter distortion;
- improved TFT performance.

Materials

Coherent twins in silicon ribbon

Coherent twins are electrically inactive.
Coherent boundaries: 1-2 and 1-3
Incoherent boundary: 3-2

When 3 twins are randomly oriented incoherent boundaries may occur.

Along the 3-2 interface TWO bonds on 3 face ONE bond on 2, resulting in:
• dangling bonds;
• lattice parameter distortion.

Present method to fabricate poly-Si film:
Amorphous silicon deposition followed by re-crystallisation

Deposition methods:
• Plasma Enhanced Chemical Vapour Deposition from SiH₄
• Low Pressure Chemical Vapour Deposition from Si₂H₆ 450°C

Crystallisation methods:
• Thermal nucleation and growth (SSC);
• Melting, nucleation and growth (RTA, ELA);
• Metal induced lateral growth (MILC).

Objective:
Minimise structural defects.
Materials

Solid state crystallisation (SSC)
- Small size grains but more uniform.
- Low fabrication cost.
- Slow and high temperature, not really suitable for glass substrates.

Rapid thermal annealing (RTA)
- Medium size grains but not very uniform.
- Medium fabrication cost.
- Decrease in yield for increase of heating area.

Excimer laser annealing (ELA)
- Large size grains but not uniform.
- High fabrication cost.
- Decrease in yield for increase of scanning size.

Materials

Poly-Si film produced by thermal recrystallisation (SSC) at 600°C for 20hrs

Under subsequent high temperature treatment, (e.g. oxidation at 950°C)
planar defects such as microtwins or stacking faults anneal out.
This material is suitable for high temperature TFTs on quartz, as used in LCD projectors.
Materials

Laser re-crystallisation:

Sharp grain boundaries;
Reduced intra-grain defect concentration.

Materials

Continuous-grain silicon technology (Ohtani, et al., Sharp, 1998)

<table>
<thead>
<tr>
<th>Channel Type</th>
<th>Vth [V] (Vd=5V)</th>
<th>S-value [mV/dec] (Vd=1V)</th>
<th>μFE [cm²/Vs] (Vd=1V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>N</td>
<td>0.12</td>
<td>74.4</td>
<td>317.7</td>
</tr>
<tr>
<td>P</td>
<td>-1.00</td>
<td>76.1</td>
<td>140.6</td>
</tr>
</tbody>
</table>
Materials

Metal induced lateral crystallisation (MILC)
- Ni or Pd deposited on a-Si film and selective crystallisation.
- Low fabrication cost.
- Low temperature process (450-500°C).

Fabrication process – a-Si TFT
Localised density of states in the band gap

The density of localised states, N(E), plotted against the energy Ec−E for a number of a-Si samples produced using the ‘glow discharge’ (or PECVD) technique in SiH₄ gas. T₀ is substrate temperature during deposition.

There are continuous localised states within the band gap for BOTH a-Si and poly-Si films (due to defects, impurities, unsatisfied bonds, grain boundary states, interface states, etc), which can be empirically fitted by:

\[ N(E) = N_{ac} e^{\frac{E-E_C}{E_{ac}}} + N_{ad} e^{\frac{E-E_C}{E_{ad}}} + N_{ds} e^{\frac{E-E_{f}}{E_{ds}}} + N_{dd} e^{\frac{E-E_{f}}{E_{dd}}} \]

**Poly-Si TFT**

Grain boundaries, interfaces, defects, ...
⇒ low mobility
large \( \Delta V_{TH} \)
transient response ...

…
Charge carrier transport is considerably affected by grain boundary (GB).

Different GB number → Different TFT performance!

Statistical fluctuation for short channel TFTs made by using large size grains.
Poly-Si TFT

Channel partially depleted (PD)
Channel depth < Film thickness
Only front interface scattering

Channel fully depleted (FD)
Channel depth = Film thickness
Both front and back interface scattering

Poly-Si TFT

Front interface states

Partially depleted channel
Poly-Si TFT

Single grain TFT using laser annealing with a pre-patterned filter for seeding arrangement. Very good registration.

L=W=2μm, with 250nm thick silicon layer and a 120-nm gate insulator.

Rana, et al., Delft/Epson, 2005
Poly-Si TFT

**SUFTLA®**
(Surface Free Technology by Laser Ablation / Annealing)
EPSON

Standard low-temperature poly-Si TFT with high performance and fine structure

Flexible substrate

Excimer Laser

Transfer of single grain TFTs possible.

---

Poly-Si TFT

**SUFTLA®**
(Surface Free Technology by Laser Ablation / Annealing)
1st Transfer Step

Temporary substrate

Temporary adhesive (Water soluble)

Original substrate (Glass)

Sacrificial a-Si layer

Excimer laser
Poly-Si TFT

SUFTLA®
(Surface Free Technology by Laser Ablation / Annealing)
2nd Transfer Step

Temporary substrate
Temporary adhesive (Water soluble)
Permanent adhesive (Non water soluble)
Final substrate (Plastic substrate)

Poly-Si TFT

SUFTLA® + E-ink

EPSON (Jun 2006)
A6 (7") (397dpi)
Silicon MOSFET vs Silicon TFT

<table>
<thead>
<tr>
<th></th>
<th>Si MOSFET</th>
<th>a-Si:H TFT</th>
<th>Poly-Si TFT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Design Rule</td>
<td>&lt; 45 nm</td>
<td>10-20 μm</td>
<td>5-10 μm</td>
</tr>
<tr>
<td>Mobility</td>
<td>1500 cm²/Vs</td>
<td>1 cm²/Vs</td>
<td>100 cm²/Vs</td>
</tr>
<tr>
<td>Device Type</td>
<td>n- &amp; p-type</td>
<td>n-type</td>
<td>n- &amp; p-type</td>
</tr>
<tr>
<td>Substrate</td>
<td>Si wafer</td>
<td>Glass</td>
<td>Glass / Quartz</td>
</tr>
<tr>
<td>Process Temperature</td>
<td>1000 °C</td>
<td>300 °C</td>
<td>450 - 700 °C</td>
</tr>
<tr>
<td>Process Technology</td>
<td>Photolithography</td>
<td>CVD deposition Photolithography</td>
<td>CVD deposition Crystallisation Photolithography</td>
</tr>
<tr>
<td>Interconnects</td>
<td>Multi-metal layers</td>
<td>One metal layer</td>
<td>&gt;1 Metal layers</td>
</tr>
<tr>
<td>Reliability</td>
<td>High</td>
<td>Low</td>
<td>Medium</td>
</tr>
<tr>
<td>Uniformity</td>
<td>High</td>
<td>High</td>
<td>Medium</td>
</tr>
<tr>
<td>Cost/Area</td>
<td>High</td>
<td>Low</td>
<td>Medium</td>
</tr>
</tbody>
</table>

Silicon MOSFETs:
- High speed and high density for CPU (GHz), Memory (Gb) and alike,
- But area is limited by wafer size.

a-Si TFTs:
- Active matrix backplane for LCD TVs and alike,
- Speed and current limited mainly by channel mobility,
- Life time limited by material instability,
- Uniform TFT performance over large area,
- But transistors suffer from degradation in performance due to bias stress.

High temperature poly-Si (HTPS) TFTs:
- Active matrix backplane for LCD projectors and alike,
- Higher speed and current than a-Si TFTs,
- Better life time and much less bias stress degradation,
- But area and costs are limited by high temperature substrates such as quartz.

Low temperature poly-Si (LTPS) TFTs:
- Active matrix backplane for OLED and alike,
- Much higher speed and current and suitable for most applications,
- But production yield is limited by transistor uniformity over large area.
Poly-Si TFT System-on-Panel

All parts can be made by using poly-Si TFTs.