Solid State Devices

4B6

Lecture 9/10 – MRAM

Daping Chu

Giant Magneto Resistance

Introduction

Giant Magneto Resistance (GMR)
– Basic structure and GMR effect
– Definition of magneto-resistance MR%
– Performance of a GMR superlattice
  Dependence of exchange coupling on spacer thickness
– Comparison of configurations
  Current-perpendicular-to-plan (CPP)
  Current-in-plan (CIP)
Giant Magneto Resistance

GMR and basic structures

Magnoeto-resistance MR%:

\[
MR\% = \frac{\Delta R}{R} (\%) = \frac{\Delta \rho}{\rho} (\%)
\]

GMR: \ \Delta R/R as high as 50% (Rm Temp)
Normal MR: typical materials << 5%

Three essential elements to get the GMR effect
Two ferromagnetic (FM) metal layers
One non-magnetic layer
Giant Magneto Resistance

Two ferromagnetic metal layers

Ferromagnetic + Metallic
– Electrons in the metal conduction band ⇒ Conduction
– Spin of the electrons ⇒ Magnetisation
– Difference of spin-related electron populations ⇒ GMR
  (∵ different scattering cross-sections between ↑↑ and ↑↓)

Giant Magneto Resistance

One non-magnetic layer

The Spacer
– Separation between the two FM layers ⇒ Strength of exchange coupling
– Conductive spacer ⇒ Spin Valve, Pseudo-Spin Valve
– Insulating spacer ⇒ Magnetic Tunnel Junction
Giant Magneto Resistance

MR definition and a GMR device

Definition of MR%:

\[ \text{MR} \% = \left( \frac{R(\text{AP}) - R(\text{P})}{R(\text{P})} \right) \times 100 = \frac{\Delta R}{R} \% = \left( \frac{\Delta \rho}{\rho} \right) \%
\]

A GMR device:
(superlattice)

\[ [\text{Co}(11\text{Å})/\text{Cu}(9\text{Å})] \times 100 \]

Giant Magneto Resistance

Magnetic coupling

For two magnetic moments, \( \mathbf{M}_i \) and \( \mathbf{M}_j \), at site \( i \) and \( j \),

\[ E_{ij} = -J_{ij} \mathbf{M}_i \cdot \mathbf{M}_j \]

the energy of magnetic interaction between them is:

where \( J_{ij} \) is the exchange coupling between these two sites.

\( J_{ij} > 0 \) ➔ Ground state is Ferromagnetic (FM)
\( J_{ij} < 0 \) ➔ Ground state is Anti-Ferromagnetic (AFM)
Giant Magneto Resistance

Spacer thickness effect

Exchange coupling depending on spacer thickness:
– RKKY type exchange interaction

\[ J_{RKKY} \propto \frac{\cos(2k_F r)}{(2k_F r)^3} \]

Giant Magneto Resistance

CPP vs CIP

CPP

CIP

[Co(6nm)/Ag(6nm)]

60 at 4.2K

[Co(6nm)/Ag(6nm)] at 4.2K
Spin valve

Introduction

Spin valve (SV)
- Basic structure and pinning
- Different pinning approaches and performances
- Spin valve MRAM arrays
  1T or 1D?
    How to write
- An example
  1D SV cell

Spin valve

Basic structure

Direction of magnetization: fixed (pinned) in one FM layer;
free to switch in the other one.
Spacer is conductive.

Different levels of MR when parallel/antiparallel \( \Rightarrow 0^\circ/1^\circ \)
**Spin valve**

**Pinning**

Fixed direction of magnetization through a strong magnetic coupling between the pinning layer and pinned layer.
Spin valve

Symmetric pinning

Antiferromagnetic coupling pinning
Spin valve

CIP spin valve GMR head

IBM CIP GMR head
(since 1997)
Density limit:
200 Gb/in²

3 GMR nanosliders on a US quarter.

Two written tracks made by IBM:
Upper track density 35 Gb/in²
Lower track density 23 Gb/in²

Spin valve

CPP spin valve GMR head

Hitach CPP GMR head
(Oct 2007)
Density expected:
500 Gb/in² to 1 Tb/in²

By 2011:   1 Tb HDD for laptop
4 Tb HDD for desktop
Spin valve

1D/1R and 1T/1R arrays

1D/1R

1T/1R

Read is easy, how to write?

The technique to avoid the mis-write due to the half-selection:
Send a pulse to word line, switching the cells half way;
Send another pulse to bit line to complete the switch;
Only the combined field is strong enough to switch the free layer of the selected cell.
Spin valve

Coincident field selection

Coincident field selection and switching threshold (asteroid) curve for writing a magnetic element of an MRAM. The ellipses show the direction of the shape anisotropy of the free magnetic layers of the bits; the arrows inside the ellipses indicate the orientations of the free-layer magnetization.

Spin valve

A 1D/1R SV cell
Pseudo spin valve

Introduction

Pseudo spin valve (PSV)
- Basic structure and operation method
- Performance of a PSV unit
  Effect of word line pulse width

Pseudo spin valve

Basic structure

Concept: Direction of magnetization can be switched in both FM layers, but at different strength of the external field \( \Rightarrow \) "soft" and "hard" layers.

Spacer is conductive.

The hard layer is used for information storage \( \Rightarrow \) "0" / "1"
Pseudo spin valve

Operation of a PSV unit

Read-out is achieved by detecting the MR changes during switching the soft layer while the hard layer remains unchanged.

Storing four states (2 bits) per cell is possible.

Pseudo spin valve

Effect of Word line pulse width
Magnetic tunnelling junction

Introduction

Magnetic tunnelling junction (MTJ)
- Basic structure
- MTJ cell and array
- Performance of an MTJ unit
  - Temperature dependence
  - Effect of the MTJ spacer thickness
  - Different aspect ratios of the junction area

Magnetic tunnelling junction

Basic structure

• Similar arrangement as a SV in CPP configuration, but the spacer is made of insulator and acts as a tunnelling barrier.

• Isolation transistor:
  - READ: ON
  - WRITE: OFF

• Motorola’s flux concentrating cladding layer to reduce the WRITE power consumption.
Magnetic tunnelling junction

MTJ cell and array

Operation of an MTJ unit

Read operation similar to PSV. 2bit/cell is also possible.

Fig. 3. Resistance versus applied magnetic field for a Co/Al₂O₃/Ni₉₀Fe₂₀ junction at room temperature and 77 K, showing JMR values of 20.2 and 27.1%, respectively. The barrier is formed by oxidation of a 8 Å Al layer (after Ref. [23]).
Magnetic tunnelling junction

Some issues – Temperature dependence

![Graph showing temperature dependence](image)

Magnetic tunnelling junction

Some issues – Effect of spacer thickness

![Graph showing effect of spacer thickness](image)

Fig. 4. Juntion magnetoresistance plotted as a function of the thickness of the Al metal overlayer used to form the Al₂O₃ barrier in (a) Co/Al₂O₃/Ni₈₀Fe₂₀ and (b) Co/Al₂O₃/Co₈₀Fe₂₀ tunnel junctions (after Ref. [14]).
Magnetic tunnelling junction

Some issues – Aspect ratio of junction area

![Graph showing magnetoresistance curves for different aspect ratios.](image)

Fig. 6. Magnetoresistance curves at room temperature for a series of junctions with an identical area (256 $\mu m^2$) but having different aspect ratios (after Ref. [1]).

MRAM summary

Some relevant topics

Comments and challenges

Motorola MRAM demonstrator

Performance comparison of some NVMs
**MRAM summary**

**Comments and challenges for MRAM**

CPP vs CIP ➔ Vertical structure good for scale down to small size.
SV vs MTJ ➔ Higher resistance for faster speed.

Metal contamination ➔ Ta layers both sides.
Metal inter diffusion within the sandwich structure at the temperature of Al/Cu interconnect process.
Power consumption of WRITE operation.
Reliable magnetic switching.
Uniformity of the very thin spacer (2-3nm) for 8-12 in wafers.

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**MRAM summary**

A deposition system for MTJ

A system installed at IBM suitable for fabricating MTJs on 200-mm or 300-mm diameter wafers, showing part of central robotic chamber in the foreground, two five-source modules in the background (left and right), and a cleaning (etching) module at the lower left.

*Canon ANELVA*
MRAM summary

IBM CMOS MRAM: 1Kb FET twin cell

The first CMOS MRAM array fabricated at IBM — a 1Kb array containing FET twin cells fabricated in a 0.25 μm technology: Time traces of input and output signals during read access operation and SEM cross section of twin-cell structure.

IBM, VLSI TSA TECH, 2005

MRAM summary

Motorola 256Kb MRAM

Feb. 2001 / June 2002

Features:
- 256 kB / 1 MB
- on 200 mm Si wafer
- 2x128k blocks / 16x64k blocks
- 1MTJ/1T
- reference cells
- five-layer metallization / magnetic cladding
- chip size: 3.9x3.2 mm² (40% for memory)
- write current: 11 mA / 3 mA

Wafer uniformity for 0.6x1.2 μm² cells:
- TMR = 44.6 ± 0.7 %
- $R_A = 9.97 \pm 0.43$ kΩμm²

from H. Brückl, Oct 2003
MRAM summary

Motorola 1Mb MRAM

1T/1MTJ with Cu interconnects

Motorola, VLSI 2002

MRAM summary

Everspin (Motorola) embedded process

Everspin 2009
MRAM summary

Increasing density of prototype MRAM chips (not to scale)

(a) IBM 1mmx1.5mm 1Kb chip with a 5.4μm² twin cell in 0.25μm technology with approximately 3-10ns access time; ©2000 IEEE.
(b) Motorola 3.9mmx3.2mm 256Kb chip with 7.1μm² cell in 0.6μm technology with 35ns access time. ©2001 IEEE;
(c) Motorola 4.25mmx5.89mm 1Mb chip with 7.1μm² cell in 0.6μm technology with 50ns access time; ©2002 IEEE.
(d) Motorola 4.5mmx6.3mm 4Mb chip with 1.55μm² cell in 180nm technology with 25ns access time; ©2003 IEEE.
(e) IBM 7.9mmx10mm 16Mb chip with 1.42μm² cell in 180nm technology with 30ns access time; ©2004 IEEE.

… … 32Mb, 64Mb and 128Mb (NEC & Toshiba), 512Mb (IBM?)

Status of MRAM development

<table>
<thead>
<tr>
<th>Update: Jan'05</th>
<th>Toshiba / NEC</th>
<th>TSMC</th>
<th>Sony</th>
<th>Samsung</th>
<th>IBM/IFX</th>
<th>Renesas</th>
<th>Motorola</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology generation</td>
<td>0.13 μm</td>
<td>0.18 μm</td>
<td>0.18 μm</td>
<td>0.24 μm</td>
<td>0.18 μm</td>
<td>0.13 μm</td>
<td>0.18 μm</td>
</tr>
<tr>
<td>Demonstrator density</td>
<td>1 Mbit</td>
<td>1 Kbit</td>
<td>1 Mbit</td>
<td>Only cells</td>
<td>16 Mbit</td>
<td>1 Mbit</td>
<td>4 Mbit</td>
</tr>
<tr>
<td>MRAM type</td>
<td>Cross Point</td>
<td>1T2UMTJ ExtVia</td>
<td>Saturn shaped MTJ</td>
<td>MTJ + SAF</td>
<td>Toggling MRAM</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operation Voltage</td>
<td>1.5 V</td>
<td>1.8 V</td>
<td>1.1 V</td>
<td>1.8V (internal)</td>
<td>1.2 V</td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td>Access time</td>
<td>250 nsec</td>
<td>40 nsec</td>
<td>NA</td>
<td>30 nsec</td>
<td>5-10 nsec</td>
<td>25-35nsec</td>
<td></td>
</tr>
<tr>
<td>Write current</td>
<td>4 mA</td>
<td>4.5 mA</td>
<td>NA</td>
<td>&gt; 3mA</td>
<td>NA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cell size (1T1C)</td>
<td>NA</td>
<td>1.06 μm²</td>
<td>2.07 μm²</td>
<td>1.42 μm²</td>
<td>0.81 μm²</td>
<td>0.54 μm²</td>
<td></td>
</tr>
<tr>
<td>Comments</td>
<td>Scalable to 6 F²</td>
<td>-</td>
<td>-</td>
<td>3 masks</td>
<td>-</td>
<td>&quot;product&quot;</td>
<td></td>
</tr>
<tr>
<td>Source</td>
<td>IEDM ’04</td>
<td>IEDM ’04</td>
<td>VLSI ’04</td>
<td>VLSI’04 / IEDM’03</td>
<td>VLSI ’04</td>
<td>IEDM ’04/ VLSI ’04</td>
<td>IEDM’03</td>
</tr>
</tbody>
</table>

D Wouters, IMEC
## NVM comparison and reflection

<table>
<thead>
<tr>
<th>Parameter</th>
<th>DRAM</th>
<th>SRAM</th>
<th>NOR Flash</th>
<th>NAND Flash</th>
<th>FeRAM</th>
<th>MRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Read cycles</td>
<td>&gt; $10^{15}$</td>
<td>&gt; $10^{15}$</td>
<td>&gt; $10^{15}$</td>
<td>&gt; $10^{15}$</td>
<td>$10^{15}$-$10^{15}$</td>
<td>&gt; $10^{15}$</td>
</tr>
<tr>
<td>Write cycles</td>
<td>&gt; $10^{15}$</td>
<td>&gt; $10^{15}$</td>
<td>$10^6$-$10^5$</td>
<td>$10^6$</td>
<td>10</td>
<td>&gt; $10^{15}$</td>
</tr>
<tr>
<td>Write voltage (V)</td>
<td>2.5-5</td>
<td>3.3-5</td>
<td>10/10</td>
<td>18</td>
<td>0.8-5</td>
<td>0.8-5</td>
</tr>
<tr>
<td>Cell write time (ns)</td>
<td>10-100</td>
<td>1-50</td>
<td>$6 \times 10^3$</td>
<td>$2 \times 10^3$</td>
<td>10-50</td>
<td>10</td>
</tr>
<tr>
<td>Write energy (pJ)</td>
<td>Few $10^{-2}$</td>
<td>9000</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Random access time (ns)</td>
<td>40-70</td>
<td>6-70</td>
<td>150</td>
<td>~10000</td>
<td>40-70</td>
<td>40-70</td>
</tr>
<tr>
<td>Cell size ($F^3$)</td>
<td>8</td>
<td>~100</td>
<td>12</td>
<td>4.6</td>
<td>9-13</td>
<td>6-10</td>
</tr>
<tr>
<td>Retention (years)</td>
<td>None</td>
<td>None</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>Scaling issues</td>
<td>Charge</td>
<td>Tunnel oxide → read current → access time</td>
<td>Erase voltage tunnel oxide scaling, SiGe</td>
<td>3D + material texture</td>
<td>Switching field increase with scaling and uniformity few kb/1 Mb by 2002(?)</td>
<td></td>
</tr>
<tr>
<td>Status/forecast</td>
<td>256 Mb/1 Gb</td>
<td>4-16 Mb</td>
<td>32 Mb/128 Mb</td>
<td>256 Mb/1 Gb</td>
<td>1 Mb/4 Mb</td>
<td>Envisaged; embedded (SOC) and mass storage</td>
</tr>
<tr>
<td>Applications</td>
<td>PC memory</td>
<td>Cache memory</td>
<td>Program code &amp; data</td>
<td>Data files (camera, MP3)</td>
<td>Contactless smartcard</td>
<td></td>
</tr>
</tbody>
</table>

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## NVM comparison and reflection

<table>
<thead>
<tr>
<th>Technology</th>
<th>Memory Mechanism</th>
<th>Fundamental Particle</th>
<th>Particles in a 20nm Cell</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRAM</td>
<td>Electrons stored on a capacitor</td>
<td>electron</td>
<td>~100,000</td>
<td>25fF*0.6V</td>
</tr>
<tr>
<td>NAND</td>
<td>Electrons stored on a floating gate</td>
<td>electron</td>
<td>~50/state</td>
<td></td>
</tr>
<tr>
<td>Phase Change</td>
<td>Crystalline state Amorphous State</td>
<td>Atomic Bond, Bond Angle Bond configuration Ge octahedral/tetragonal coordination</td>
<td>~5E4</td>
<td></td>
</tr>
<tr>
<td>RRAM</td>
<td>Conducting Filament Broken Filament</td>
<td>Cu ion or oxygen vacancy</td>
<td>few hundred</td>
<td>Constant with scaling</td>
</tr>
<tr>
<td>STRAM</td>
<td>Correlated electron spins (Bohr Magnetons)</td>
<td>Bohr Magneton</td>
<td>~40,000</td>
<td>20 nm diameter X 2 nm thick free layer 2 μm/Co, Fe atom</td>
</tr>
<tr>
<td>Ferro Electric DRAM</td>
<td>Correlated dipoles</td>
<td>Ferroelectric Dipole</td>
<td>~700,000</td>
<td>Capacitor matched to DRAM at 20μC/cm²</td>
</tr>
</tbody>
</table>

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\[ K \text{ Prall, et al, Micron, 2013} \]
## NVM comparison and reflection

<table>
<thead>
<tr>
<th>Technology</th>
<th>State Change</th>
<th>Barrier between states</th>
<th>Method of modifying barrier</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRAM</td>
<td>Electrons stored in a dielectric</td>
<td>Energy required for electrons to leak through p-n junction of MOS transistor</td>
<td>Turning transistor on/off</td>
</tr>
<tr>
<td>NAND</td>
<td>Electrons stored in the floating gate</td>
<td>Energy required to tunnel through tunnel oxide barrier/IPD</td>
<td>Electric Field Induced Fowler-Nordheim Tunneling</td>
</tr>
<tr>
<td>Ferroelectric</td>
<td>Energetically Bi-stable states Ferroelectric domain polarity</td>
<td>Energy required to switch polarity</td>
<td>Electric field overcoming ferroelectric polarity</td>
</tr>
<tr>
<td>Phase Change</td>
<td>Energetically Bi-stable states Crystallinity of the material</td>
<td>Energy required to switch crystallinity</td>
<td>Thermal Energy</td>
</tr>
<tr>
<td>RRAM</td>
<td>Ions stored in a dielectric</td>
<td>Energy required to ionize and migrate metal or oxygen ions</td>
<td>Electric field driven ionic conduction</td>
</tr>
<tr>
<td>STTAM</td>
<td>Energetically Bi-stable states Magnetic Anisotropy of free layers</td>
<td>Energy required to switch polarity</td>
<td>Spin Torque</td>
</tr>
</tbody>
</table>

*K Prall, et al, Micron, 2013*

## NVM comparison and reflection

<table>
<thead>
<tr>
<th>Current or Field Based</th>
<th>Technology</th>
<th>Typical Input Energy 20nm cell</th>
<th>Input Energy 20nm cell (J)</th>
<th>Energy Efficiency of Energy Retained/Energy Input</th>
<th>How is Energy Corresponding to Retention Loss Calculated</th>
<th>Primary Write State Loss Mechanism</th>
</tr>
</thead>
<tbody>
<tr>
<td>Field</td>
<td>DRAM</td>
<td>E=1/2 CV²</td>
<td>1.80E-14</td>
<td>~1</td>
<td>Zero Loss</td>
<td>Relaxation, Dielectric Leakage</td>
</tr>
<tr>
<td>Field</td>
<td>NAND</td>
<td>E=1/2 CV²</td>
<td>1.09E-16</td>
<td>~1</td>
<td>Zero Loss</td>
<td>Electrons trapped outside of floating gate</td>
</tr>
<tr>
<td>Field</td>
<td>Ferroelectric</td>
<td>Integrate 90X32 25 μf/cm², 3.5 μm capacitance</td>
<td>3.00E-13</td>
<td>~0.8-1</td>
<td>~0.8-1</td>
<td>Only-edge dipoles contain a usable signal, Center dipoles compensated, Final or a spin-polarized state</td>
</tr>
<tr>
<td>Current</td>
<td>NOR</td>
<td>E=1/2 CV²</td>
<td>~1E-6</td>
<td>~1E-6</td>
<td>E=1/2 CV²</td>
<td>Very few lucky electrons injected on the floating gate</td>
</tr>
<tr>
<td>Current</td>
<td>Phase Change</td>
<td>E=1/2 CV²</td>
<td>~4.4E-5/1.4E-6</td>
<td>Thermal energy loss outside of chalcogenide</td>
<td>Thermal energy loss outside of chalcogenide</td>
<td></td>
</tr>
<tr>
<td>Current</td>
<td>RRAM</td>
<td>E=1/2 CV²</td>
<td>~2E-3/1.2E-4</td>
<td>Activation barrier for charged vacancy diffusion (0.5eV in HfO)</td>
<td>Thermal energy loss of parasitic current</td>
<td></td>
</tr>
<tr>
<td>Current</td>
<td>STTAM</td>
<td>E=1/2 CV²</td>
<td>~1.5E-6</td>
<td>60KJ Input Energy</td>
<td>Spin-related thermal agitation tunneling efficiency stochastic switching</td>
<td></td>
</tr>
</tbody>
</table>

*K Prall, et al, Micron, 2013*
# NVM comparison and reflection

<table>
<thead>
<tr>
<th>Technology</th>
<th>Demonstrated Scalability</th>
<th>Picture</th>
<th>Technology</th>
<th>Demonstrated Scalability</th>
<th>Picture</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRAM</td>
<td>&lt;20nm</td>
<td></td>
<td>Phase Change</td>
<td>~1nm</td>
<td></td>
</tr>
</tbody>
</table>
