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Graphene and Related Materials for Resistive Random Access Memories

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Graphene and related materials (GRMs) are promising candidates for the fabrication of resistive random access memories (RRAMs). Here, this emerging field is analyzed, classified, and evaluated, and the performance of a number of RRAM prototypes using GRMs is summarized. Graphene oxide, amorphous carbon films, transition metal dichalcogenides, hexagonal boron nitride and black phosphorous can be used as resistive switching media, in which the switching can be governed either by the migration of intrinsic species or penetration of metallic ions from adjacent layers. Graphene can be used as an electrode to provide flexibility and transparency, as well as an interface layer between the electrode and dielectric to block atomic diffusion, reduce power consumption, suppress surface effects, limit the number of conductive filaments in the dielectric, and improve device integration. GRM-based RRAMs fit some non-volatile memory technological requirements, such as low operating voltages (<1V) and switching times (<10 ns), but others, like retention >10 years, endurance >10^9 cycles and power consumption ≈10 pJ per transition still remain a challenge. More technology-oriented studies including reliability and variability analyses may lead to the development of GRMs-based RRAMs with realistic possibilities of commercialization.

1. Introduction

The technology-driven development during the past half-century has been possible thanks to the creation of new electronic devices (computers, smart phones, vehicles, medical equipment), which allow for the performance of multiple complex operations (calculations, interpolations, statistics), leading to the appearance of new services (email, global positioning system (GPS), data mining) that create new jobs.[1] Non-volatile memories (NVMs) are essential elements in most modern electronic devices and integrated circuits, as they allow storing enormous amounts of data (5.62×10^{10} bits cm^{-2})[2] in a fast (<ns bit^{-1})[3] and cheap (≈0.019 \$ GB^{-1})[4] way. For this reason, it is estimated that the memory market reached 47 billion USD in 2016.[5] To date, the most used NVM device is the NAND Flash.[6] It stores one bit of information in a capacitor (integrated in the floating gate of a field-effect transistor, FET).[6] The charge/discharge of the capacitor can be used to simulate the ones/zeros of the binary code, therefore storing information. Over the past 25 years technological advances have been linked to the scaling down of the NAND Flash memory, a process that improved its size (from 2 µm node in 1980 to 7 nm in 2015),[7] switching speed (from 1MB s^{-1} in 1985 to 10GB s^{-1} in 2012)[8] and cost (from 437,500 \$ GB^{-1} in 1980 to 0.019 \$ GB^{-1} in 2016).[4] As the size approaches the nanometer range, leakage currents in the capacitor become prohibitive, leading to severe information loss.[9,10] Therefore, in order to continue the growth of information storage, new devices using non-capacitive working principles need to be developed.

According to the International Technology Roadmap for Semiconductors (ITRS),[2] the performance requirements for any NVM technology are (see **Table 1**): i) low operating voltages (<1V); ii) low power consumption (≈10 pJ per state transition); iii) high operation speed (<10 ns per transition); iv) high endurance >10^9 cycles (this is defined as the number of times a NVM can be switched on/off before one of the states becomes irreversible);[2] v) long state retention time >10 years (>3×10^8 s; this is defined as the time before the state is lost, i.e. a state change without the application of any electrical stress);[2] vi) small size below 600 nm^2 (this refers to the cell that stores 1 bit of information, not the whole NVM); vii) good integration, with a capacity density larger than 10^{11} bits cm^{-2}; and viii) simple structure, which usually brings associated low fabrication costs. Several new memory concepts are being developed to achieve these targets,[1,2] including dynamic RAM (DRAM),[11,12] ferroelectric RAM (FRAM),[13,14] phase change RAM (PCRAM),[15,16] magnetoresistive RAM (MRAM),[17,18] resistive RAM (RRAM),[19–22] carbon nanotube (CNT) RAM,[23,24] spin transfer torque magnetic RAM (STTM-RAM),[25,26]

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molecular memories,[27,28] and Mott memories.[29,30] A comparative review of the different technologies being considered for future information storage can be found in Ref. [1]. Until now RRAMs have shown the most advanced performance (see Table 1).[2,31–33]

The RRAM is a simple and industry-compatible structure formed by a matrix of metal/insulator/metal (MIM) junctions,[34] in which the sandwiched dielectric enables reversible electrical resistance changes (see **Figure 1**). This phenomenon, called resistive switching (RS),[34] can be used to induce two logic states: the high resistance state (HRS) and the low resistance state (LRS).[35] Cyclic transitions between these two states can also be used to simulate the ones and zeros of binary code, without need for a capacitor, making the storage of digital information possible.[36] Before stable cycling between HRS and LRS can be achieved (e.g., 50 electrical pulses applied to a MIM cell produce 50 state changes without resistance mismatch), most RRAMs require a one-time activation process called forming.[34] This is defined as the first generation of a reversible dielectric breakdown (BD) in the insulator.[2] The RS phenomenon can be classified as: i) unipolar/bipolar if the electrical stresses that produce the state change are of the same/opposed polarity;[37] or ii) local/distributed if the atomic rearrangements that produce the state change take place at few/most locations within the area under stress.[36,38]

State of the art RRAMs use transition metal oxides (TMOs) as insulators, including HfO_2,[39–42] Al_2O_3,[43–46] TiO_2[47–50] and TaO_X.[51,52] In these cells, RS is related to the formation and dissolution of a nanosized conductive filament (CF) across the insulator,[35] leading to an effective connection/separation of the two electrodes. In this case RS is a local phenomenon. The physical mechanisms inducing the formation/dissolution of the CF depend on the materials that compose the MIM cell (not only the insulator, but also the metal),[53] and it is thought that mainly two phenomena are predominant.[54–58] The first is the movement of oxygen vacancies in the TMO as a consequence of the applied field, leaving behind an oxygen-free metallic path.[54] These devices have been called valence change memories (VCM)[55] and/or redox random access memory (ReRAM).[56] The second is the generation of a CF made of metallic ions from the adjacent electrodes, which can penetrate into the dielectric when the MIM structure is polarized.[57] These devices are called electrochemical metallization (ECM) memories,[55] programmable metallization cells (PMC)[58] and/or conductive bridge random access memories (CBRAM),[59] even though all these names refer to the same structure.

Over the past decade many RRAM prototypes with different characteristics have been reported.[39–52] Amongst them, the most remarkable performances are: i) ultrafast (<20 ns) logic state transitions;[31,32,44,45,60] the reset (LRS-to-HRS transition) process is usually much slower (60 ns) than the set (HRS-to-LRS transition) one.[61,62] Ref. [32] achieved sub-nanosecond (300 ps) set/reset transitions in HfO_X-based RRAMs. ii) Energy consumption per state transition down to 0.1 pJ,[31,44] lower than that of other technologies, such as PCRAM[63] and MRAM.[64] iii) Long cycling endurance up to 10^{12} cycles. Ref. [33] achieved 10^{12} cycles using Ta_2O_{5-X}/TaO_{2-X} bilayer structures coupled with Pt electrodes. iv) Long data retention.[46] Ref. [65] indicated that RRAMs can retain a resistive state even at high temperatures (up to 200 °C). v) As the switching takes place through nanosale CFs,[35] the area of the cell is just limited by the area of the CF (typically tens of nanometers).[31] For example, Ref. [31] reported a 10 nm × 10 nm TiN/Hf/HfO_X/TiN RRAM with fast ns-range on/off switching times at low voltage below 3V, switching energy <0.1 pJ bit^{-1}, excellent endurance >5 × 10^7 cycles, current on/off ratios (I_{ON}/I_{OFF}) >50. The devices also showed 30 h retention at 200 °C. RS has been observed in even smaller areas (≈10 nm^2) using the tip of a conductive atomic force microscope (CAFM).[35] vi) Simple fabrication process, as the structure basically consists of a capacitor. The materials that form the RRAM have been used in complementary metal oxide semiconductor (CMOS) technology for years. This favors their three dimensional integration.[66] RRAMs have also shown potential for multi-bit storage per unit cell,[43,67] highly desired for future NVM technologies.[2]

All these factors, summarized in Table 1, have been observed in RRAMs made of different materials (e.g. TaO_X provides the highest endurance, HfO_X the fastest transitions and lowest power consumption), but no single RRAM has yet shown all NVM technology requirements simultaneously.[1,2] The most critical tradeoffs are speed–retention, power–speed and

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Table 1. Technology requirements for RRAM according to ITRS[2] compared to the best performances reported for TMO-based and GRMs-based RRAM. I_{ON}/I_{OFF} is not strictly a technology requirement, but it is a reference parameter usually quoted in RRAM literature.

Parameter	Technology requirements	TMOs based RRAMs			GRMs based RRAMs		
		Best performance	Device structure	Ref.	Best performance	Device structure	Ref.
Operating voltages	<1 V	0.3 V	Ti/HfO_2/TiN	[41]	≈ –0.6 V	ITO/GO/Ag	[251]
		0.1 V	Pt/Ni/Al_2O_3/SiO_2/Si	[43]	≈0.4 V	Ti/*h*-BN/Cu	[163]
		–0.2 V (set)/0.5 V (reset)	Pt/TiO_2/Pt	[111]	≈0.7 V	Al/GO/Al	[253]
Power consumption	≈10 pJ/transition	0.1 pJ per transition	TiN/Hf/HfO_X/TiN	[31]	≈100 pW	Gr/TiOx/Al_2O_3/TiO_2/Gr	[185]
		0.1–7 pJ per transition	Al/Ti/Al_2O_3/s-CNT	[44]	–	–	–
Switching times	<10 ns/transition	300 ps	TiN/TiO_X/HfO_X/TiN	[32]	10 ns (set)/1 ns (reset)	W/ta-C/W	[286]
		<10 ns	Al/Ti/Al_2O_3/s-CNT	[44]	5 ns (set)/5 ns (reset)	Pt/RGO–th/Pt	[273]
		≈ ns level	Cu/Al_2O_3/aSi/Ta	[45]	<10s	PEN/Ti/Pt/GO/Ti/Pt	[280]
Endurance	$>10^9$ cycles	10^{12} cycles	Pt/Ta_2O_{5-X}/TaO_{2-X}/Pt	[33]	2×10^{13} cycles @ 75 °C	W/ta-C/W	[286]
		5×10^9 cycles	Pt/TaO_X/Pt	[364]	10^8 cycles	Al/PFCF/RGO/ITO	[351]
		$>10^{12}$ cycles	Ta/TaO_X/TiO_2/Ti	[111]	10^3 cycles	Ag/MoS_2/Ag	[316]
		10^{10} cycles	Pt/TaO_X/Ta	[346]	>650 cycles	Ti/h-BN/Cu	[163]
		10^{11} cycles	W/AlO/TaO_X/ZrO_X/Ru	[347]	–	–	–
Data retention	>10 years	>10 years @ 85 °C	Pt/Al_2O_3/HfO_2/Al_2O_3/TiN/Si	[46]	$>10^7$ s (115 days)	Al/GO/ITO	[249]
		>10 years @ 85 °C	Pt/TaOx/Pt	[364]	–	–	–
MIM cell Size	576 nm^2	5 nm^2	TaN/TiN/Zr/HfO_2/CAFM tip	[296]	8.5 nm^2	Pt/ta-C/C-AFM tip	[296]
		10 nm × 10 nm	TiN/Hf/HfO_X/TiN	[31]	–	–	–
I_{ON}/I_{OFF} ratio	10^6	3×10^6	Ni/GeO/STO/TaN	[348]	$\approx 10^9$	Ag/ZrO_2/SLG/Pt	[349]
		2×10^6	Pt/Gd_2O_3/Pt	[350]	$>10^6$	Ti/*h*-BN/Cu	[163]

endurance–retention.[1] Crossbar Inc.[68] claimed the development of RRAMs covering all these capabilities, but no details about the composition of the core cell have been revealed to date. ITRI,[65] NEC,[69] and Fujitsu[70] have also announced similar devices, with no commercial device yet available. Panasonic has commercialized the MN101L RRAM Embedded 8-bit microcontroller unit,[71] Adesto is distributing their Mavriq 45 nm CBRAM,[72] and Nantero developed a RRAM memory using MIM cells integrated on CNTs, but their use is still limited to few applications (mainly sensors).[73] More information about commercial RRAMs can be found in Ref. [1].

Despite these developments, reliability issues (endurance, retention) and variability (cycle-to-cycle and device-to-device) of essential parameters like set/reset voltages (among others), as well as the understanding of failure mechanisms are still hindering large-scale RRAM manufacturing.[1,2] Therefore, the reproducibility and uniformity of RS in RRAMs still remains an area of active research, with the need to optimize the materials that form MIM cells.

One promising approach consists of replacing the metallic and/or insulating films of the MIM structures with novel materials with enhanced capabilities which, at the same time, could provide new features to the devices, such as transparency and flexibility.[74,75] Along these lines, graphene and related materials (GRMs) are at the centre of an ever-increasing research area due to their unique electronic,[76] physical,[77] chemical,[78] mechanical,[79] optical,[80] magnetic[81] and thermal[82] properties.[83] The term GRMs encompasses graphene, graphene oxide (GO), transition metal dichalcogenides (TMDs), hexagonal boron nitride (*h*-BN), black phosphorous (BP) and any other layered material (LM). Furthermore, a variety of thin carbon films have been considered for the implementation of RRAMs, ranging from sp^2 rich amorphous carbons (a-C),[84–87] to sp^3 rich tetrahedral amorphous carbons (ta-C).[88,89]

Here we review the use of GRMs to build RRAMs, we describe the fabrication process of RRAM devices using GRMs (Section 2), the advantages of using graphene as top/bottom electrode (Section 3), the performance achieved using graphene oxides (Section 4) and amorphous carbons (Section 5), as well as recent observations of RS in other LMs, including TMDs, *h*-BN and BP, among others (Section 6). The status and prospects of GRM-based RRAM technology are discussed in Section 7.

2. Fabrication of RRAMs using GRMs

A detailed description of the different approaches for the preparation of GRMs can be found elsewhere.[83,90] The aim of this section is to emphasize the methods used to implement GRM-based RRAMs, with special emphasis on those that are scalable. We also include practical information for device integration.

2.1. Device Architecture

Different device architectures to achieve NVM using GRMs have been suggested. The first used a NVM configuration based

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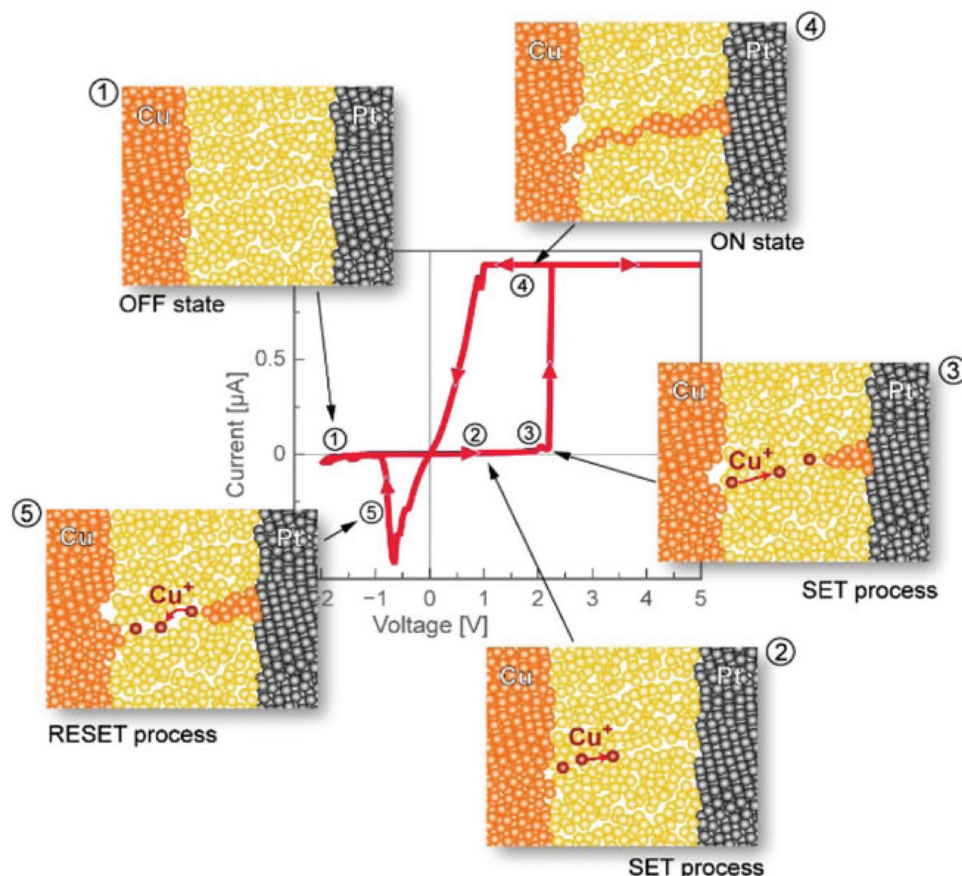

Figure 1. Current–voltage characteristics of ECM/CBRAM cell with schematic of the physical processes. Reproduced with permission.[34] Copyright 2014, John Wiley and Sons.

on graphene FETs (GFETs), such as floating gate and charge-trap memories.[91–99] RRAMs based on redox-switchable functionalized graphene nanoribbons,[100] stripes of thin (<10 nm) graphitic material grown by chemical vapor deposition (CVD)[101] and graphene/metal contacts[102] have also been proposed.

The first reports using GRMs in MIM-like RRAMs did not use the vertical MIM structure, but planar configurations containing a transversal insulating nanogap[101–105] (see **Figure 2**a and b). Ref. [103] fabricated a planar device with two electrodes connected by a single layer graphene (SLG) placed on a 300 nm SiO_2/Si substrate by micromechanical exfoliation (MC), very similar to a single back-gated GFET.[106] By applying between 2.5 and 4 V, the breakdown of the SLG channel (physical fracture) was induced.[103] By applying a reverse bias from 0.1 up to 5 V, reproducible transitions between HRS and LRS could be observed. Ref. [104] improved this performance using 5–10-nm-thick

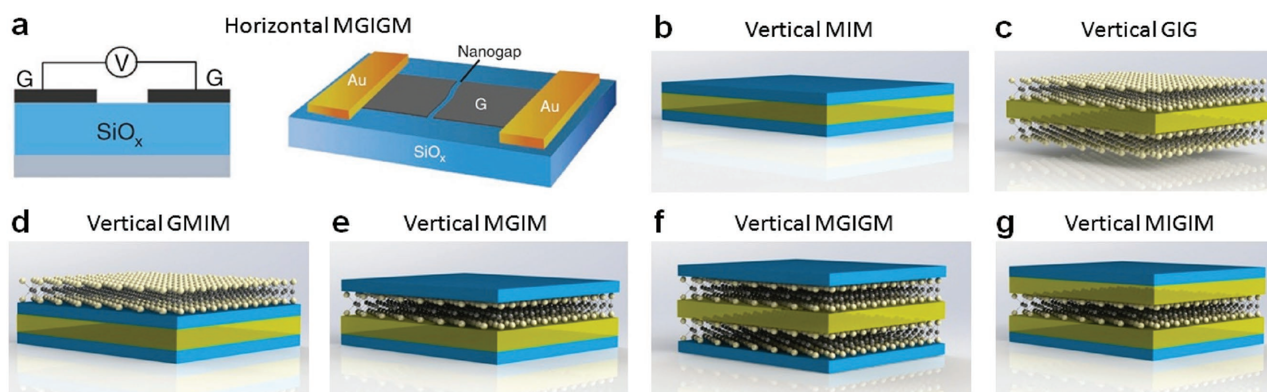

Figure 2. Device structures proposed in GRMs-based RRAM technology. M indicates metal, I indicates insulator, and G indicates GRM. The electric field in (b–g) is always applied between top and bottom layers.

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films of graphitic material (consisting of discontinuous graphene sheets grown by CVD) and reported bistability in current vs. voltage (I–V) curves with I_{ON}/I_{OFF} up to 10^7 and switching times as fast as 1 µs. Ref. [105] further enhanced the capabilities of planar bilayer graphene (BLG) switching devices by coating a 10-nm layer of conducting 3-aminopropyltriethoxysilane (APTES) molecules over the surface of the insulating region (SiO_X). Nevertheless, the difficulty in controlling the size of the nanogap[104–106] and the likely large device-to-device variability (statistical information was not reported), made most works concentrate on the vertical MIM-like RRAMs (such as those shown in Figure 2b), which is by far the most widespread and competitive device architecture developed thus far for RS-based NVMs. [107–112]

The core cell of state-of-the-art RRAMs consists of a matrix of vertically aligned MIM structures[34,35] (see Figure 2b). These can be fabricated by sequentially depositing each material on a desired substrate, using standard industrial processes such as atomic layer deposition (ALD),[113] sputtering[107] and/or electron-beam evaporation.[114] GRMs can be used in multiple parts of RRAMs (see Figure 2c–f): i) replacing one/all layers in the MIM structure, leading to alternative configurations such as, for example, graphene/insulator/graphene (GIG) or metal/*h*-BN/metal structures; and ii) introducing one/few additional GRM layer/s within the standard MIM cell, leading to MGIM, MIGM, MGIGM, GMIM, MIMG and GMIMG (where *G* denotes a generic GRM). Another possible configuration is the MIGIM structure, in which the GRM is used for charge trapping purposes[115,116] (see Figure 2g). In all cases, the goal is to improve the NVM performance (i.e. switching speed, retention time, endurance, power consumption) as well as to exploit some of the distinctive properties of the GRM (i.e. transparency[74] and flexibility;[75] enhanced thermal heat dissipation,[117] and chemical stability have been achieved using GRMs in other devices like FETs,[118] meaning that these properties may be also achieved in RRAMs).

2.2. Insertion of GRMs in the RRAM Structure

The main challenge associated with the fabrication of vertical RRAMs using GRMs is that the GRM cannot be introduced in the MIM structure using conventional fabrication tools. A large portion of the reports on GRMs used non-scalable techniques, such as micromechanical exfoliation (MC).[119,120] MC can produce flakes with a very low number of defects,[121,122] but this is not yet industrially scalable. This strongly limits its application in RRAMs, and only allows RS studies using local techniques, such as CAFM.[123] Industrially scalable GRM production methodologies,[83] such as liquid phase exfoliation (LPE)[83,90,124] and CVD[90,125] are now available, and are the most used for the fabrication of RRAMs.[126–129]

LPE gives GRMs flakes of different sizes and thicknesses (typically below 1-µm diameter and 1–20 layers thick).[83,90,124,130] They have been introduced in RRAMs by drop casting,[131] spin coating,[132] or ink-jet printing,[133] which leads to 15–500-nm-thick films.[126–129] LPE is cheap and scalable,[83] but the rough surface of the samples obtained by this method (typically RMS > 20 nm)[134] may be an important source of variability,[135–137] which is one of the main concerns of RRAM technology.[1] The lack of variability analyses in all LPE-based-RRAM reports published to date[138–141] indicates the need for further studies.

CVD is the technology most widely used to produce GRMs for electronic devices, as it allows wafer-scale production.[83] GRMs can be grown by CVD on different substrates. In the case of SLG, metals with low carbon solubility (such as Cu, Ir, Co, Ni) are necessary.[142–144] Some reported direct CVD growth on SiO_2.[145–147] For MoS_2,[148–152] TiS_2,[153] TaS_2,[154] WS_2,[155] $MoSe_2$[156,157] and WSe_2[158] direct CVD growth on insulating substrates like SiO_2 and Al_2O_3 is preferred because their lattice constants offer a good match to that of the GRM.[148–158] CVD growth of *h*-BN was also reported on Cu,[159] Fe,[160] and Pt.[161] Ref. [162] reported the CVD growth of BP on Si using a red phosphorous powder source.

When working with insulating GRMs (such as *h*-BN) grown by CVD, the metallic substrate can be used as bottom electrode.[163] This facilitates the fabrication of RRAMs, and the top electrode can be then deposited by photolithography or shadow mask, plus metal evaporation. However, the underlying metal can have large roughness (RMS ≈ 30 nm)[164] due to the polycrystallization suffered during the CVD growth at high temperatures, usually not below 800 °C.[142–144,148–152] Therefore, the growth of insulating GRMs on ultra-flat metal-coated wafers is of utmost importance to avoid roughness-induced variability, as well as to offer better integration with industry. In general, the thermal budget may be an issue for the fabrication of GRM-based RRAMs. On the contrary, when working with conductive GRMs (such as graphene), the metallic substrate used during CVD growth is a burden for RRAM fabrication, because sometimes the presence of GRMs is required on substrates not favorable for their CVD growth, e.g. HfO_2 and other TMOs.[106] One approach is to transfer GRMs onto the desired substrate using polymer scaffolds, polymethyl mechacrylate (PMMA) being the most commonly used.[83,90,165–167] The problems associated with this technique are: i) physical breakdown of GRMs,[168,169] producing cracks, which may locally alter the properties of the devices.[170,171] For example, a MGIM device in which the GRM contains holes may lead to local MIM structures. ii) polymer residuals on the GRM surface. Although this may not result in device failure, since the polymer is insulating, it can be understood as a decrease of the effective area of the MIM capacitor. The introduction of annealing processes (at ≈300 °C)[172] may contribute to the removal of these impurities, but may produce polycrystallization of TMOs in the RRAM (if any), leading to unwanted inhomogeneities and thickness fluctuations.[135–137] Polymer-free transfer techniques, such as electrostatic graphene/substrate attraction, can be used,[173] but this may increase the complexity of the process.[174,175]

Other methodologies to grow GRMs are physical vapor deposition,[176] growth on SiC,[177] and the hydrothermal method[178] but, to the best of our knowledge, their use in RRAM technology has not yet been reported.

The deposition of insulators on GRMs is also problematic. According to Ref. [179], TMOs cannot be deposited directly by atomic layer deposition (ALD) on defect-free SLG, due to the lack of dangling bonds or functional groups. Ref. [180] observed that, when trying to grow HfO_2 by ALD on MoS_2, HfO_2 did not form a homogeneous film, but instead islands on the MoS_2 surface, probably located at MoS_2 defects (where there are dangling bonds

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that allow HfO_2 agglutination).[181] One possible approach is the functionalization of the GRM surface,[182–185] which may enhance the homogeneity of the TMO film at the interface. The most common strategies to achieve a uniform SLG/high-k interface are functionalization with NO_2,[182] metal seed layers,[183] organic seed layers[184] and ozone (O_3).[182–184] An interesting method to generate a SLG-TiO_x/Al_2O_3/TiO_2-SLG cell was proposed by Ref. [185]. A seed Ti layer was first deposited on the bottom SLG electrode by e-beam evaporation and then oxidized to TiO_x in air. The Al_2O_3/TiO_2 stack was then deposited by ALD, and the top SLG electrode was transferred. Another similar GIG device was fabricated by Ref. [186] by depositing a bilayer insulating film made of Ta_2O_{5-x}/TaO_y on a CVD-SLG using radio-frequency and reactive sputtering, followed by another CVD-SLG transfer.

For devices designed to be tested in a probe station, the use of top metallic electrodes is unavoidable, as placing the large tip on a SLG top electrode may damage it. Therefore, the GI interface is in fact a MGI. One method to measure the SLG electrodes without the need of metal deposition is the use of CAFM, which controls very accurately the tip/sample contact force and does not damage the GRM surface.[187] CAFM can also allow the investigation of ultra-scaled RRAMs.[35]

3. Use of Graphene as Top/Bottom Electrode

3.1. Transparency

One motivation for using graphene in electronic devices is to provide them with flexibility[75] and transparency.[74] For transparent devices, indium tin oxide (ITO) has been traditionally the preferred electrode material,[188–190] but its brittle nature makes it less suitable for flexible/foldable devices. One alternative is using organic materials, such as conductive polymers,[191] but in this case the NVM performance (with retention times of just 10^4 s and endurance below 100 cycles) is usually much lower than state-of-the-art TMO-based RRAMs. [1,31–33]

Ref. [192] fabricated transparent MLG/Dy_2O_3/ITO structures by transfer of CVD-grown multilayer graphene (MLG) patterned in a subsequent photolithography step. The devices showed forming-free unipolar RS with $I_{ON}/I_{OFF} \approx 10^5$, low set and reset voltages (0.4 and 0.2 V respectively), endurance >100 cycles, retention time $>10^4$ s and typical switching power and speed of 4.4 μW and 60 ns. Furthermore, the devices showed a transparency ≈80%. The performance as RRAMs of these devices is better than other graphene-free cells, such as ITO/ZnO/ITO,[188] ITO/AlN/ITO,[189] ITO/Gd_2O_3/ITO,[190] and other transparent prototypes like Ga-doped ZnO.[193] Ref. [105] further improved the optical performance by exploiting bi-layer graphene (BLG) in BLG/SiO_X/BLG structures, with a transmittance >90% (see **Figure 3**a–c). Ref. [74] also achieved good RRAM functionality with an overall light absorptance <25% in devices made of ITO/SLG/ZnO/ITO, which also showed better RS uniformity than its graphene-free counterparts. Ref. [75] used MLG with a transmittance up to 92% to fabricate a flexible organic memory device.

The characteristics of transparent and flexible graphene-based RRAM devices in literature are summarized in **Table 2**. Coupling graphene electrodes with organic RS media seems to provide the highest transparency ≈92%,[194] maintaining high

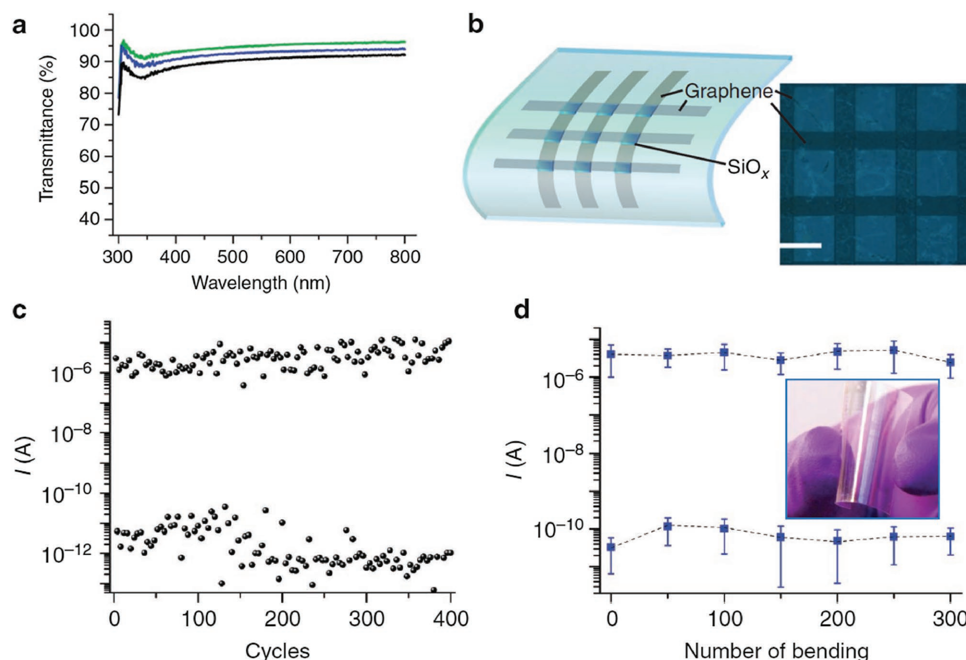

Figure 3. a) Transparency of SLG/SiO_2/SLG RRAM on glass. b) Schematic SLG/SiOx/SLG crossbar structures on a plastic (fluoropolymer) substrate (left panel) and optical image (right panel). Scale bar = 20 μm. c) Endurance measured from one of the crossbar devices using +5 and +14 V as set and reset voltages. The memory states (current) were recorded at +1 V. d) Current levels of both ON and OFF memory states (read at +1 V) from a crossbar device during repeated bending of the plastic substrate to $r_b \approx 0.6$ cm. The inset shows transparent memories using the pillar structures on plastic substrate. Reproduced with permission.[105] Copyright 2012, Nature Publishing Group.

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Table 2. Graphene-based RRAMs with transparency and/or flexibility capability. In the column headed "Flexible", r_b and C are the bending radius and number of RS cycles collected during the test. In the "Transparent" column, the percentages correspond to light transmittance, and "Yes" means that the authors claim that the structure is transparent but did not quantify it.

Device structure	Fabrication method	Device size	I_{ON}/I_{OFF}	Set V [V]	Retention [s]	Endurance [cycles]	Power consumption [µW]	Switching time [ns]	Transparent	Flexible	Ref.
MLG/Dy_2O_3/ITO	CVD (Transfer)	$80 - 3 \times 10^4$ [μm^2]	$>10^5$	0.4	$>10^4$	>100	4.4	60 (set) 60 (reset)	80%	No	[192]
ITO/SLG/ZnO/ITO	CVD (Transfer)	200 µm in diameter	20	–	10^4	>100	–	–	Yes	No	[74]
PS/SLG/PMMA/ SLG/PMMA[a)]	CVD (Transfer)	500 µm in diameter	L1: 10^4 L2: 10^6	L1: –2 L2: –4	10^4	1	–	–	Yes	No	[116]
Al/PMMA/MLG/ PMMA/ITO/PET	CVD (Transfer)	18–27 µm in diameter	4.4×10^6	3.4	1×10^5	1.5×10^5	–	–	Yes	$r_b = 10$ mm $C = 1.5 \times 10^5$	[195]
MLG/PI:PCBM/Al	CVD (Transfer)	–	$\approx 10^6$	4	1×10^4	>30	–	–	92%	$r_b = 4.2$ mm $C = 1 \times 10^4$	[75]
Ti/Pt/TiO_2/G/PEN (G thickness not mentioned)	CVD (Transfer)	36×36 [μm^2]	10^2	2	10^6	1	3 (set) 94 (reset)	–	Yes	$r_b = 10$ mm $C = 100$	[196]
BLG/SiO_X/BLG/ ITO	CVD (Transfer)	100 µm in diameter	10^{5}[b)]	5	–	100	–	–	90%	No	[105]
BLG/SiO_X/BLG/ Polymer	CVD (Transfer)	100 µm in diameter	10^6	5	–	400	–	–	Yes	$r_b = 12$ mm $C = 300$	[105]

[a)]This device shows multilevel RS. Depending on V_{SET}, I_{ON}/I_{OFF} changes. Table 2 reports the parameters for both levels; [b)]This value is not well supported in Ref. [116]: the I–V curve only shows 1–2 orders of magnitude, while the R vs. Cycle plot shows $\approx 10^5$.

I_{ON}/I_{OFF} $\approx 10^6$ and long retention $\approx 10^4$ s. All graphene-based transparent devices were fabricated by CVD plus transfer (see Table 2).

3.2. Flexibility

Graphene can be used to increase the flexibility of RRAM cells. Ref. [105] reported BLG/SiO_X/BLG cells with no RS degradation after bending >300 times at a bending radius (r_b) ≈1.2 cm (see Figure 3d). Ref. [195] presented a flexible organic device based on SLG sandwiched by two insulating poly(ethylene terephthalate) polymer (PET) layers.[195] A Ni/PMMA/SLG/PMMA/ITO/PET cell was fabricated by transferring a CVD-SLG and spin-coating the PMMA layers. In this case SLG was used as a charge storage medium. Ref. [195] reported a good memory performance including endurance $>1.5 \times 10^5$ cycles, I_{ON}/I_{OFF} $>10^6$, and retention time $>1 \times 10^5$ s. Especially significant was the lack of interference observed for scaled-down devices with SLG, as well as the ability of the devices to maintain similar switching characteristics (set/reset voltages and I_{ON}/I_{OFF}) even after being bent ($r_b \approx 1$ cm) over 1.5×10^5 times. Ref. [75] designed 8×8 cross-bar array-type flexible organic RRAMs on PET using MLG electrodes coupled with two different active layers: one polyimide and the other 6-phenyl-C_{61} butyric acid methyl ester (PCBM). Typical write-once-read-many characteristics and high I_{ON}/I_{OFF} up to 10^6 were achieved; for >1000 mechanical cycles (r_b between 4.2 and 27 mm) the devices maintained a retention time $>10^4$ s with <12.5% resistance fluctuations in both HRS and LRS.[75] Comparing the RS performance of all flexible RRAMs exposed to mechanical stresses is complex because these may have been applied using different r_b and times. The influence of the bending time in flexible RRAMs was not reported to date, while most works report r_b.[75,105,195,196] Smaller r_b may produce more damage to the devices, as this introduces higher stresses. Therefore, from Table 2 it can be concluded that the RRAMs with the best performance under bending are those in Ref. [195].

3.3. Blocking Layer for Atomic Diffusion

The most common electrode materials in RRAMs are Al, Pt, Au, Cu, Ti and Ni.[197–202] These not only serve as contacts, but play an essential role on the physics,[53] kinetics[202] and statistical distribution[203,204] of the RS. For example, different metallic electrodes can alter the number of CFs in RS media, which has an impact on the shape (sharp or progressive) of the reset process, among others.[53] One strategy to tune the switching characteristics of RRAMs is the use of active metal electrodes

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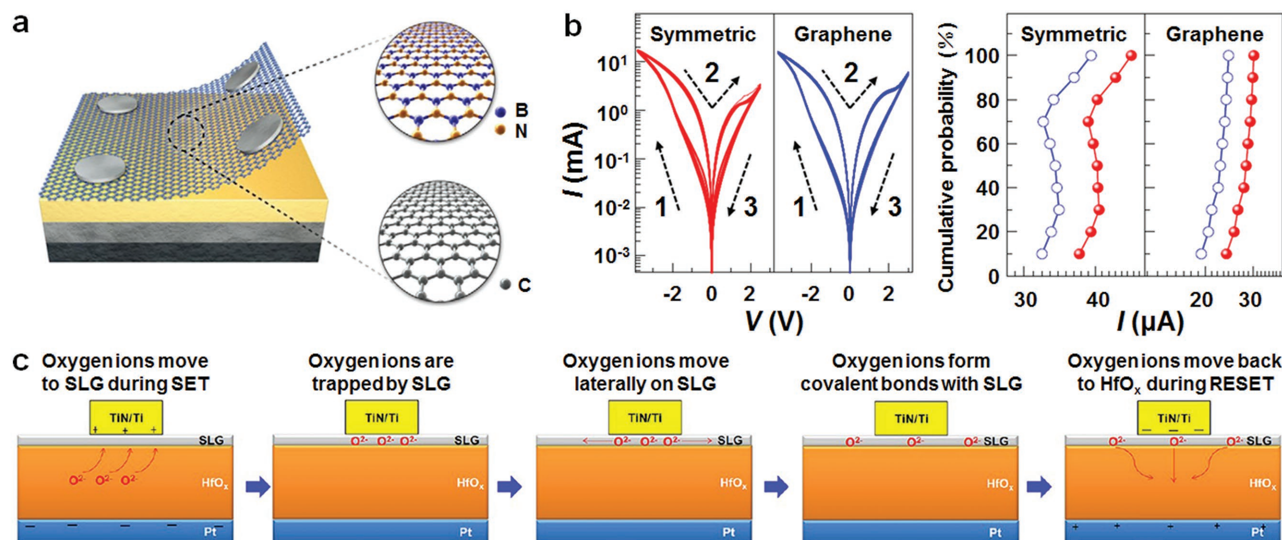

Figure 4. a) Schematic of SLG inserted between the top electrode and insulating film of a RRAM cell. b) Resistance switching *I–V* characteristics of a symmetric Al–WO_3–Al device and a Al(SLG)–WO_3–Al device. Cumulative probability of the HRS current at ±0.5 V for both configurations. Reproduced with permission.[107] Copyright 2015, Elsevier. c) Schematic diagrams of oxygen ions movement in MGIM structures. The diagrams represent (from left to right) steps of the process including movement of oxygen ions to SLG during SET, capture of oxygen ions by SLG, movement of oxygen ions laterally on SLG, formation of covalent bonds with SLG, followed by movement of oxygen ions back to HfO_X during reset. Reproduced with permission.[217] Copyright 2013, American Chemical Society.

(like Ti or Zr) that can interact with the species from the insulator. For example, in Pt/Ti/HfO_2/Pt cells[205–207] oxygen atoms from the HfO_2 layer can interact with the Ti electrode. This allows the observation of bipolar RS thanks to the movement of oxygen in and out of the HfO_2 film, forming an O-vacancies-based CF with the narrower end at the cathode side.[206] On the contrary, in Pt/HfO_2/Pt devices[205–207] the O-vacancies movement towards the electrode is difficult, generating a CF that can only be disrupted by applying large currents,[205,206] which melt the filament by Joule effect.[208] In this case, the forming event is sharper, which leads to a higher $I_{ON}/I_{OFF} \approx 10^4$ for Pt/HfO_2/Pt instead of ≈12 for Pt/Ti/HfO_2/Pt, but the endurance may be worse due to the generation of an avalanche current,[209] BD spot propagation,[210] thermal heat,[211] insulator contamination by metal migration[212] and dielectric-breakdown-induced epitaxy.[213] Comparing the performance of Pt/Ti/HfO_2/Pt and Pt/HfO_2/Pt cells it has been observed that,[205–207] while the LRS currents in Ti-free devices were linear and the filament was symmetric, those including inserted Ti layers drove exponential currents representative of partially formed conical filaments, with the narrower end at the HfO_2/Ti interface. This was confirmed by fitting the experimental *I–V* curves to the quantum point contact model.[214] Moreover, at larger electric fields, the movement of metallic ions may also be activated, allowing their penetration in the TMO and producing even larger changes in the device conductivity than the motion of oxygen vacancies.[40] Therefore, as SLG is impermeable,[77,215] introducing SLG between metal and insulator alters these interactions.[108,216]

Ref. [107] observed that inserting CVD-SLG in Al/WO_3/Al structures stabilized the characteristics of the RRAM devices (see **Figure** 4a and b), reducing the variability of the set/reset voltages and currents, as well as enhancing the endurance. In SLG-free cells, when positive bias is applied to the top electrode, oxygen ions from the Al/WO_3 interface are pushed into the oxide bulk, leading to the formation of CFs rich in oxygen vacancies (which can be charged by electrons). During the reset process, the oxygen-deficient region is reoxidized. Ref. [107] suggested that SLG blocks the diffusion of oxygen ions into the reactive Al layer, which reduces the cycle-to-cycle variability in *I–V* curves. The dissolution of oxygen in SLG is very scarce and it presents a barrier for potential oxygen diffusion.[56] Both factors impede the diffusion of oxygen through SLG, avoiding the interaction with the metallic top electrode. Ref. [217] suggested that the electric field applied during the set operation can move the oxygen ions towards the metal/oxide interface, but they cannot penetrate into the Ti electrode due to the presence of the interfacial SLG (see Figure 4c). At most, the oxygen ions could form covalent bonds with the SLG defects (missing atoms and/or dangling bonds),[185,217] leading to a p-type doping that can be released during the reset transition. However, Ref. [55] reported the migration of metallic ions from the electrode into the dielectric in ECMs, even with the presence of interfacial SLG. Ref. [55] reported that, in ECM cells based on Ta/SLG/TaO_X/Pt stacks, the switching is influenced by the formation of Ta ions and their interaction with the TaO_X active layer. Nevertheless, Ref. [55] used large device areas ranging between 25 × 25 and 1000 × 1000 µm^2. The presence of cracks and leaky grain boundaries can happen in CVD-grown and transferred SLG,[218] thus MLG may provide a better protection than SLG.

3.4. Lowering Power Consumption

The out-of-plane SLG contact resistance is larger than that of metallic electrodes,[219] which can be used to reduce the currents

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in both resistive states of the RRAMs, lowering power consumption. Ref. [217] analyzed bipolar RS in TiN/Ti/SLG/HfO_X/Pt RRAMs. Cyclic voltammetry indicated a reduction of the reset current by a factor ≈11 compared to SLG-free devices (**Figure 5**a), further corroborated using cumulative probability plots. Despite this improvement, the plots indicate that the HRS currents under positive polarity for the SLG-based devices increase, which is an unwanted effect. Ref. [217] pointed out that comparisons between SLG-based and SLG-free cells using similar current limitations (CL, defined as the threshold current used during the forming/set processes to limit BD) were not reliable due to the low endurance of SLG-free cells at such low (100 µA) current levels. To solve this problem, Ref. [217] compared the typical RS cycles using the optimal CL for each cell (10 µA for SLG-based cells and 100 µA for SLG-free ones), suitable to produce a lower cycle-to-cycle variability (Figure 5b), and concluded that: i) The CL needed to stabilize RS in the SLG-based device is lower, which from the power consumption point of view is an advantage. Despite the current in the HRS being the same, the LRS current was reduced more than one order of magnitude. This implies that, when the filament is completely formed in the LRS, its size (diameter) is much smaller using SLG-based electrodes. ii) The decrease of LRS current reduces I_{ON}/I_{OFF}. iii) SLG avoids the current overshoot during the set process, which also reduces the maximum current during the reset transition (I_{RESET}): in SLG-based RRAMs, I_{RESET} was half CL, while in SLG-free, I_{RESET} was 2–3 times larger than CL (see Figure 5b).

Ref. [98] fabricated a Pt/Ti/TiO_x/SLG RRAM and reported similar data as Ref. [217] (Figure 5c). I_{ON}/I_{OFF} as well as both HRS and LRS currents were reduced. Therefore, from these two results,[98,217] SLG helps to stabilize RS at lower CLs, which reduces the reset current (probably due to the formation of narrower CFs) and the overall power consumption.

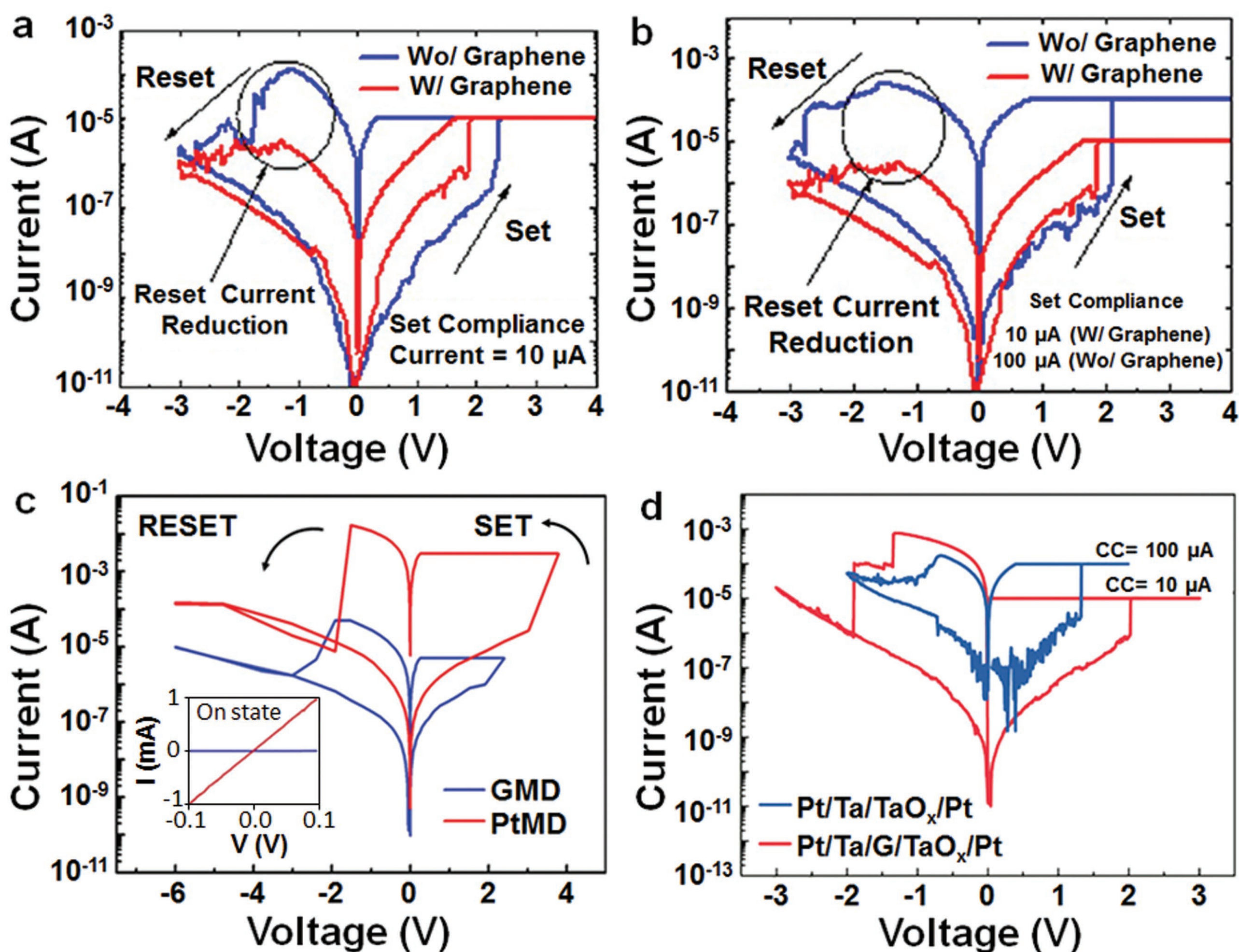

Figure 5. a) Typical RS behaviour of Ti/SLG/HfO_X/Pt (red) and Ti/HfO_X/Pt RRAMs under the same CL. b) Typical RS behaviour for the same devices but using optimal testing conditions. 10 and 100 µA are applied to achieve steady RS. Reproduced with permission.[217] Copyright 2013, American Chemical Society. c) RS curves of typical TiO_2-based memristive devices using SLG and Pt electrodes, with a SET current compliance of 5 µA and 3 mA. The arrows point to the RS directions. Inset: small-bias *I–V* curves for both devices in the ON state, showing different resistance. Reproduced with permission.[196] Copyright 2014, Wiley-VCH. d) *I–V* comparison between a Pt/Ta/TaO_X/Pt cell with SLG inserted between the Ta and the TaO_X layers (red) and one cell without (blue). The cell without SLG needs higher HRS currents for stable RS. That with SLG offers higher I_{ON}/I_{OFF} and HRS current reduction. Reproduced with permission.[55] Copyright 2015, Wiley-VCH 2015.

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Ref. [55] also observed that lower CLs (10 μA) stabilize Pt/Ta/SLG/TaO_X/Pt RRAMs (Figure 5d), producing an increase of the reset current and I_{ON}/I_{OFF} in the SLG-based cell (compared to SLG-free). These results are surprising because the CL used for the SLG-based cells was smaller, and it is usual for the reset to take place at currents similar to CL in all kinds of RRAMs (including ECMs, VCMs).[55] Indeed, Figure 5d shows a current overshoot. We cannot tell how reproducible these observations are because, unlike Ref. [217], Ref. [55] did not include the evolution with the number of cycles. On the other hand, Ref. [217] observed reset currents smaller than CL in SLG-based devices. More work is thus necessary to confirm these observations.

3.5. Suppression of Surface Effects

Most devices based on TMOs are influenced by surface effects,[220] including surface band bending,[221] chemisorption/photodesorption,[222] and surface roughness.[223] The barrier for species diffusion provided by SLG was used by several groups. For example, Ref. [74] inserted SLG into an ITO/ZnO/ITO stack to explore the device performance variation under different atmospheres (see **Figure 6**). O^{2-} chemisorption happened at the top surface of the MIM structures (in contact with the environment), resulting in defects associated to the oxygen partial pressure. Due to oxygen ion chemisorption, the partial pressure of oxygen can influence the TMOs electrical properties, as more O_2 molecules are chemisorbed with increased partial pressure.[224–227] O_2 molecules are absorbed at the TMO surface defects,[224] such as oxygen vacancies,[228] acting as electron acceptors to form chemisorbed oxygen ions, which will contribute to decrease the conductivity of metal oxide. However, the introduction of SLG (forming an ITO/SLG/ZnO/ITO structure) protects the ZnO film from chemisorption of O_2 molecules, avoiding surface effects. The effect of oxygen ions chemisorption on the switching properties of RRAMs was analyzed by Ref. [74] by comparing the resistance of HRS and LRS with and without SLG electrodes under various ambient conditions. Without SLG, the HRS shifts to a higher resistance as it can interact with the atmospheric O_2,[224] because the chemisorbed oxygen ions induce lower conductivity near the ZnO surface.[224,226] As the oxygen ions concentration increases, the surface band bending effect is more pronounced. However, with the SLG introduction at the ITO/ZnO interface the variation of HRS resistance is suppressed,[74] and it almost completely decouples the average variation of the HRS resistance from atmospheric conditions.[74] This improves device reliability, giving endurance >10^2 cycles and retention time >10^4 s.

3.6. Functionalization of Graphene Electrodes

Different functionalization strategies can be followed to achieve specific performances. For example, SLG can be used as blocking interfacial layer to avoid metal/insulator interactions.[229] If SLG is intentionally patterned with selected numbers of holes or defects, the properties of the cell at those

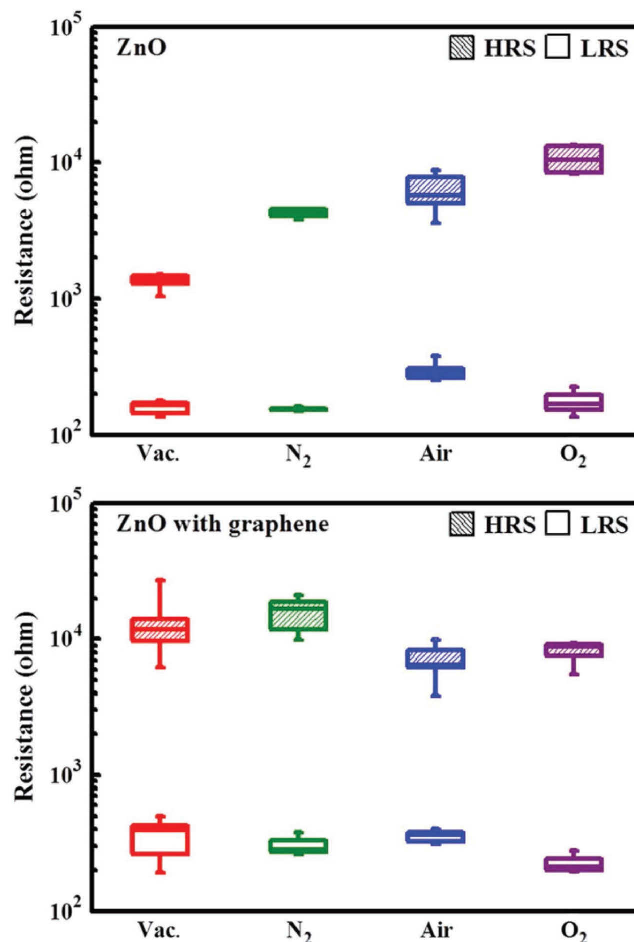

Figure 6. Atmosphere-dependent resistance in HRS and LRS of ZnO RRAMs with and without SLG electrodes. The bottom and the top of the box are the 25th percentile and the 75th percentile, the band near the middle of the box is the 50th percentile, and the ends of the whiskers represent the 10th percentile and the 90th percentile. Reproduced with permission.[74] Copyright 2013, IEEE.

locations can be modified, leading to specific local phenomena, such as local (instead of distributed) O-vacancy scavenging. Ref. [170] functionalized SLG in a MGIM structure by using controlled Ar^+-ion-assisted bombardment, which generated different amounts of defects, depending on the bombardment energy.[230] By means of CAFM Ref. [170] showed that the leakage current in functionalized samples was more confined than in pristine ones (see **Figure 7**), probably due to the lower conductivity of the SLG-free locations (i.e. the holes patterned in SLG). MGIM devices with Ar^+-ion-bombarded SLG had smaller variability in the set and reset voltages than those without, and more stable currents in each state.[170] This strategy was further studied by Ref. [171], who tuned ionic transport in Pd/Ta/SLG/Ta_2O_5/Pd RRAMs using SLG with engineered nanopores. SLG was grown by CVD on Cu and transferred with the assistance of a polymer scaffold.[165–167] The migration of oxygen ions in the device was controlled by opening some nanopores in SLG, which allowed to tune the properties of the devices.[171] However, since the nanopores

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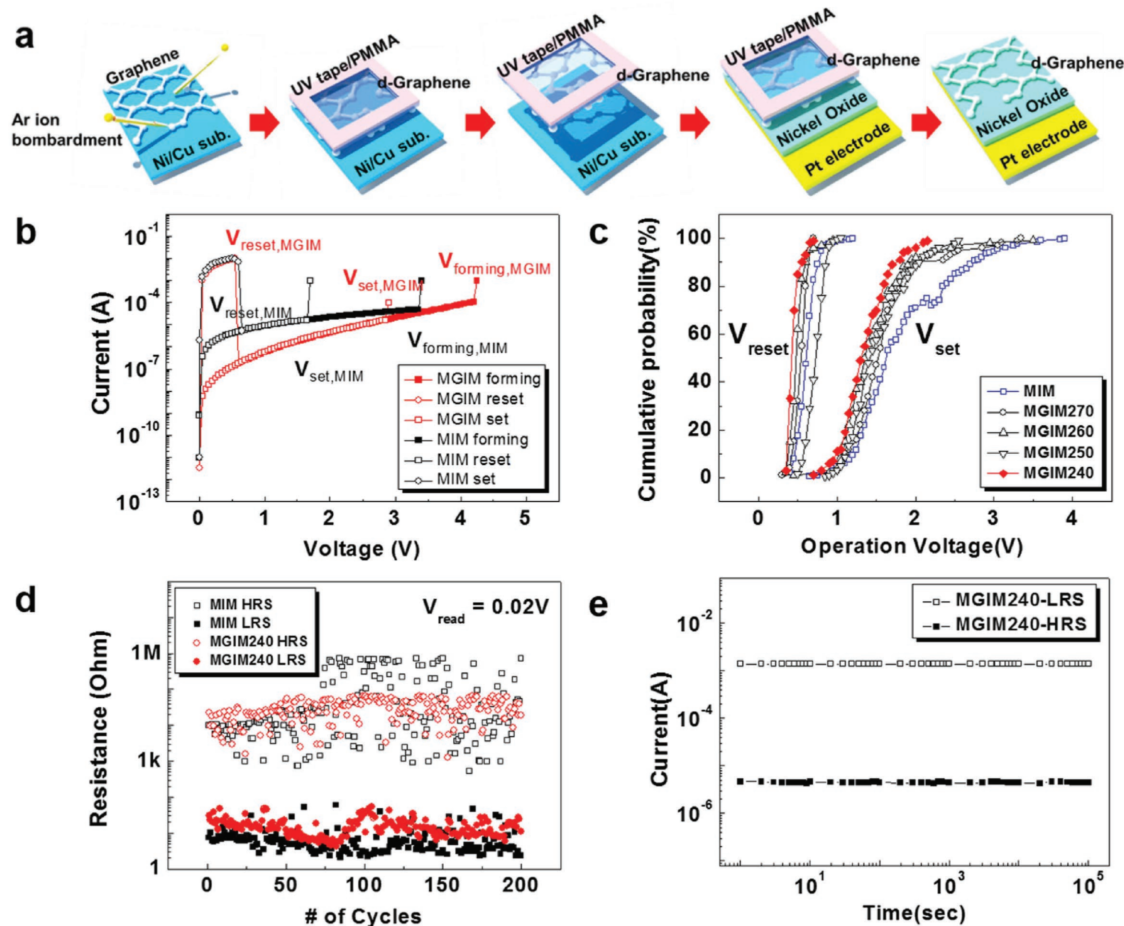

Figure 7. a) Fabrication process for a MGIM structure using functionalized SLG prepared before transfer. b) Initial *I–V* characteristics of MGIM and conventional MIM structures. c) Cumulative probability of RS voltages, V_{set} and V_{reset}, for MGIMs with SLG irradiated with Ar+ ions at 240 eV (MGIM240), 250 eV (MGIM250), 260 eV (MGIM260), and 270 eV (MGIM270) as well as a MIM. d) Change in resistance states for MGIM240 and MIM, measured at room temperature and atmospheric pressure. e) Retention characteristics of MGIM240 measured at 85 °C at 1 mTorr as well as ambient atmospheric conditions, under reading voltage ≈0.1 V. Reproduced with permission.[170] Copyright 2015, Nature Publishing group.

were patterned with e-beam lithography, the process is less scalable than in Ref. [170], which used ion-assisted reaction treatment after transfer of MLG to etch residues as well as induce defects in SLG. In all, it was demonstrated that inserting a functionalized SLG in the structure of RRAMs is a good approach to tune their properties.

Ref. [231] reversed the manufacturing order of the RRAM stack (from MLG/TaO_y/Ta_2O_{5-x}/MLG to MLG/Ta_2O_{5-x}/TaO_y/MLG). In this case, the conventional linear bipolar RS became highly nonlinear due to the bottom MLG electrode being oxidized at 400 °C in an Ar/O_2 plasma during the reactive sputtering deposition of TaO_y. Due to the low currents driven by these devices (0.5 mA at 8 V), they are promising as threshold switching and/or selector elements.

Another potential advantage of SLG electrode engineering is that the Fermi energy can be controlled, which is not possible in standard MIM structures. Using this approach, Ref. [98] engineered the tunneling barrier width and height at the interface of a Pt/Ti/TiO_2/SLG/Pt RRAM device, resulting in three orders of magnitude reduction of the switching power (from 10^{-5} W to 10^{-2} W).

3.7. Integration

One advantage when building NVMs using MIM structures is the potential for stackability and integration. One common approach[113,232,233] consists of fabricating a nanostructured material with alternate metallic and insulating films. Then, a vertical aperture (hole) is patterned and the RS media is deposited.[113,232,233] Finally, the rest of the hole is filled with another metal, leading to vertically aligned MIM cells in which the vertical electrode serves as common electrode, and each horizontal metallic film is the specific electrode of each (independent) MIM cell.[113,232] In this structure the thickness of each insulating film should be large enough to avoid cross-talk noise from cell to cell, therefore it cannot be reduced below a safe value (in the case of SiO_2 ≈ 6 nm).[113] On the contrary, the thickness of the metal should be low enough to ensure good in-plane conductivity. SLG is thus a promising building block because: i) it is only 0.34 nm thick[113] and its in-plane conductivity is excellent (≈3000 $Wm^{-1}K^{-1}$);[234] and ii) the lateral connection between SLG and the RS media provides a lower contact resistance (compared to metals). Ref. [235] used FETs with

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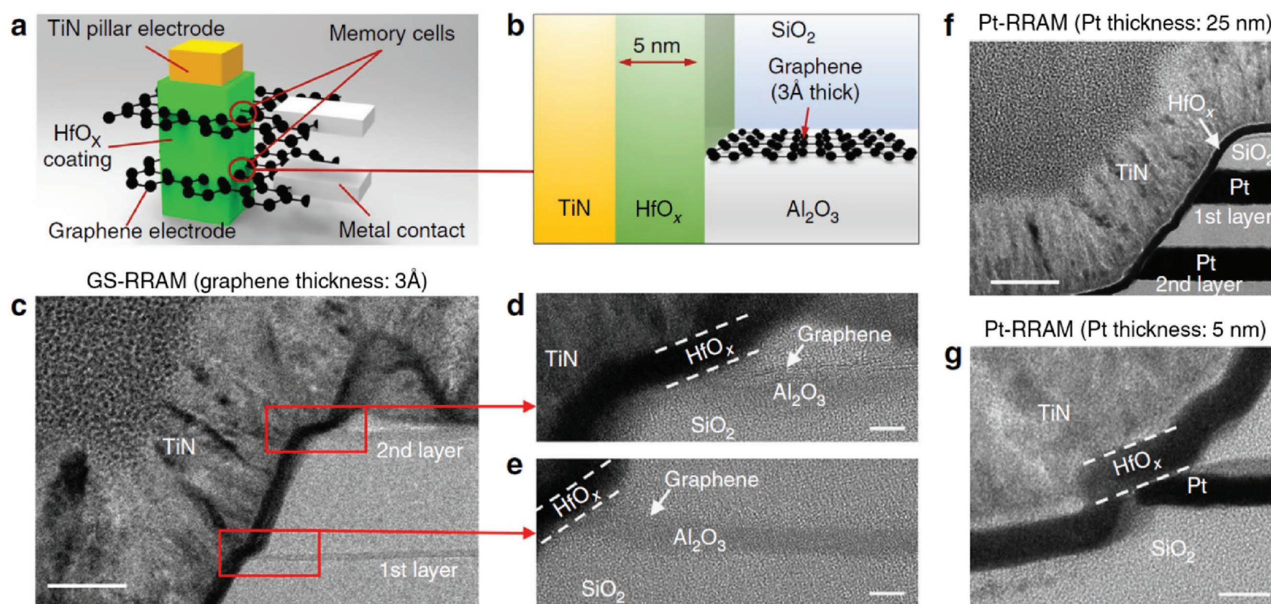

Figure 8. a) SLG-based RRAM in a vertical cross-point architecture. The RRAM cells are formed at the intersections of the TiN pillar electrode and the SLG plane electrode. The RS HfO_x layer surrounds the TiN pillar electrode and is also in contact with SLG. b) Schematic cross-section of the SLG-based RRAM. c) High-resolution TEM image of the two-stack graphene set electrode RRAM (GS-RRAM) structure. The RRAM memory elements are highlighted in red. Scale bar = 40 nm. d,e) First and second layer of GS-RRAM with SLG on top of Al_2O_3. Scale bars = 5 nm. f, g) TEM images of the two-stack Pt-based RRAMs. Scale bars = 40 nm (f) and 5 nm (g). Reproduced with permission.[113] Copyright 2015, Nature Publishing Group.

metallic electrodes that contacted the SLG channel laterally, and observed a mobility of 140 000 $cm^2 Vs^{-1}$, much higher than that of similar devices in which the SLG channel is connected vertically (40 000 $cm^2 Vs^{-1}$),[236] and very close to the phonon limited model.[235] The reason is that the in-plane bonding is covalent, while metallic electrodes deposited on top of SLG rely on weaker Van der Waals interactions. A similar methodology can be used in RRAMs, employing SLG as planar electrode contacted from the side (see **Figure 8**).[113] Using this principle, Ref. [233] fabricated RRAM devices with I_{ON}/I_{OFF} >80, low reset currents ≈20 µA and low set/reset voltages (2 to 4 V).

Ref. [186] used a similar structure consisting of SLG as edge electrode to investigate the scaling limit of RRAM integration. In this case, the RS medium was a superstructure made of Ta_2O_{5-x}/TaO_y and, as in Ref. [233], SLG was grown by CVD and transferred on SiO_2 by an electrochemical approach.[237] The Pt column and SLG serve as pillar and edge electrodes respectively. As a result, SLG edge electrodes allowed a larger density of three dimensional RRAM integration.

4. Graphene-Oxide-Based Switching Media for RRAM

Even though the electrodes are a crucial element defining the performance of RRAMs, the switching medium is the dominant one.[34] Apart from TMOs, a wide variety of materials has been proposed as switching media in RRAMs, including organic materials,[238] polymers,[239] perovskites,[240] GRMs[241] and amorphous carbons.[84–89] Mixtures/alloys of some of them, such as polymers with high density of graphene flakes[195] or organic polymers,[239] have also been used.

GO and reduced GO (RGO) have been widely investigated for RS applications.[132,133,241–253] GO films consisting of interconnected flakes are typically produced by LPE and spin coated on the surface of a substrate (which serves as top electrode), with subsequent deposition of top contacts on the GO surface[254] (see **Figures 9** and **10**). This contrasts with the atomically flat CVD-SLGs, and could have implications in terms of device-to-device variability.

Ref. [241] prepared a GO compound by using the Hummers method[255] and the resulting material was transferred onto $Pt/Ti/SiO_2/Si$ substrates, followed by top Cu electrode evaporation. The resulting Cu/GO/Pt RRAMs contained a 30-nm-thick GO film (see Figure 10), which showed I_{ON}/I_{OFF} >10, long retention times >10^4 s, and low switching threshold <1 V. The ability of GO to change its electrical resistance when subjected to voltage stresses was later confirmed in Al/GO/ITO cells.[249,256,257] Several authors[126,258–262] combined a GO active layer with diverse electrode metals (Pt, Au, Al), which allowed tuning the RS characteristics of the devices.[126,258–262]

Two competing hypotheses have been proposed to interpret the bipolar switching observed in GO films.[242,263] The first[242,263] resembles that of ECM cells using active metallic electrodes, in which metallic ions can diffuse from the electrodes towards the GO layer, leading to the formation/dissolution of a CF. The independence of the LRS resistance on temperature and the proportionality of the currents to the electric field support this mechanism.[242,263] An X-ray photoelectron spectroscopy (XPS) study of an Al/GO/ITO stack detected Al atoms along the GO film when the device was working in LRS, pointing to mass transfer during the cyclic switching.[249] The second[241] is similar to that of homogeneous VCM for inorganic materials, and suggests that absorption and

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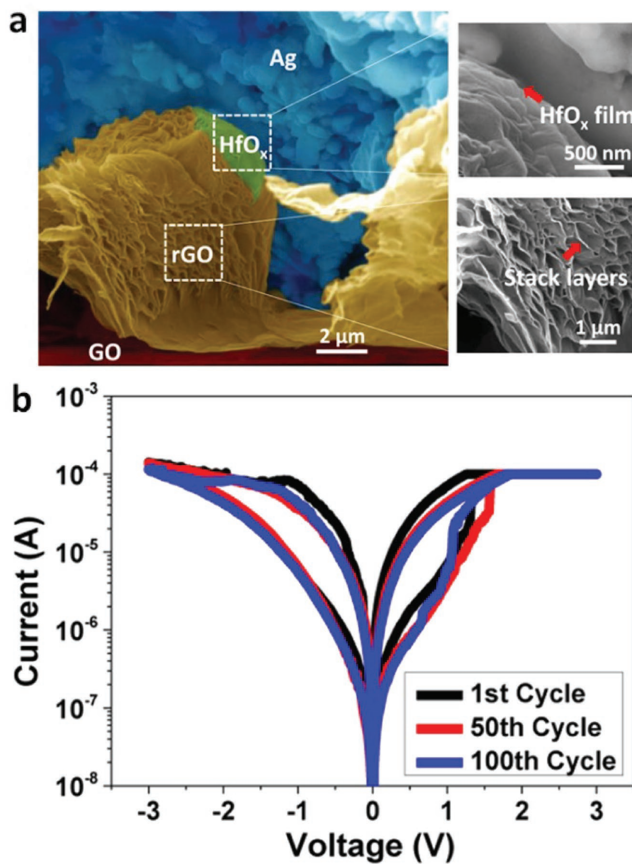

Figure 9. a) Cross-sectional SEM images of folded, aggregated and misaligned GRMs used in RRAM technologies. The insets highlight HfO_X films and stacked RGO layers, respectively. b) RS behaviour of laser-scribed RGO (LSG-) based RRAM at the first, 50th and 100th cycle, respectively. Reproduced with permission.[254] Copyright 2014, American Chemical Society.

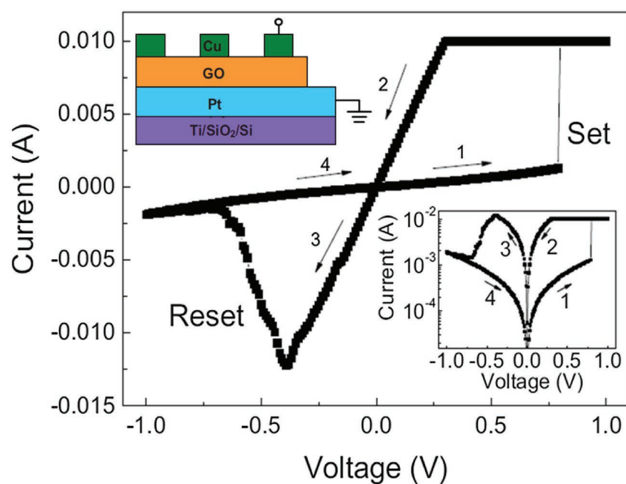

Figure 10. *I–V* characteristics of Cu/GO/Pt RRAM cell showing RS. The arrows indicate the sweep direction. The insets show the *I–V* characteristics in semilogarithmic scale and the schematic configuration. Adapted with permission.[241] Copyright 2009, American Institute of Physics.

desorption of oxygen functional groups could induce RS in the GO film.[264] In most cases, GO is associated with various oxygen groups, such as carboxyl,[265] hydroxyl, and epoxide, with their oxygen ions usually contributing to form the conduction path.[264,265] Two states—sp^3 and sp^2—exist in these oxygen groups; the latter has larger conductivity due to the introduction of π-electrons from the removed oxygen groups.[264] The change of the oxygen bonding state in the GO film usually causes a variation of the leakage currents.[241] This interpretation received partial support from the e-beam-induced current profile at the GO/metal interface and XPS depth profiles of oxygen and metals in HRS and LRS, which displayed distinct oxygen bonding near the interface.[126,266] However, the spatial distribution of the oxygen functional groups can vary in each resistive state. Furthermore, experiments on devices with different sizes indicate that the leakage current is proportional to the cell size.[105] Therefore, both results suggest that oxygen migration plays a dominant role in the switching of GO-based RRAMs.[241]

Ref. [267] observed different switching polarities, switching modes or the absence of them depending on the active metallic electrode (Al, Cu, Ni, Ti). The switching directions are characterized by the different area, field and temperature dependences between them. Except for Ni electrodes (which did not show RS),[267] all the others (Al, Cu and Ti) showed bipolar switching under positive set (applied at the top electrode, bottom grounded).[267] Ti showed additional negative bipolar switching under negative set, and Al showed additional unipolar switching.[267] The bipolar RS under negative set might be related to the absorption/release of oxygen based functional groups,[241,268] while the bipolar RS under positive set may be associated with metallic ion diffusion.

The main performances shown by GO-based RRAMs are compared in **Table 3**. The highest I_{ON}/I_{OFF} was achieved in ITO/GO/Ag[242] and p-Si/GO/Ag[247] structures. Ag electrodes seem to provide the lowest switching voltages,[133,153,242,245] but this contrasts with the results of Ref. [251], which show operating voltages ≈6.7 V (the thickness of the GO film in Ref. [251] was ≈15 nm, while in Refs. [133,242] it was not indicated). By comparing rows 2 to 5 in Table 3,[248] it can be concluded that Cu electrodes provide higher I_{ON}/I_{OFF} than Ti, Ag and Au, probably due to the higher diffusivity of Cu atoms in the GO film, which may result in a more effective CF disruption during the reset process. It would be interesting to try ITO/GO/Cu and p-Si/GO/Ag RRAM structures. The ITO/GO/Al RRAMs from Ref. [249] show retention times >10^7, but they are still insufficient for RRAM technology (see Table 1).[2] By comparing the ITO/GO/Al RRAMs from Ref. [249] with the ITO/GO/Ag from Ref. [242] it looks like Ag electrodes cannot provide long retention (10^7 vs. 10^3), which is consistent with the lower operation voltages for Ag electrodes.[133,153,242,245] In any case, the long retention observed in Ref. [249] requires further corroboration (as well as the high operating voltages observed in Ref. [251]). The use of semiconductor electrodes in RRAMs, e.g. Si/GO/Al,[250] Ge/GO/Al[250] and p-Si/GO/AG[247] show (unwanted) high operation voltages of –5.5 V, –8.7 V and 3.5 V (respectively). While Si/GO/Al,[250] Ge/GO/Al[250] show low I_{ON}/I_{OFF} <120, p-Si/GO/AG[247] reached 10^4. Further confirmation of the results in Ref. [247] is necessary. Despite all papers

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Table 3. Switching in GO-based devices.

Device Structure	Device size	I_{ON}/I_{OFF}	Set V [V]	Retention [s]	Endurance [cycles]	Ref.
Pt/GO/Cu	100 µm in diameter	500	≈0.7	>10^4	>100	[241]
Pt/GO/Cu	100 µm in diameter	≈1250	≈0.8–1.2	>10^4	>100	[245]
Pt/GO/Ti	100 µm in diameter	≈650	≈0.8–1.2	≈10^5	>100	[245]
Pt/GO/Ag	100 µm in diameter	≈100	≈0.5–1	≈10^5	≈100	[245]
Pt/GO/Au	100 µm in diameter	≈40	≈0.6–0.8	≈10^5	>100	[245]
Si/GO/Al	600 × 600 [µm^2]	110	–5.5	10^3	≈100	[250]
Ge/GO/Al	600 × 600 [µm^2]	76	–8.7	10^3	>100	[250]
Al/GO/Al	–	10^3	0.7	–	–	[253]
ITO/GO/Al	180 µm in diameter	10^3	–1.6	10^7	>100	[249]
ITO/GO/Ag	–	10^4	–0.6 ± 0.2	>10^3	–	[242]
ITO/GO/Ag	80 µm in diameter	<10	0.6	–	–	[133]
Ag/GO/Ag	–	10	6.7	>10^3	–	[251]
p-Si/GO/Ag	≈50–150 µm in diameter	10^4	3.5	>10^3	>100	[247]
Al/GO/Au/GO/ITO	–	10^2	–	–	10^4	[243]

using spin coating reporting thick >10 nm layers,[241,245,249,250] the endurance for all RRAMs in Table 3 is just ≈100 cycles. This value, which may be related to the large number of defects (missing bonds) in the GO film,[269] is very far from the technology requirements for NVMs (10^9 cycles, see Table 1).[2] Similarly, despite all papers in Table 3 claiming that GO may be interesting for future nano RRAM devices, the RRAM size was >7500 µm^2, and we are not aware of any CAFM-based RS study (like those in Ref. [35]) for GO films. The data in Table 3 needs to be corroborated in smaller MIM cells.

The endurance can be enhanced by using RGO instead of GO, as can be observed by comparing Table 3 and **Table 4**. Ref. [262] reported unipolar RS in ITO/RGO/ITO cells (5 µm in diameter), with endurance >10^5 cycles. The replacement of one of the ITO electrodes by Au[270] did not alter the operation voltage (2V) and retention time (10^5), indicating that in these structures the RGO (not the electrode) plays a dominant role in the charge transport.[270] The use of one Al electrode in conjunction with the RGO/ITO stack does not significantly alter the switching time[260] (compared to ITO/RGO/ITO)[262] even in much larger cells (≈3 mm in diameter). When both electrodes are made of Al[271,272] the devices show much lower I_{ON}/I_{OFF} <100. This observation correlates with a reduction of the operating voltage (≈0.6 V).[271,272] The use of Pt electrodes shows high operation voltages <1.9 V and I_{ON}/I_{OFF},[273] similar to those of Au electrodes. This is reasonable because both Au and Pt are noble metals with low reactivity with GO. In agreement with these observations, RGO-based RRAMs using Al electrodes showed the smallest retention times.[260,271–274] A device with Ag electrodes showed the lowest I_{ON}/I_{OFF} (10) and endurance (100).[254]

GO and RGO can be combined with additional layers with the aim of further improving the performance of RRAMs.[194,264,275–278] Prototype RRAM cells combining ZnO–graphene quantum dots

Table 4. Switching in RGO-based devices.

Device structure	Device size	I_{ON}/I_{OFF}	Set V [V]	Retention [s]	Endurance [cycles]	Switching time [ns]	Ref.
PET/ITO/RGO+PVA+Au NP/Al	–	>10^3	0.44	>10^4	–	–	[352]
ITO/RGO/ITO	50 µm in diameter	–	2	10^5 @ 85 °C	>10^5	30 (set) 30 (reset)	[262]
Au/RGO/ITO	–	10^3	2	10^5	–	–	[270]
Al/GO/ITO	≈3 mm in diameter	10^5	–	>10^4	–	25 (set) 25 (reset)	[260]
Al/RGO/Al	–	10	–	>10^6	>100	–	[272]
Al/RGO/Al	100 µm in diameter	10^2	0.6	>10^4	>250	–	[271]
Pt/RGO–th/Pt	100 µm in diameter	>10^4	≈1.9–3.9	>10^5	>350	5 (set) 5 (reset)	[273]
Al/PFCF/RGO/ITO	0.4 mm in diameter	10^4	–1.2	10^4	10^8	–	[351]
Al/RGO-ferrocene/ITO	0.04 mm in diameter	10^3	–	10^3	10^3	–	[274]
Ag/HfO$_X$/LSG (laser-scribed RGO)	–	10	–	10^4	100	–	[254]

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(GQDs),[194] metallic (Ni,[278] Au[243]) nanoparticles and nanocrystalline cellulose/GO[277] have been reported. Ref. [194] introduced ZnO–GQDs as active components and demonstrated a solution-processed organic NVM array with one-diode-one-resistor (1D1R) architecture. The switching mechanism of the ZnO–GQDs devices was governed by thermally activated transport before the turn-on process.[194] The 1D1R cell showed typical unipolar switching and low cross-talk noise. An analogous architecture of ZnO nanorods (ZnONRs) with GO displayed a significant reduction of the operating voltages (2.1 V) compared to the cell without ZnONRs (3.9V), indicating enhanced concentration of oxygen vacancies in the GO due to the incorporation of ZnONRs.[246] Ref. [278] used Ni-incorporated GO to fabricate RRAM devices with endurance >100 cycles, and Ref. [243] combined GO with Au nanoparticles, which lead to bipolar RS with retention times ≈10^4 s.[243]

The combination of GO with polymers such as poly (N-vinylcarbazole) derived GO (GO-PVK),[275] triphenylamine-based polyazomethine (TPAPAM),[274] showed typical bistable electrical conductivity and nonvolatile rewritable memory effects, with a turn-on voltage ≈–1 V and I_{ON}/I_{OFF} >10^3. Ref. [264] presented a RRAM-based on solution-processed GO/$Pr_{0.7}Ca_{0.3}MnO_3$ forming a cell of Pt/GO/PCMO/Pt. In this structure, two active layers are necessary because GO or PCMO independently sandwiched by metal electrodes cannot reach stable RS. For example, the Pt/PCMO/Pt control sample showed no RS,[264] due to the almost Ohmic contact between each layer, and the *I–V* characteristics of a single Pt/GO/Pt device displayed an irreversible BD. However, the device with two active layers exhibited intrinsic and reversible bipolar RS, along with the conduction mechanisms associated to oxygen ions movement between the two active layers (see **Figure 11**). Three different phases can be detected from *I–V* characteristics collected in these devices: i) An initial linear behavior at low voltages. ii) A sudden current increase that switches the device to LRS, probably related to the movement of oxygen ions from GO towards the PCMO surface, which contains large amounts of oxygen vacancies compared to the bulk region. And iii) the resistance of the PCMO layer is decreased by reducing the oxygen vacancy concentration, inducing the reset and transition back to the HRS. Therefore, electrical pulses can cyclically induce a HRS to LRS transition, and vice versa.

Refs. [243,258] reported multiple stable resistive states in GO when incorporating either Au nanoparticles[243] or polyimide.[258] The presence of more than one resistive state allows for a higher information storage density as, instead of bits, multiple digits can be stored. Up to four differentiated levels and retention times of at least 10^4 s were reported.[243] The performance of RRAMs using GO, RGO-polymer and mixed structures as RS media are summarized in **Table 5**. Outstanding performance in terms of endurance (10^8 cycles) is achieved[275,276] using GO-polymer composites sandwiched by ITO–Al electrodes, approaching, but not meeting, the NVM technology requirement (10^9). These two cells[275,276] also show high retention times >10^4 s and I_{ON}/I_{OFF} ≈10^3, being only surpassed by the RGO/P3HT:PCBM/Al structures shown in Ref. [279] (10^4–10^5).

GO can also provide flexibility and transparency to the devices. For example, ITO/GO/Ag RRAMs with I_{ON}/I_{OFF} ≈ 10^3

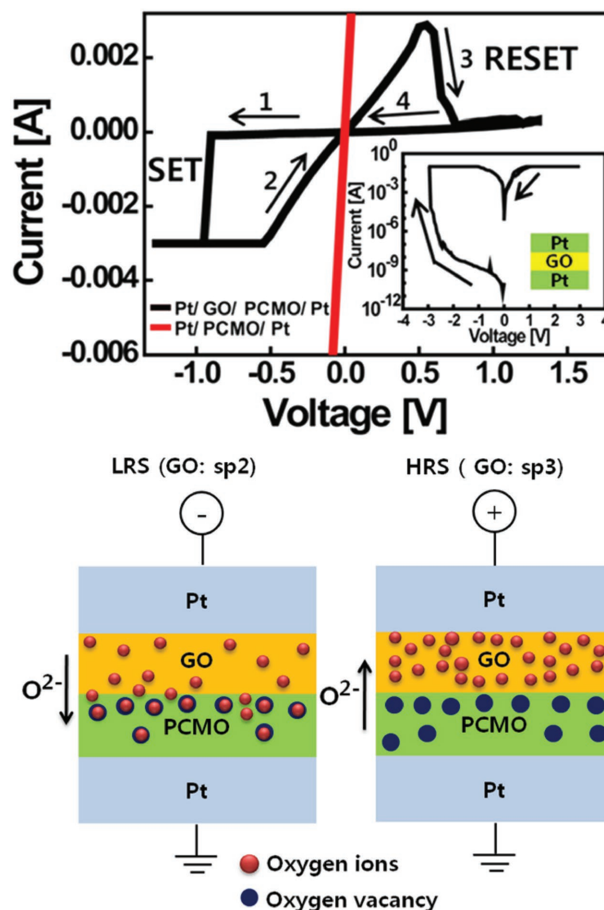

Figure 11. Typical *I–V* hysteresis curves of GO/PCMO and PCMO cells (top). The inset shows the *I–V* hysteresis for a Pt/GO/Pt device. Proposed switching mechanism in LRS (left) and HRS (right) for GO/PCMO devices (bottom). Reproduced with permission.[264] Copyright 2011, American Institute of Physics.

and stable retention characteristics for >10^3 s within 1000 cycles for r_b > 4 mm have been reported.[249] Ref. [262] fabricated RGO-based RRAMs by dip-coating, and obtained ≈80% transparency from 425 to 900 nm. These devices exhibited unipolar RS characteristics with I_{ON}/I_{OFF} >10^5, endurance ≈10^5 cycles for each state, retention times >10^5 s and multilevel capability. The performance of flexible RRAMs using GO and RGO as RS media is summarized in **Table 6**. Outstanding performance (I_{ON}/I_{OFF} >10^3, retention >10^5 s and endurance >10^3 cycles) was achieved in PEN/Ti/Pt/GO/Ti/Pt RRAMs,[280] with MIM cells ≈100 nm × 100 nm, making these values more reliable. This is an important step towards enabling future transparent device applications based on GO and its derivatives.

5. Amorphous Carbon as Switching Media for RRAMs

Non-crystalline carbons are referred to as amorphous carbons. When the sp^3 fraction is higher than 50%, these are called tetrahedral-amorphous carbons, ta-C.[281–284]

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Table 5. Switching in GO and RGO-polymer and mixed structures.

Device structure	Device size	I_{ON}/I_{OFF}	Set V [V]	Retention [s]	Endurance [cycles]	Ref.
ITO/TPAPAM-GO/Al	0.4 × 0.4 [mm^2]	10^3	–1	>10^4	10^8	[276]
ITO/GO-PVK/Al	–	>10^3	–2	>10^4	10^8	[275]
PET/ITO/PVK:Gr(GO)/Al	–	–	≈0.2–0.4	–	Not reversible	[353]
ITO/PVA+GO/Al	200 µm in diameter	10^4	–0.75	10^4	>10^4	[354]
ITO/PVDF-GO/Al	0.0004 [cm^2]	10^4	≈3.6–4.1	–	–	[355]
Al/CuO/GO/CuO/Al	–	–	3.0	–	–	[244]
ITO/PMMA/GO/PMMA/Al	30 µm in diameter	>10^3	–1.7	10^4	>10^5	[356]
Gr/GO/ZnONR/Nb	–	10^3	–	–	>50	[357]
ITO/GOAu/Al	200 µm in diameter	10^6	–1	10^4	>300	[358]
ITO/GO-FeO/Pt	–	5 × 10^3	0.9	10^5	>1100	[359]
ITO/FPA-rGO/Al	0.04 [mm^2]	10^3	1.6	>10^3	>10^3	[274]
Al/GO-PFCz-ITO	≈ 0.16–0.0225 [mm^2]	10^3	0.38	>10^4	10^8	[351]
Au/PrGODMF/ITO	–	100	–	>1000	100	[128]
Ag/PI/GO:PI/PI/ITO	–	1000	5	1400	130	[258]
Pt/GO/PCMO/Pt	–	10^2	–0.75	10^4	150	[264]
Al/PS-b.P4VP-GO/ITO	0.4 × 0.4 mm^2	10^4	≈6	>10^4	10^8	[360]
Al/P3HT:PCBM/rGO/glass	–	10^6	–	–	–	[140]
Pt/Zr:SiO*x*/C:SiO*x*/TiN	–	100	–	–	–	[268]
rGO/P3HT:PCBM/Al	–	10^4–10^5	–	–	–	[279]
PET/rGO/MoS$_2$-PVP/Al	–	≈10^2	–	–	–	[320]

Amorphous carbons can change resistance by applying unipolar electrical pulses or voltage sweeps. RS in amorphous carbons has led to their addition to the selection of emerging memory technologies in the 2014 ITRS.[2] The switching mechanism, however, is still under debate. Several mechanisms have been put forward, such as sp^2 clustering,[86,285] sp^2 filament formation,[286–289] metal filament formation[85,290] and electron trapping/detrapping.[291]

In 1972 Ref. [292] first reported RS in 10nm thick evaporated a-C films sandwiched between Al electrodes, reporting 100 000 switching cycles. Ref. [292] found that a forming step is needed to create a CF and activate RS. Switching only occurred by applying a positive voltage to the bottom Al electrode, while opposite polarity was needed for the RESET.[292] RS was attributed to metal filament formation, since Al is a diffusive metal and amorphous carbon produced by evaporation has usually very low sp^3 content and switching in sp^2 rich amorphous carbon is not reversible.[285]

Non-volatile RS in doped amorphous carbon films was demonstrated by several groups.[84–89,293–300] This includes RS in nitrogen,[88,89,295,296] hydrogen,[84–87] oxygen,[294,301] silicon,[302] Co[297] and Cu[298–300] incorporated amorphous carbon films. **Table 7** summarizes the literature RS data in doped amorphous carbons.

Table 6. Switching in GO and RGO on flexible substrate.

Device structure	Device area	I_{ON}/I_{OFF}	Set V [V]	Retention [s]	Endurance [cycles]	Switching time [ns]	Ref.
PET/ITO/GO/Al	300 µm in diameter	280	2.2	10^4	>100	–	[261]
PES/Al/GO/Al	50 µm × 50 µm	>100	–2.5	5 × 10^4	≈100	–	[126]
PES/ITO/GO/ITO	150 µm in diameter	10	≈0.7–1	10^5	–	–	[361]
PET/ITO/GO/ZnO nanorods/Al	200 µm in diameter	≈100	≈1–4.8	10^4	>200	–	[246]
PET/ITO/GO/Al	200 µm in diameter	≈100	3.9	–	–	–	[246]
PET/ITO/GO/Ag	0.026 [mm^2]	5	–0.14	≈10^3	13	–	[139]
PET/ITO/RGO+PVA+Au NP/Al	–	>10^3	–0.44	>10^4	–	–	[352]
Pt/RGO–th/Pt	100 µm in diameter	>10^4	≈ 1.9–3.9	>10^5	>350	5	[273]
Al/RGO/Al	100 µm in diameter	10^2	–0.6	>10^4	>250	–	[271]
PEN/Ti/Pt/GO/Ti/Pt	100 nm × 100 nm	–	3.5	>10^5	>10^3	<10 (set)	[280]
Al/GO/ITO	180 µm in diameter	10^3	–1.6	10^7	>100	–	[249]

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Table 7. Doped amorphous carbon-based RRAMs.

Device structure	Device area	I_{ON}/I_{OFF}	Set *V* [V]	Retention [s]	Endurance [cycles]	Switching time [ns]	Ref.
W/a-CO_x/Pt,Ti,W	100 nm in diameter	>10^2	–	10^4 @ 85 °C	>10^4	40 (set) 4 (reset)	[294,301]
Pt/a-$CN_{0.15}$/Cu	100 µm in diameter	1	0.6	>10^6	10^3	–	[295]
FTO/a-C:Co/Al	–	25	–	>10^5	–	–	[297]
Pt/a-C:Cu/Cu	0.1 × 0.1 [µm^2]	10^2	0.7	10^4 @ 85 °C	>10^3	–	[298,299]
Pt/a-C:Cu/Pt	30 × 30 [µm^2]	–	0.7	–	–	–	[300]
Pt/a-C:N/C-AFM tip	12 nm in diameter	–	3	–	–	–	[296]
Pt/a-C:Si/C-AFM tip	–	–	3.5	–	–	–	[296]

Refs. [88,89] reported a reversible NVM effect in nitrogen-doped tetrahedral amorphous carbon, ta-C:N, with write times down to 100 µs.[90] They attributed the switching to the promotion of electrons from acceptor states in the gap to higher donor states. However, the LRS retention was poor, only one year,[90] too short for commercial applications. Ref. [295] prepared nanoporous nitrogen-doped amorphous carbon and studied a Pt/a-C:N/Cu device structure. Set and reset occurred at opposite voltage polarities.[295] Decreasing the amount of nitrogen led to a reduction of switching voltages to +0.6 V for set and –0.5 V for reset.[295] Over 1000 switching cycles and a retention >80 days at room temperature were reported, still not good enough to meet industry requirements.[295] The switching mechanism was attributed to the formation and rupture of Cu filaments.[295] Ref. [296] reported the effect of nitrogen implantation on RS of amorphous carbon to analyze the role of sp^2 filamentation and clustering. Nitrogen implantation made the films more conductive with an increase in sp^2 bonding and clustering, facilitating the SET process.[296]

Several groups reported reversible, non-volatile switching in hydrogenated amorphous carbon, a-C:H,[85–88] with the results summarized in **Table 8**. RESET within 30 ns and SET in ≈30 ns were reported,[86] long data retention >10^5 s,[85] 10^7 switching cycles[87] and I_{ON}/I_{OFF} ≈10^3.[86] The RS mechanism was attributed to different processes: Ref. [85] assigned RS in Pt/a-C:H/metal structures, with the metal top electrode being Cu, Ag or Au, to the formation and rupture of metal filaments, due to diffusion of the top electrode metal into the a-C:H film.[85] Ref. [86] studied RS in a-C:H with TiN as bottom and Cu, Pt or W as top electrodes, and assigned RS to thermally induced conductive sp^2 clusters filament formation.[86] Ref. [87] attributed the switching to a sp^2 carbon CF formation in a TiN/a-C:H/Pt structure. RESET was achieved by applying the opposite voltage polarity to the bottom TiN electrode and attributed to hydrogen atoms pulled from the Pt top electrode and absorbed by double bonds in sp^2 carbon.[87]

A limiting factor in a-C:H RS is the need of a forming step, where the material needs to be biased at the breakdown electric field.[303] The breakdown results from a capacitive discharge current, which can be 10–20 mA[86,303] and occurs within a few ns.[86,303] Therefore, an on-chip resistor or transistor is needed to limit the current during forming.[86,303] Due to the high current density during the forming step, metals from electrodes might diffuse into the carbon, if the forming is done in a dc-sweep, instead of an energy-limiting short pulse.[85,287,295,303]

The influence of other dopants, such as Co and Cu, was reported by various groups;[297–300] see Table 8. Ref. [297] studied RS in Co-doped amorphous carbon. They observed non-volatile, bipolar and reversible RS with I_{ON}/I_{OFF} ≈25, but good retention >10^5 s at room temperature.[297] RS was attributed to a filament formed by Co ions created by an electrochemical reaction, migrating toward the top Al electrode through defects in the a-C film, forming a conductive path between top and bottom electrode.[297] Other groups[298–300] investigated RS in Cu doped carbon. They obtained I_{ON}/I_{OFF} ≈ 10^2 and retention of 10^4 s at 85 °C and >10^3 switching cycles.[298] Ref. [300] used a slightly different device configuration with both top and bottom electrodes made of Pt. A forming step was needed. Subsequent set and reset processes could be achieved at ≈+0.7 V and –0.5 V.[300] RS was attributed to the formation and rupture of Cu filaments.[298–300]

Ref. [294] prepared oxygenated amorphous carbon, a-CO_x, by physical vapour deposition. Ref. [294] reported switching times ≈40 ns for SET and ≈4 ns for RESET, with opposite voltage polarity needed.[294] Ref. [294] measured cycling endurance >10^4 in devices with W as bottom and Pt, Ti or W as top electrodes,[294] with I_{ON}/I_{OFF} ≈5 × 10^2 during retention measurements up to

Table 8. Hydrogenated amorphous carbon-based RRAMs.

Device structure	Device size	I_{ON}/I_{OFF}	Set *V* [V]	Retention [s]	Endurance [cycles]	Critical field [V cm^{-1}]	Switching time [ns]	Ref.
Cr/a-C:H:(B)/Au	–	10^2	–	–	–	5 × 10^5	–	[84]
Pt/a-C:H/Cu (Ag orAu)[a)]	100 µm in diameter	>100	1.1	>10^5	110	–	–	[85]
TiN/a-C:H/Cu (Pt, W)[b)]	49 ± 11 nm in diameter	>10^3	4.1	57 600	15	–	30 (set) <30 (reset)	[86]
TiN/a-C: H/Pt	0.36 to 16 [µm^2]	100	1.5	10 000 @ 85 °C	10^7	–	–	[87]

[a)]The Cu electrode was also replaced by Ag and Au, and the resulting devices also show resistive switching. I_{ON}/I_{OFF} and switching threshold voltages (*V*) vary as follows: I_{ON}/I_{OFF} (Cu) > I_{ON}/I_{OFF} (Ag) > I_{ON}/I_{OFF} (Au) and $V_{Cu} > V_{Au} > V_{Ag}$; [b)]This report used devices with Cu, Pt or W electrodes. It is unclear which electrode corresponds to the performances indicated.

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Table 9. ta-C- and a-C-based RRAMs.

Device structure	Device size	I_{ON}/I_{OFF}	Set V [V]	Retention [s]	Endurance [cycles]	Critical field [V cm^{-1}]	Switching time [ns]	Ref.
n-Si/a-C/C-AFM tip	–	10@80 K	5	3000	20	–	–	[307]
TiN/a-C (sp^{2}rich)/C-AFM tip (PtSi)	≈20 –30 nm in diameter	–	≈1–2	–	Not reversible	–	–	[285]
Pt/ta-C/C-AFM tip	8.5 nm in diameter	–	12V pulse amplitude	–	–	–	5 (set)	[296]
W/ta-C/W	150 nm in diameter	>10^3	≈1–3	–	2.3×10^{13}@75 °C	–	10 (set) 1 (reset)	[286]
Ag/a-C/CNT	0.001 [μm^2]	40–200	≈5.4 –7.5	>10^6	31	–	–	[290]
Al/a-C/Cu	–	3	<3	10^5	–	–	–	[291]
Al/ta-C/W	2500 [μm^2]	10	<1	>10^5	120	–	–	[287]
Pt/a-C/Cu,Ag	50×50 [μm^2]	–	0.18@0 K	10^4@85 °C	–	–	–	[306]
Pt/a-C/Cu	500 μm in diameter	100	0.1	10^8	–	–	–	[304]
Pt/a-C/Cu	100 μm in diameter	>70	1	–	110	–	–	[305]
Pt/ta-C/W	50–500 nm in diameter	>300	0.8	–	–	5×10^7	50 (set) 4 (reset)	[288,289,301]

10^4 s at 85 °C. The RS mechanism was attributed to an electrochemical redox reaction leading to the formation of a conductive carbon filament.[294] The choice of metal electrode material was crucial for the reset process, with strong dependence on the electron affinity of the metal electrode.[294] To make the reduction reversible, two electrode materials were needed to store and release oxygen. One with similar electron affinity to carbon, such as W, and the other with higher electron affinity, such as Pt.[294]

RS in amorphous carbons with different sp^2/sp^3 ratio was reported by several groups.[285,304–312] RS in sp^2 rich a-C was studied in a Si/TiN/a-C devices, using a CAFM as top contact.[282] The key parameters of RS devices based on a-C/ta-C are reported in **Table 9**. RS was assigned to an electrothermally (Joule heating) induced increase in the sp^2 cluster size and was non-reversible.[285] RS in a-C was shown to be polarity independent.[304–307] Ref. [306] studied the influence of the top metal electrode material on RS, and assigned this to metal filamentation in devices with Cu top electrodes. Pt, W and Ni top electrodes did not show switching.[306] This was attributed to the less diffusive nature of those metals.[306] Data retention> 10^5 s,[304] low switching voltage of 0.18 V[306] within pulses of 1 μs,[306] I_{ON}/I_{OFF} ≈70,[305] endurance ≈110[305] and device structures down to 50×50 μm^2[306] were demonstrated.

I_{ON}/I_{OFF} and endurance are the main challenges faced by RRAMs based on a-Cs. The issue of a low I_{ON}/I_{OFF} can be overcome by using ta-C. Ref. [308] demonstrated high I_{ON}/I_{OFF} in Pt/ta-C/(SLG)/Au devices. Devices with an interfacial SLG reached I_{ON}/I_{OFF} ≈4×10^5 at 0.2 V, while maintaining low switching power density of 14 μW μm^{-2}.[308] This was attributed to the reduction of leakage currents due to the low SLG density of states near the Dirac point.[308] Refs. [288,289] explained the switching in terms of nanoscale sp^2 filament formation and rupture through field-induced dielectric breakdown and thermal fuse effect, i.e. an electrothermally driven set process and a thermally driven reset process. Low switching voltages of 0.4V for RESET within 10 ns and 1.2V for SET within 50 ns,[288] 10^{13} read cycles at 75 °C,[286] >10^6 s retention[290] with device sizes of 50 nm diameter[289] and 10^3 switching cycles[288] were also demonstrated. The presence of multiple resistive states was reported by Ref. [308]. Multilevel storage is of particular interest as it allows to store more than one bit per cell, while the memristive behavior can be exploited to provide a range of signal processing/computing-type operations, such as implementing logic, providing synaptic and neuron-like mimics, i.e. circuits that simulate brain-like neurological functions, and performing analogue signal processing functions, paving the way for non-von-Neumann architectures, in which processing and non-volatile storage are carried out simultaneously.[313,314]

Endurance is one of the major challenges for a-C based switching devices. A comparative study by Ref. [301] of RS in ta-C and a-CO$_x$ with Pt bottom electrodes and W top electrodes suggested that, by incorporating oxygen, the endurance could be enhanced to 40 000, but at the expense of bipolar operation.[301] In ta-C devices, SET and RESET were achieved with pulses of 50 and 4 ns and switch energies of 15 and 3pJ, while a-CO$_x$ could be set and reset with 40 and 4 ns pulses with switch energy of 2 and 1pJ, respectively.[301] Both, ta-C and a-CO$_x$ showed good data retention of 10^4 s at 85 °C.[294,301]

Several groups[301,302,311,312] theoretically studied the switching mechanism in amorphous carbons, and assigned RS to heat driven sp^2 clustering and filament formation.

Ref. [303] pointed out that one of the biggest advantages of carbon-based memory devices might be the high temperature retention ≈250 °C, making them attractive for automotive and harsh conditions.[303] Another advantage of carbon-based memories is that devices do not rely on rare mineral extraction, with easier disposal/recycling, and low total energy production compared to other electronics materials.[280]

6. Layered Materials

Non-carbon-based LMs have also been introduced into the structure of RRAMs, mainly TMDs (like MoS$_2$[315,316] and

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$MoSe_2$[317]) and h-BN.[163] Ref. [318] reported a RRAM prototype using BP flakes.

TMDs are naturally semiconducting materials,[319] thus they are not ideally suited for RRAMs. For this reason, they need to be functionalized in order to form an insulating layer.[319] Ref. [320] suggested to combine TMDs with an insulator (such as polymers) whereby the TMD would act as dopant of the insulating layer. In Ref. [320], a stack of RGO/MoS_2-PVP/Al in which the PVP (polyvinylpyrrolidone), typically used to assist the exfoliation of MoS_2, became the dielectric RS-driving layer. The devices were fabricated using spin coating of the MoS_2-PVP solution on the RGO film, resulting on a thickness of 70 nm, and large 0.2×0.3 mm^2 electrodes were thermally evaporated. The RRAM devices show $I_{ON}/I_{OFF} \approx 10^2$. Ref. [320] claimed the switching was due to charge trap and de-trap of the MoS_2 embedded in the PVP. However, others[321,322] reported RS also in structures with pure PVP as active layers, while Ref. [273] detected RS in RGO. We note that Ref. [320] did not provide temperature nor area analyses, which makes it difficult to discern if the RS in these devices is a local or distributed phenomenon. Therefore, the ability of MoS_2 to drive the RS is questionable.

Similar studies were developed by Ref. [323] in a PET/Al/PMMA/MoS_2/PMMA/Al stack and by Ref. [324] for Au/MoS_2-PMMA/SLG. These have $I_{ON}/I_{OFF} \approx 10^4$ and 2.5×10^3, respectively. However the need for a TMD to be combined with PMMA is doubtful. Ref. [325] demonstrated that MoS_2-free Ag/PMMA/ITO devices can also achieve reproducible RS ($I_{ON}/I_{OFF} \approx 10^2$), which is driven by the penetration of metallic ions into the polymer, leading to a reversible CF through it. The combination of MoS_2 and GO resulted in a similar $I_{ON}/I_{OFF} \approx 10^2$ for a RRAM device.[326] Ref. [327] produced printable RRAM memories with tuneable performances using Ag/MoS_2-MoO_x/Ag stacks, with $I_{ON}/I_{OFF} > 10^6$, retention times >8000s, and non RS degradation after bending >10^4 times. As in Refs. [324,326], the RS in Ref. [320] does not seem to be attributable to the MoS_2 sheets, which served to homogenize the interface between the MoO_x and Ag bottom electrode. A different approach was reported by Ref. [328], who used MoS_2 flakes, also giving RS. In this case, the resistance changes were attributed to tunnelling across junction barriers. Very similar devices, but using $MoSe_2$ nano-islands, were studied by Ref. [317], which showed $I_{ON}/I_{OFF} \approx 12$ and low currents (>1 µA) in the LRS.

RS driven by MoS_2 was reported by Refs. [315,316]. Ref. [317] used three-terminal horizontal devices similar to FETs (see **Figure 12**a and b), with a grain boundary (GB) in the MoS_2 extending in the channel. Ref. [320] considered different GB configurations, including parallel and perpendicular to the channel, as well as intersecting. In all cases, $I_{ON}/I_{OFF} > 10^2$ was achieved. RS in these devices was assigned to the motion of S vacancies in the MoS_2, which tend to accumulate at the GBs.[320] However, the reproducibility of this phenomenon was not firmly established, as Ref. [315] reported only 15 cycles. On the other hand, Ref. [316] compared two vertical Ag/MoS_2/Ag devices using a 550-nm MoS_2 film formed by MoS_2 flakes dispersed in propanol and spin-coated on a Ag foil, followed by a thermal treatment at 130 °C for 12h and 0.1 mm^2 top electrode deposition using Ag paste (Figure 12c and d). The differences between the two devices was the MoS_2 phase, in one case 1T flakes, and in the other 2H bulk. Despite the methodologies not being ideal for scaling and integration (deposition of electrodes by Ag paint using a shadow mask is to be avoided because it can lead to contaminants at the interface, inhomogeneous shapes and cracks) the devices using 1T-MoS_2 showed good RS behaviour with $I_{ON}/I_{OFF} > 10^3$ during 100 cycles. Ref. [316] assigned RS to the migration of Mo and S ions under electrical field. Ref. [316] also included a modification of this device using Ag/MoS_2/Ag/MoS_2/Ag vertical structures, showing the possibility of reducing the current at low voltages (<0.2 V) by negative differential resistance, which may be useful to avoid sneak path

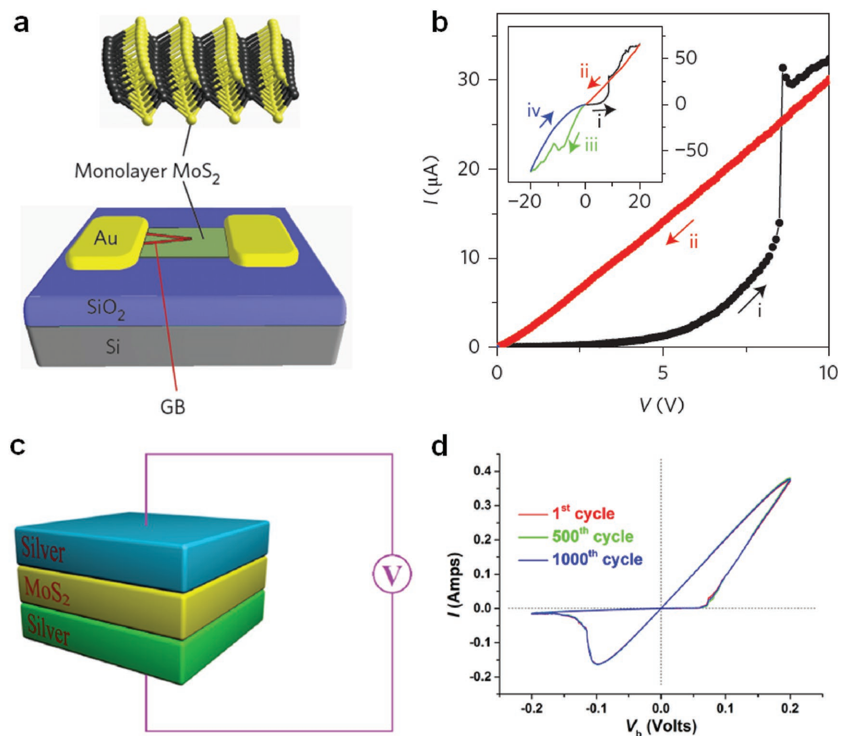

Figure 12. a) Schematic horizontal MoS_2 RRAM cell with two GBs connected to one of the electrodes and intersecting at a vertex within the channel. b) Partial I–V characteristics of an electroformed intersecting-GB memristor (channel length, L = 7 µm) obtained immediately after electroforming. The set process occurs at V_{set} = 8.3 V with an abrupt twofold increase in current. Inset: Full I–V characteristics of one switching cycle. Measurements were performed at a sweep rate of 1 V s^{-1} and V_g = 40 V under vacuum (pressure < 2×10^{-5} torr). The voltage was swept in the order 0 V → 20 V → 0 V → −20 V → 0 V, as shown by the coloured arrows with the four sweeps labelled i, ii, iii and iv. Reproduced with permission.[315] Copyright 2015, Macmillan Publishers Limited. c) Schematic structure of vertical Ag/MoS_2/Ag RRAM cell. d) Typical I–V characteristic of Ag/MoS_2/Ag switch at the 1st (red), 500th (green), and 1000th (blue) cycle at room temperature. Reproduced with permission.[316] Copyright 2015, American Chemical Society.

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Table 10. TMD-based RRAMs.

Device structure	Fabrication method	I_{ON}/I_{OFF}	Retention [s]	Endurance [cycles]	Power consumption [μW]	Transparent	Flexible	Ref.
PMMA-MoS_2/MLG/SiO_2/Si	CVD (Transfer)	2.5×10^3	–	–	–	NO	NO	[317]
Ag/$MoSe_2$/FTO	Hydrothermal	12	>50	–	–	NO	NO	[315]
Au/MoS_2/SiO_2/Si	CVD	10^3	–	–	–	NO	NO	[326]
Ag/MoS_2/Ag	LPE (spin coating)	10^3	–	10^3 a)	–	NO	NO	[316]
Ag/MoS_2-MoO_x/Ag	Modified Langmuir–Blodgett	$>10^6$	–	>8000	10 nW	NO	YES	[327]
Al/MoS2-GO/ITO	LPE (spin coating)	10^2	–	–	–	NO	NO	[326]
RGO/ZIF-8 coated MoS_2/RGO	LPE (spin coating)	7×10^4	1.5×10^3	–	–	NO	YES	[362]
RGO/MoS_2-P123/RGO	LPE (spin coating)	5.5×10^2	4×10^3	>50	–	NO	NO	[363]
PET/RGO/MoS_2-PVP/Al	Polymer-assisted exfoliation	$\approx 10^2$	–	–	–	NO	YES	[320]
RGO/MoS_2/ITO/Si	Hydrothermal	10^4	5.5×10^3	–	–	NO	NO	[328]

a)This value is not well supported in Ref. [316]. The authors only show the 1st, 500th and 1000th *I–V* curves, and no *R* vs Cycle or Weibul plot is shown. The top electrodes of the devices in Ref. [316] are made by drying Ag paint on spin-coated MoS_2 using a shadow mast. More work is needed to confirm these performances.

currents in crossbar arrays. Nevertheless, none of the MoS_2-based works to date presents a conclusive memristive analysis. For example, Ref. [316] claimed 1000 cycles, but no variability analyses (like those, for example, in Refs. [315–317,324]) were presented (just 3 *I–V* curves are displayed). More information on the different TMDs-based RRAMs is in **Table 10**, including dependence on critical parameters, such as device area, working temperature, top electrode material and current limitations (among others). The RS parameters are still far from those reported for state-of-the-art TMO-based RRAM memories (see Table 1).[2,31–33]

The use of *h*-BN in RRAMs is even more incipient. In principle, as h-BN is an insulator,[163] if a reversible CF/BD can be induced through it, the RS behaviour should be more accentuated (larger I_{ON}/I_{OFF}) due to the larger resistivity in HRS (the constriction would be more insulating than in semiconducting materials). Nevertheless, this is in principle not an easy task, as the BD may become irreversible depending on the atomic structure of the *h*-BN stack. One should clearly distinguish between research articles using layered *h*-BN[163] (see **Figure 13**c and d), and those in which amorphous BN was used (Figure 13a and b).[329] Ref. [329] claimed the fabrication of RRAMs using multilayer *h*-BN stacks, but the layered nature of the film is not supported by the cross-sectional TEM images, and the layer looks more like an amorphous BN film (see Figure 13a and c). This is very important because amorphous BN may not hold the properties of the *h*-BN stack, such as transparency,[330] flexibility,[331] high thermal conductivity[332] and high chemical stability.[333] Ref. [316] fabricated a family of RRAMs using *h*-BN as RS medium. By tuning the *h*-BN stack thickness and the *h*-BN domain size, Ref. [163] achieved forming-free operation, low switching voltages down to 0.5 V, high I_{ON}/I_{OFF} up to 10^6, retention times >10 hours and low device-to-device variability (i.e. deviations of V_{SET}/V_{RESET} <10%). In Ref. [163] the RS was attributed to the migration of B atoms towards the electrodes, as well as metallic ions penetration into the *h*-BN stack to form and disrupt one/few CFs. These atomic diffusions are more abundant at GBs, which are defect-rich locations (missing bonds, missing atoms, pentagonal/heptagonal lattices)[334,335] that can favour atomic rearrangements at lower potentials (compared to the grains), leading to a softer BD that may be easier to recover. The formation of B-vacancies at the GBs of polycrystalline *h*-BN stacks (see Figure 13c) presents an interesting parallelism to O vacancies at the GBs of polycrystalline TMOs. The key role of GBs in the RS is supported by the fact that the BD process in single crystalline *h*-BN flakes is an irreversible phenomenon that leads to the removal of the material,[336] with the formation of holes during a characteristic layer-by-layer BD process. Therefore, it is unlikely that a perfect single crystalline *h*-BN would offer RS capabilities. Ref. [107] investigated a RRAM comprising a monolayer CVD-grown *h*-BN flake inserted between the top electrode and the dielectric of an Al/WO_3/Al cell, but the performance was worse than the *h*-BN- free counterpart (I_{ON}/I_{OFF} < 10). This is likely because it is difficult to create CFs in *h*-BN/WO_3 superstructures, i.e. the CF is only created at large electrical fields that produce the irreversible BD in the *h*-BN/WO_3 stack. Ref. [337] reported indications of RS in layered Ti/*h*-BN/Cu stacks (Figure 13d). The devices exploited the Cu substrate used to grow the *h*-BN as bottom electrode, avoiding the need for transfer.[316] When applying constant voltage stresses (CVS) at 2.5 V to the devices, the current vs. time (*I–t*) curves show sudden changes of the electronic resistance (up to 10^3) similar to unipolar RS characteristics.[337] A detailed comparison of the RS capabilities of *h*-BN-based devices in literature is presented in **Table 11**. Ref. [338] also observed unipolar RS transitions in planar nanogap-based *h*-BN obtained by MC. However, thus far, the use of planar structures in RRAM technology is limited due to the difficulty in controlling the rupture kinetics of the nanogaps, which may result in poor RS endurance and device-to-device variability. We note that statistical information of RS in planar devices made of any GRM has not yet been reported. Moreover, MC is not a scalable technique. Ref. [337] reported layer-by-layer BD at the grains by means of CAFM,

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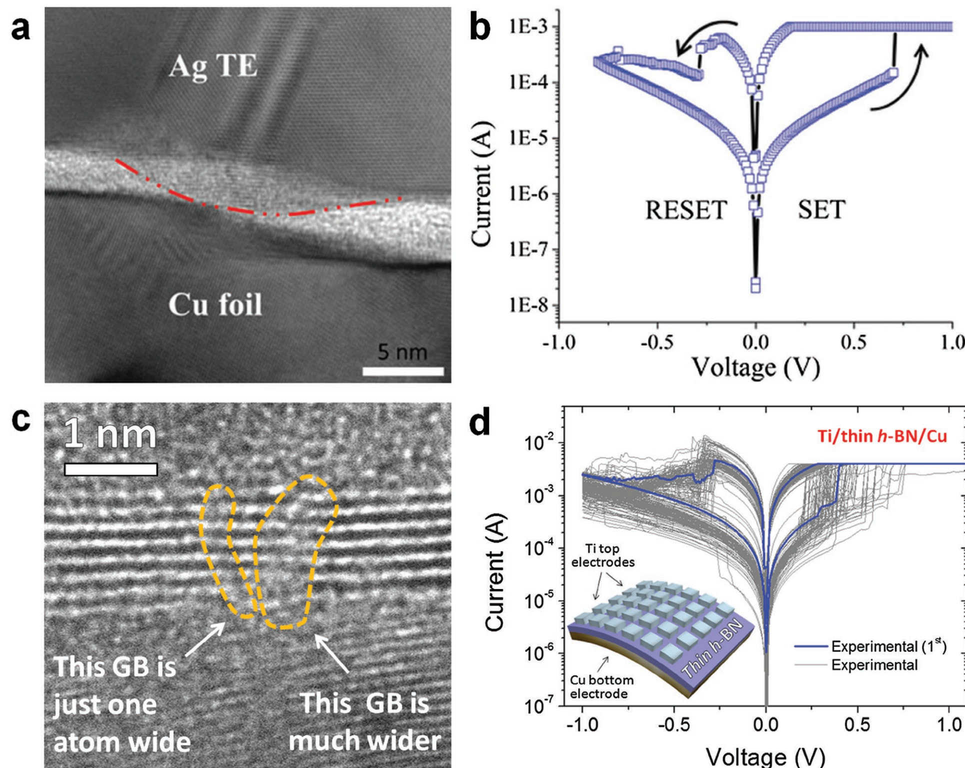

Figure 13. a) TEM image of a CF in amorphous BN. The thinnest region of the CF is at the amorphous BN/Cu foil interface. b) Switching characteristics of Au/amorphous BN/Cu foil/PET devices. Reproduced with permission.[329] Copyright 2016, Wiley-VCH. c) Cross-section TEM image of Ti/*h*-BN/Cu stacks. d) *I*–*V* curve collected in a Ti/*h*-BN/Cu (5–7 layers thick). Reproduced with permission.[163] Copyright 2016, Wiley-VCH.

while at the same time measuring reproducible conductivity changes at the device level, which may be related to the presence of GBs. As the use of LM-dielectrics provides a flatter interface to graphene and TMDs than high-k dielectrics,[179,180] RS applications of *h*-BN should be deeper investigated.

BP is a layered semiconductor prone to degradation when exposed to atmosphere.[339] The degradation of the surface is generated by the insertion of oxygen groups, leading to a PO_X structure.[339,340] This layer provides RS, as reported by Ref. [318]. They exfoliated BP using both γ-butyrolactone and isopropanol and the devices were fabricated by spin-coating on a ITO/PET flexible and transparent substrate, followed by top circular (500 µm in diameter) Ag electrode deposition by magnetron sputtering using a shadow mask. They observed that, after some days/months of exposure to atmosphere, reproducible RS with I_{ON}/I_{OFF} up to 10^3–10^4 could be achieved (**Figure 14**). They attributed this to the formation of Ag conductive filaments across the oxidized and insulating PO_X superficial layer. However, Ref., [318] was just a proof-of-concept, lacking important RRAM parameters, specially variability. Ref. [119] reported the observation of RS in (PET)/Au/BPQD-PVP/Ag structures, with $I_{ON}/I_{OFF} > 10^4$ and endurance >1100 cycles. Both BP-based RRAM devices[119,318] were fabricated by LPE and spin coating and showed flexibility. The characteristics of these two prototypes are summarized in **Table 12**. None of these works show endurance analyses. They concentrate on the proof-of-concept and I_{ON}/I_{OFF} ratio, which makes it difficult to know the real usefulness of this material in RRAMs.

7. Discussion, Challenges and Prospects

The most advanced RRAMs use MIM structures formed by metallic electrodes (Ti, Au, Ag, Cu, Ni, Pt) coupled with TMOs (HfO_2,[39–42] Al_2O_3,[43–46] TiO_2[47–50] and TaO_X).[51,52] RS in metal/TMO/metal structures was first observed in 1962,[341] and RS-based memories were proposed in 1967.[342] After more than 50 years of research, devices with high operation speeds (≈300 ps per transition),[32,44,45,60] low power consumption (≈0.1 pJ per transition),[32,44] good endurance (above 10^{12} cycles),[33,111,346,347,364] long data retention times (above 10 years),[46,364] small size (down to 10 nm × 10 nm),[31,296] and high integration capacity (>1 × 10^{11} bits cm^{-2})[2] have been developed. GRMs were firstly introduced in the structure of RRAMs in 2008,[103] and in less than a decade the performance of some GRM-based RRAMs prototypes fits some of the NVM technology requirements (low operation voltages <1 V,[163,251] high switching speeds down to 1 ns,[273,280,286] endurance >10^9 cycles,[286] and small cell size (8.5 nm^2).[296]

Table 1 compares the best performances reported for TMO-based and GRM-based RRAM devices. These are similar for both types of RRAMs, and in one case (endurance) one GRM-based RRAM achieved record values. Several GRM-based RRAMs showed low (<1 V) operating voltages,[163,248,253] and acceptable switching speeds.[273,280,286] In contrast, the number of TMO-based RRAMs that fit at least one technology

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Table 11. *h*-BN-based RRAMs.

Structure	Fabrication method	Bipolar RS under positive set	Forming process needed	V_{SET} [V] I_{SET} [A]	V_{RESET} [V] I_{RESET} [A]	I_{ON}/I_{OFF}	Endurance cycles	Retention time	Bipolar RS Under negative set	Threshold RS	Ref.
Ti/hBN/Cu	CVD (no transfer)	YES	NO	0.4 V 4×10^{-4} A	–0.3 V 4×10^{-3} A	10	>350	–	NO	YES	[163]
Ti/hBN/Cu	CVD (no transfer)	YES	NO	0.7 V 4×10^{-6} A	–0.7 V 10^{-2} A	10^4	>600	–	YES	YES	[163]
Ti/hBN/CuNi	CVD (no transfer)	YES	YES	0.7 V 4×10^{-3} A	–0.4 V 2×10^{-2} A	15	–	–	NO	NO	[163]
Ti/hBN/CuNi	CVD (no transfer)	YES	YES	6 V 10^{-3} A	–2 V 10^{-1} A	10^6	–	–	YES	NO	[163]
Ti/hBN/ITO	CVD (transfer)	YES	NO	0.4 V 2×10^{-4} A	–0.3 V 10^{-3} A	10	>180	–	NO	NO	[163]
Ti/MLG/hBN/MLG/Au	CVD (transfer)	YES	YES	2.3 V 10^{-3} A	–0.6 V 4×10^{-2} A	10^3	>450	4×10^4 s	NO	NO	[163]
Al/hBN/WO_3/Al	CVD (transfer)	–	–	–	–	<10	≈80	3×10^4 s	–	–	[107]
Ag/hBN/Cu/PET[a)]	CVD (no transfer)	–	YES	–	–	100	550	3×10^3 s	–	–	[329]
Au/Ti/hBN/Cu[a)]	CVD (no transfer)	–	YES	–	–	–	>100	–	–	–	[329]
Au/Ti/SLG/hBN/SiO_2/Si	MC	–	–	–	–	10^3	–	10^5 s	–	–	[338]

[a)]The layered structure of the BN in Ref. [329] is not well supported. From their cross-sectional TEM it looks like amorphous hBN (see Figure 13a).

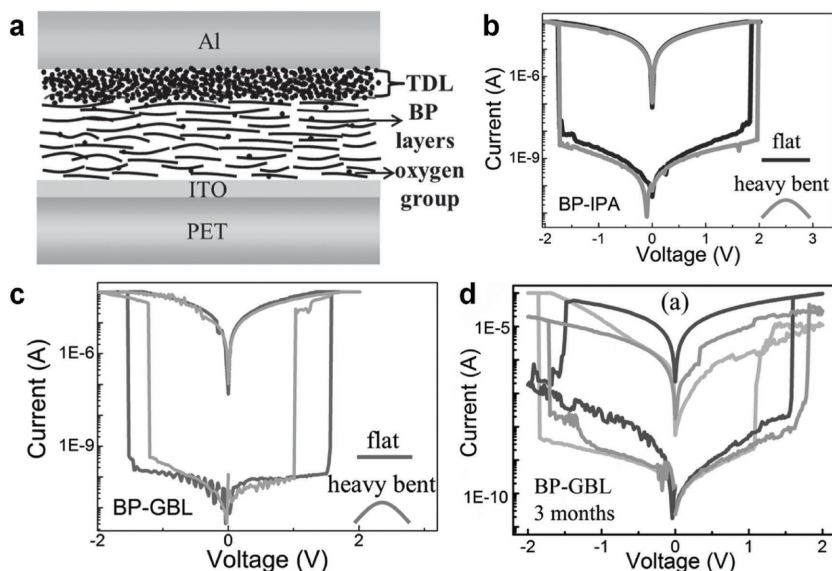

Figure 14. a) Schematic illustration of RRAM-BP cross-section. *I–V* characteristics for the RRAM-BP device for b) BP-IPA, and c) BP-GBL, in flat and bent conditions. d) Typical *I–V* curves obtained for repeated voltage sweeping cycles in the RRAM-BP devices fabricated with BP-GBL. Reproduced with permission.[318] Copyright 2016, Wiley-VCH.

requirement is much larger (Table 1 only displays a selection of them). Therefore, more work in the direction of GRMs-based RRAMs is necessary.

7.1. Fabrication

The fabrication methods used for GRMs-based RRAMs should be improved. For example, one of the best endurances reported for RRAMs exploiting non-carbon GRMs (10^3 cycles in Ag/MoS_2/Ag)[316] was observed using Ag foils as bottom electrode, and top electrodes deposited with Ag paint and MIM cell size ≈0.1 mm^2. These processes/parameters are not compatible with industry, and the knowledge extracted from such works may not be applicable to ultra-scaled (state-of-the-art) RRAMs. Future work in GRMs-based RRAMs should concentrate on the use of industry-compatible methodologies (e.g., for the deposition of electrodes

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Table 12. BP-based RRAMs.

Device structure	Fabrication method	I_{ON}/I_{OFF}	Retention time	Transparent	Flexible	Ref.
Al/TDL/BP/ITO/PET	LPE (spin coating)	$\approx 3 \times 10^5$	10^5 s	NO	YES	[318]
(PET)/Au/BPQD-PVP/Ag	LPE (spin coating)	6×10^4	1100 s	NO	YES	[119]

evaporation/and/or sputtering are preferred) and smaller device sizes (so that they can be applicable to nanosized devices).

Furthermore, in most works using transferred SLG as interface electrode (see, e.g, Table 2) the device size is very large (>8000 µm^2). Under such large areas, it is common that SLG layers show cracks, especially after transfer.[168,169] As the transversal electrical resistance of the MGI junction (non-cracked region) is larger than that of the MI one (at the cracked region),[170,171] and because the forming/BD is a stochastic process that takes place at the electrically weakest location of the area under stress (less insulating),[343,344] CFs in these devices are more prone to be formed at SLG cracks. Moreover, as the currents measured through the devices (especially in LRS) are mainly driven by the CFs, the *I–V* characteristics of many RRAMs using transferred SLG may refer to these nanosized MI junctions, and they may not be representative of the MGI structures under study. Ref. [217] reported that the insertion of SLG electrodes in TMO-based RRAMs reduces the HRS current by 1–3 orders of magnitude due to an increase of the out-of-plane resistance (non-cracked regions). Since the endurance and retention times are related to the CF properties, the presence of cracks should have a major influence. Future works using transferred SLG should prove that no cracks are present. One route could be to reduce the device area, which lessens the probability of finding a crack. Another option is to use MLG, which presents fewer cracks and is more resistant to mechanical fractures during transfer.[163]

Many GRMs-based RRAMs works based on polymer-scaffold-assisted transfer did not evaluate the presence of residues on the GRM surface after polymer removal. These may decrease the device size, given their higher thickness >10 nm and insulating nature.[345] This process is random, but can be reduced by using better cleaning processes,[172] which may result in device-to-device variability.[135–137] Future works should include nanoscale surface characterization techniques, such as topographic AFM maps. Including annealing treatments after transfer to remove rests of polymer may be an option.

Therefore, GRM transfer should be avoided when possible, not only due to device performance concerns, but also because it slows down the fabrication process (making it more expensive). The ideal solution would be to develop transfer-free processes, but the direct growth of GRMs on TMOs is a longer term goal. The use of insulating LMs as RS medium is preferred because, first, they do not need transfer,[163] and, second, the absence of cracks can be corroborated by the observation of a forming and/or set process.[329] Recent works on CVD-grown *h*-BN report transfer-free RRAM devices,[163,329] but they still use metallic foils. The direct growth of GRMs by CVD (or any other scalable technique) on metal coated flat wafers is highly desirable. Another option is to use LPE GRM insulators that can be spin coated on arbitrary substrates, but that may present variability, given their large roughness (typically ≈20 nm),[134] much larger than flat GRMs prepared by CVD. The use of coating methods that reduce the roughness below 1 nm is necessary. Note that the roughness of TMOs for RRAM (usually grown by ALD) is ≈0.2 nm. [35,62,135]

7.2. Characterization

Many papers on GRM-based RRAMs only focus on RS proof-of-concept, showing acceptable >10^2 I_{ON}/I_{OFF} in very large >1 mm^2 devices.[196,316] Information on the number of devices tested in each work and variability analyses is missing. Usually the reports do not concentrate on the study of the technology requirements (note that high I_{ON}/I_{OFF} is not a technology requirement, i.e. just one order of magnitude is enough to reliably distinguish HRS and LRS).[2] For example, we did not find GRM-based RRAM works giving the power consumption in units of energy (Joules) per transition, which is what is demanded by industry.[2] Similarly, most GRM-based RRAMs works do not focus enough on the switching times (e.g. detailed zoomed in plots at the set/reset transition are often missing). Sometimes, endurance and retention plots are shown, but the values (<10^3 cycles[351] and >10^7 s,[249] respectively) are still insufficient to meet industry requirements.[2] The only paper showing excellent switching times and power consumption (Ref. [286], Table 1) comes from industry. Future works should study several device parameters, such as RS medium thickness, electrode material and CL, as well as provide information on endurance, retention, temperature, and variability analyses performed with a probe-station, as well as modelling and CAFM. The use of CAFM to demonstrate the switching between HRS and LRS in some GRM-based reports is very deficient, as no statistical analyses of the current/size of the CFs are provided. The methods for a correct characterization of RS using CAFM are described in Ref. [35]. Similarly, the structure of LMs-based RS is often not well supported, as explained in Figure 13. Furthermore, the electrical stresses applied to most devices (*I–V* curves) are suitable only for proof-of-concept, but real devices work under fast (<10 ns) voltage pulses.[34]

Many GRM-based RRAM reports do not present variability analyses (just typical values are shown), which raises concerns on the reliability and reproducibility of the results. Device-to-device variability was rarely reported (see, for example, Ref. [163]). In the future, more information about the dispersion of V_{SET} and V_{RESET} in groups of more than 20 devices is needed. The inclusion of atomistic simulations and physical modelling to further complement the experimental observations is also necessary. For example, the QPC model,[210] one

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of the most widespread for studying the different conductance levels in HRS and LRS in RRAMs,[205,206] has been used in very few GRM-based devices.[163,308]

7.3. Technology Viability

The number of TMO-based RRAMs reporting performances above the technology requirements is much larger than for GRM-based ones. For this reason, TMO-based RRAMs are more reliable and (still) superior to GRM-based RRAMs. Moreover, as for TMO-based RRAMs, there is still not a GRM-based RRAM fitting all technology requirements simultaneously, indicating that more research is required. Nevertheless, the faster optimization speed of GRM-based RRAMs as well as the superior electronic,[76] physical,[77] chemical,[78] mechanical,[79] optical,[80] magnetic[81] and thermal[82] properties.[83] of GRMs (compared to TMOs) are strong arguments to further explore this technology.

8. Conclusions

GRMs have been introduced in the structure of RRAMs with the objectives of i) enhancing their performance as NVM (endurance, retention, switching time, power consumption, operation voltages) and ii) provide additional capabilities (flexibility, transparency, chemical stability, heat dissipation). Graphene can be used as electrode to provide flexibility and transparency, and/or as interface layer between electrodes and RS medium, to decrease the cycle-to-cycle variability, by avoiding atomic diffusion between electrode and insulator. This can reduce the power consumption due to its high out-of-plane contact resistance (compared to metallic electrodes), and suppress surface effects by avoiding chemisorption and/or photodesorption. Surface band bending may allow one to tune the properties of the devices by functionalization, reducing the thickness of the electrodes and improving the three dimensional stackability. GO, a-C, TMDs, *h*-BN and BP can be used as active RS media to induce the resistivity changes either by migration of intrinsic species (such as oxygen in GO and sulfur in MoS_2) or by penetration of metallic ions from adjacent electrodes. Graphene is usually produced by CVD and inserted in RRAMs by polymer-assisted transfer. When using *h*-BN as RS medium, the standard transfer can be avoided, and the catalyst substrate for CVD growth can be used as bottom electrode. GO and BP are usually produced by LPE and spin coated on a conductive wafer, which serves as bottom electrode. TMDs have been inserted in RRAMs either by CVD plus transfer or LPE plus spin coating. In all cases, top electrodes can be easily fabricated using an evaporator/sputtering coupled with standard photolithography.

GRMs-based RRAMs have shown reproducible unipolar and bipolar RS with high $I_{ON}/I_{OFF} > 10^5$, low operating voltages <1V and fast switching times (<30 ns). In most reports the switching is attributed to the formation/disruption of CFs in the RS medium, and the atomic rearrangements in each state transition are related to the movement of intrinsic species and/or penetration of metallic ions from adjacent layers, showing parallelism with TMO-based RRAMs. GRMs have also been mixed/embedded with polymers, nanoparticles, nanorods and quantum dots in order to enhance the performance (mainly retention and endurance), but in many cases it is unclear what the real need/usefulness of the GRMs are. Despite all efforts, NVMs technological requirements like endurance $>10^9$ cycles and data retention >10 years still remain a challenge. Only one report using a-C as dielectric demonstrated excellent endurance $>10^9$ cycles, and we are not aware of any GRMs-based RRAM showing retention times >10 years. From the point of view of flexibility, GRM-based RRAMs can hold RS under more than $>10^5$ bending stresses with radius down to few mm (no technological requirements in this sense have been established). Moreover, GRM-based RRAMs with transparencies >92% have been reported. The benefits of other GRM properties (such as high chemical stability and thermal heat dissipation) on the performance of RRAMs have not been discussed.

Most RS studies in GRMs concentrated on proof-of-concept demonstrations using large area (>2000 μm^2) devices, which makes it difficult to extrapolate to real ultra-scaled RRAMs. Future GRMs-based studies should use smaller sizes (<1 μm^2), focus on demonstrating performances (i.e. endurance, retention, switching time and power consumption) above the NVM technology requirements, and include reliability and variability analyses. The use of atomistic simulations and modelling to support/explain the experimental observations is also necessary.

The fact that GRMs-based devices already fit some NVM technology requirements (operating voltages, endurance and switching times) makes this field worth of further investigation.

Abbreviations

a-C	Amorphous carbon
a-C:H	Hydrogenated amorphous carbon
a-C:N	Nitrogenated amorphous carbon
a-CO_x	Oxygenated amorphous carbon
ALD	Atomic layer deposition
APTES	3-Aminopropyltriethoxysilane
BD	Dielectric breakdown
BLG	Bilayer graphene
BP	Black phosphorous
BP-GBL	Black phosphorous in (γ-butyrolactone)
BP-IPA	Black phosphorous in isopropanol
CAFM	Conductive atomic force microscopy
CBRAM	Conductive bridge random access memory
CF	Conductive filament
CL	Current limitation
CMOS	Complementary metal oxide semiconductor
CVD	Chemical vapor deposition
CVS	Constant voltage stresses
1D1R	One diode one resistor
DRAM	Dynamic random access memory

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ECM	Electrochemical metallization
FET	Field effect transistor
FRAM	Ferroelectric RAM
GB	Grain boundary
GFET	Graphene field effect transistor
GI	Graphene/Insulator
GIG	Graphene/Insulator/Graphene
GMIM	Graphene/Metal/Insulator/Metal
GMIMG	Graphene/Metal/Insulator/Metal/Graphene
GO	Graphene oxide
GQDs	Graphene quantum dots
GO-PVK	Poly (n-vinylcarbazole) derived graphene oxide
GRMs	Graphene and related materials
GS-RRAM	Graphene set electrode resistive random access memory
h-BN	Hexagonal boron nitride
HRS	High resistance state
ITO	Indium tin oxide
ITRS	International Technology Roadmap for Semiconductors
LM	Layered material
LPE	Liquid phase exfoliation
LRS	Low resistance state
LSG-RRAM	Laser-scribed reduced graphene oxide
MC	Micromechanical exfoliation
MGIGM	Metal/Graphene/Insulator/Graphene/Metal
MGIM	Metal/Graphene/Insulator/Metal
MIGM	Metal/Insulator/Graphene/Metal
MIM	Metal/Insulator/Metal
MIMG	Metal/Insulator/Graphene/Metal
MLG	Multilayer graphene
MRAM	Magnetoresistive random access memory
NVM	Non-volatile memory
PCBM	6-Phenyl-C61 butyric acid methyl ester
PCMO	Pr0.7Ca0.3MnO3
PCRAM	Phase change random access memory
PET	Poly(ethylene terephthalate)
PMC	Programmable metallization cells
PMMA	Polymethyl mechacrylate
PVK	Poly (n-vinylcarbazole) derived graphene oxide
PVP	Polyvinylpyrrolidone
QPC	Quantum point contact
RGO	Reduced graphene oxide
RRAM	Resistive random access memory
RS	Resistive switching
SLG	Single-layer graphene
STTM-RAM	Spin transfer torque magnetic random access memory
ta-C	Tetrahedral amorphous carbons
TEM	Transmission electron microscopy
TMDs	Transition metal dichalcogenides
TMO	Transition metal oxide
TPAPAM	Triphenylamine-based polyazomethine
VCM	Valence change memory
ReRAM	Redox random access memory
XPS	X-ray photoelectron spectroscopy
ZnONRs	ZnO nanorods

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