Phys. Status Solidi B **246**, No. 11–12, 2514–2517 (2009) / **DOI** 10.1002/pssb.200982356

physica status solidi b
www.pss-b.com
basic solid state physics

Fabrication of graphene nanoribbons via nanowire lithography

A. Fasoli[*,1], **A. Colli**[2], **A. Lombardo**[1], **and A. C. Ferrari**[1]

[1] Department of Engineering, University of Cambridge, Cambridge CB3 0FA, UK
[2] Nokia Research Centre Cambridge UK, c/o Nanoscience Centre, University of Cambridge, Cambridge CB3 0FF, UK

Received 1 July 2009, revised 17 August 2009, accepted 28 August 2009
Published online 29 October 2009

PACS 81.07.−b, 81.05.Uw

* Corresponding author: e-mail af343@cam.ac.uk, Phone: +44 1223 748349, Fax: +44 1223 748348

Graphene nanoribbons (GNRs) are the counterpart of nanotubes in graphene nanoelectronics. The search for a cheap, parallel, and deterministic technique for practical implementation of these structures is still open. Nanowire lithography (NWL) consists in using nanowires (NWs) as etch masks to transfer their one-dimensional morphology to an underlying substrate. Here, we show that oxidized silicon NWs (SiNWs) are a simple and compatible system to implement NWL on graphene. The SiNWs morphology is transferred onto a graphene flake by a low-power O_2 plasma in a deep-reactive-ion-etcher. The process leads to conformal GNRs with diameter comparable to the overlaying NW lateral dimensions. The diameter can be further reduced by multiple O_2 etching steps. Field-effect measurements show the transition to a semiconductor for low diameters.

© 2009 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

1 Introduction Graphene is the latest carbon allotrope to be discovered, and it is now at the center of a significant research effort [1–6]. Near-ballistic transport at room temperature and high mobility [5–9] make it a potential material for nanoelectronics [10–12], especially for high frequency applications [13]. Its transparency and mechanical properties are ideal for micro- and nanomechanical systems, thin-film transistors and transparent and conductive composites, and electrodes [14–17].

Similar to the case of nanotubes, confinement modifies the electronic structure of graphene, when cut into nanoribbons [18–24]. The edges of graphene nanoribbons (GNRs) could in general be a combination of armchair or zigzag regions [25–28]. If a GNR is uniquely limited by one type of edge, it is defined either as armchair or zigzag [18, 19, 28]. Edges are also preferred sites for functionalization with different groups [29, 30].

The most common route to get GNRs is patterning a graphene flake with e-beam lithography [31–33] or using the tip of a scanning probe microscope [34, 35]. Solution processing was also used to produce sub-10-nm GNRs [36]. However, even if this route looks promising for large scale production, the GNR width distribution and the need to assemble the as-produced GNRs into devices are critical issues. Recently, dielectrophoretic assembly was suggested as a means to achieve high-density arrays of individual graphene and GNRs devices from solution [37]. Unzipping of nanotubes was also shown to produce GNRs [38, 39]. This technique, once optimized, could be combined with the expertise in nanotube placement, selection, and assembly and be a viable route for large scale GNR devices.

Nanowires (NWs) can be used as selective etch masks [40, 41]. This is commonly referred to as nanowire lithography (NWL) [40, 41]. This technique could be used to patter graphene, with, in principle, several benefits: (i) since NWs with diameters down to a few nanometers can be grown by several methods [42, 43], GNRs with similar sized can be easily produced, (ii) a mesh of NWs can be used to yield a GNR network over large areas, converting a semi-metallic graphene layer into a nanostructured semiconducting film; (iii) the NWL concept can rely not only on straight NWs as masks, but also on other nanostructures with more complex shape. For example, Si nanochains [44, 45] could be used to produce an array of sub-10-nm constrictions for quantum-blockade devices.

Here we report the fabrication of GNRs via NWL. We show that silicon NW (SiNW) masks coupled with anisotropic etching based on O_2 plasma can yield conformal

© 2009 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

GNRs with diameter similar to the SiNW mask. Field-effect transistors made of individual GNRs are obtained with process flow similar to that we introduced for NWL on Si [40]. A controlled undercut can also allow to realize GNRs with a smaller width than the SiNW mask.

2 Experimental Graphene flakes are produced via mechanical cleavage of graphite (NGS NaturGraphit) on a 300 nm-thick SiO_2 thermally grown on top of a heavily n-doped Si wafer. SiNWs (30–50 nm in diameter) are grown via Au-catalyzed vapor transport using Si powders as solid precursor [43]. As described in Ref. [40], SiNWs can be oxidized to behave as inert etch masks for NWL. Graphene flakes and SiNWs are visualized by scanning electron microscopy (SEM) and optical microscopy (Nikon Eclipse ME600L, 100× objective) [46] and further characterized by Raman Spectroscopy [47]. Graphene etching is achieved in a Deep Reactive Ion Etcher (Adixen AMS 100), by means of an O_2 plasma. Etching anisotropy is favored by the acceleration the ions undergo, as a consequence of the bias between the region where the plasma is formed and the substrate. In addition, the limited diffusion of oxygen radicals under the nanowire mask further slows down the lateral etch rate (undercut). The following parameters were used: O_2 flow rate = 100 sccm; pressure = 10^{-2} mbar; coil power = 400 W; substrate power = 15 W (pulsed mode, 5/95 ms ON/OFF ratio); substrate temperature = 0 °C; and minimum etching time = 10 s. For the fabrication of devices, electrodes are patterned by e-beam lithography followed by thermal evaporation of Cr and Au (20 and 100 nm, respectively). Electrical measurements are taken with a Cascade Microtech probe station coupled to an Agilent B1500A device analyzer.

3 Results Figure 1 shows schematically the device fabrication steps. A graphene flake is initially mapped on the surface by optical microscopy and Raman spectroscopy [46, 47]. A SiNW is then deposited on top of the flake by contact printing [48]. Back-gated FETs are obtained by clamping an NW mask between two metal leads in contact with the graphene flake. Upon O_2 etching, the exposed graphene is removed, resulting in a GNR channel. Note that large graphene islands also remain beneath the metal leads, ensuring good contacts. Given that the SiNW is oxidized, it does not contribute to the transport.

Scanning electron microscopy micrographs in Fig. 2 demonstrate the successful GNR fabrication. After a SiNW

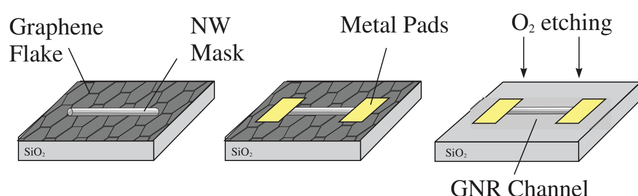

Figure 1 (online color at: www.pss-b.com) Schematic of GNR-FET fabrication process.

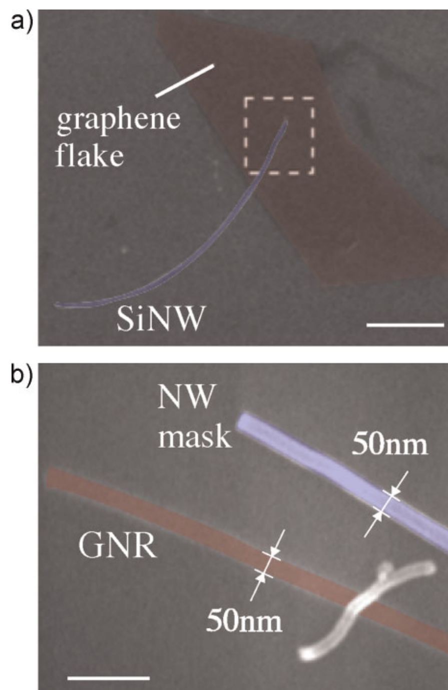

Figure 2 (online color at: www.pss-b.com) SEM micrographs of (a) NW deposited onto a graphene flake (scale bar: 1 μm); (b) NW dislodged after O_2 etching revealing a GNR (scale bar: 200 nm).

is deposited onto a graphene flake (Fig. 2a), a 10 s O_2 plasma is used to remove the unscreened carbon. A GNR is revealed as the NW mask is dislodged using an AFM tip (Fig. 2b). Note that the GNR width matches very well the NW diameter, indicating the highly anisotropic character of the etching process. Given that only a relatively mild etching is needed to attack single-layer graphene, this particular application of NWL may rely on NW masks made of a wide range of materials, including some robust organic nanofibers. On the other hand, when applying NWL on silicon, a more aggressive etching is required [40].

Graphene nanoribbons of different width (Fig. 3a and b) can be made via NWL following three different strategies. First, NWs of different diameter can be used. Second, etching anisotropicity can be enhanced by increasing plasma power. For example, a 600 W O_2 plasma induces significant undercut in only 20 s, producing ~15–30 nm wide GNRs from NW masks ~40–50 nm in diameter (Fig. 3a and b). However, GNR devices fabricated in these conditions sometimes show no conductance, indicating that an aggressive plasma may cut a ribbon completely. For this reason, we believe a third method, which involves varying the etching time rather than the plasma power, to be a more controllable approach to produce GNRs thinner than the NW masks.

We then assess the electrical properties of our GNR FETs. In no case conductance is seen between the electrodes without a bridging NW mask, confirming the successful flake removal. Figure 4 shows three transfer curves of a 40 nm

© 2009 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

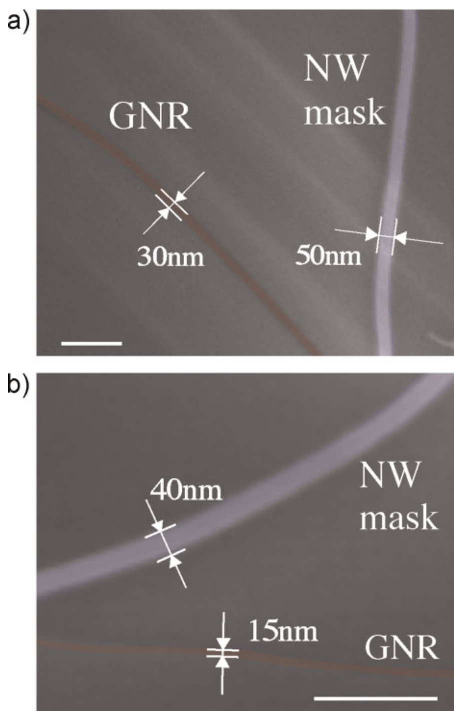

Figure 3 (online color at: www.pss-b.com) (a and b) SEM micrographs of GNRs narrower than the NW mask used for their fabrication. Scale bars: 200 nm.

wide, 400 nm long GNR after consecutive etching steps of 10 s (etch1), 15 s (etch2), and 15 s (etch3). (etch1) removes the exposed graphene producing a GNR matching the NW diameter. Since the NW diameter is ~40 nm, no appreciable confinement effects are expected for this GNR [31, 49]. Indeed, the curve corresponding to etch1 in Fig. 4 (blue) has the same ON/OFF ratio (~2.5) of the original flake, while the drain current decreases consistently with the channel width reduction from 10 μm of the flake to 40 nm of the GNR. After the second etching step (etch2, green curve Fig. 4), no difference is seen. After the third etch step, however, the device behavior is significantly altered. For the same range of gate voltages, the field-effect response is stronger and the ON/OFF ratio increases to 14. Moreover, by sweeping the gate voltage in both directions, we observe that a relatively large hysteresis is introduced by the etch3 step, while after etch1 and etch2 hysteresis is negligible (Fig. 4). The trend reported in Fig. 4 suggests that our etch process, ideally anisotropic for short times (10–15 s), may eventually result in undercutting for longer plasma treatments. Indeed, higher ON/OFF ratios reflect gap opening, which for GNRs on this scale is inversely proportional to the ribbon width [31, 49].

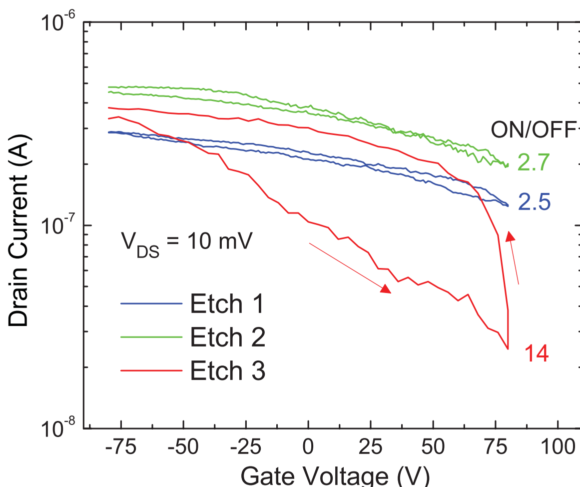

Figure 4 (online color at: www.pss-b.com) Transfer curves of GNR after multiple (one to three) etching steps. Red arrows show voltage sweep direction.

A narrower ribbon could also explain the larger hysteresis in Fig. 4 after etch3, if one assumes that this is due to trap states on the NW masks surface [49, 50]. The edges of a conformal ribbon beneath a NW mask with distributed charged states will be less affected by the traps field than the central GNR portion. This geometrical effect will decrease for smaller GNR width, resulting in a stronger hysteresis. The edges can also play a critical role in determining the device behavior. A better understanding of the edge roughness induced by etching is needed for a more accurate understanding of the system.

In conclusion, we used NWL and SiNW mask to etch conformal GNRs in graphene. Fabrication of individual-GNR back-gated FETs was demonstrated. Transfer curves from devices undergoing multiple etching steps are consistent with GNR undercutting.

Acknowledgements We acknowledge funding from the Cambridge Integrated Knowledge Centre (CIKC) and the Cambridge–Nokia partnership. A. L. acknowledges funding from Palermo University, A. C. F. from The Royal Society and the European Research Council Grant NANOPOTS.

References

[1] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, Science **306**, 666 (2004).
[2] A. K. Geim and K. S. Novoselov, Nat. Mater. **6**, 183 (2007).
[3] A. H. Castro Neto, F. Guinea, N. M. R. Peres, K. S. Novoselov, and A. K. Geim, Rev. Mod. Phys. **81**, 109 (2009).
[4] J. C. Charlier, P. C. Eklund, J. Zhu, and A. C. Ferrari, Topics Appl. Phys. **111**, 673 (2008).
[5] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, M. I. Katsnelson, I. V. Grigorieva, S. V. Dubonos, and A. A. Firsov, Nature (London) **438**, 197 (2005).
[6] Y. Zhang, Y. W. Tan, H. L. Stormer, and P. Kim, Nature (London) **438**, 201 (2005).
[7] K. S. Novoselov, Z. Jiang, Y. Zhang, S. V. Morozov, H. L. Stormer, U. Zeitler, J. C. Maan, G. S. Boebinger, P. Kim, and A. K. Geim, Science **315**, 1379 (2007).
[8] S. V. Morozov, K. S. Novoselov, M. I. Katsnelson, F. Schedin, D. C. Elias, J. A. Jaszczak, and A. K. Geim, Phys. Rev. Lett. **100**, 016602 (2008).

© 2009 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

[9] (a) K. I. Bolotin, K. J. Sikes, J. Hone, H. L. Stormer, and P. Kim, Phys. Rev. Lett. **101**, 096802 (2008).
(b) K. I. Bolotin, K. J. Sikes, Z. Jiang, G. Fundenberg, J. Hone, P. Kim, and H. L. Stormer, Solid State Commun. **146**, 351 (2008).
[10] M. Y. Han, B. Oezylmaz, Y. Zhang, and P. Kim, Phys. Rev. Lett. **98**, 206805 (2007).
[11] Z. Chen, Y. M. Lin, M. Rooks, and P. Avouris, Physica E **40**, 228 (2007).
[12] M. C. Lemme, T. J. Echtermeyer, M. Baus, and H. Kurz, IEEE Electron Device Lett. **28**, 4 (2007).
[13] Y. M. Lin, K. A. Jenkins, A. Valdes-Garcia, J. P. Small, D. B. Farmer, and P. Avouris, Nano Lett. **9**, 422 (2009).
[14] J. S. Bunch, A. M. van der Zande, S. S. Verbridge, I. W. Frank, D. M. Tanenbaum, J. M. Parpia, H. G. Craighead, and P. L. McEuen, Science **315**, 490 (2007).
[15] P. Blake, P. D. Brimicombe, R. R. Nair, T. J. Booth, D. Jiang, F. Schedin, L. A. Ponomarenko, S. V. Morozov, H. F. Gleeson, E. W. Hill, A. K. Geim, and K. S. Novoselov, Nano Lett. **8**, 1704 (2008).
[16] Y. Hernandez, V. Nicolosi, M. Lotya, F. Blighe, Z. Sun, S. De, I. T. McGovern, B. Holland, M. Byrne, Y. Gunko, J. Boland, P. Niraj, G. Duesberg, S. Krishnamurti, R. Goodhue, J. Hutchison, V. Scardaci, A. C. Ferrari, and J. N. Coleman, Nature Nanotechnol. **3**, 563 (2008).
[17] G. Eda, G. Fanchini, and M. Chhowalla, Nature Nanotechnol. **3**, 270 (2008).
[18] K. Nakada, M. Fujita, G. Dresselhaus, and M. S. Dresselhaus, Phys. Rev. B **54**, 17954 (1996).
[19] M. Fujita, K. Wakabayashi, K. Nakada, and K. Kusakabe, J. Phys. Soc. Jpn. **65**, 1920 (1996).
[20] Y. Miyamoto, K. Nakada, and M. Fujita, Phys. Rev. B **59**, 9858 (1999).
[21] K. Wakabayashi, M. Fujita, H. Ajiki, and M. Sigrist, Phys. Rev. B **59**, 8271 (1999).
[22] Y. W. Son, M. L. Cohen, and S. G. Louie, Phys. Rev. Lett. **97**, 216803 (2006).
[23] L. Pisani, J. A. Chan, B. Montanari, and N. M. Harrison, Phys. Rev. B **75**, 064418 (2007).
[24] K. Nakada, M. Igami, and M. Fujita, J. Phys. Soc. Jpn. **67**, 2388 (1998).
[25] Y. Niimi, T. Matsui, H. Kambara, K. Tagami, M. Tsukada, and H. Fukuyama, Phys. Rev. B **73**, 085421 (2006).
[26] Y. Kobayashi, K. Fukui, T. Enoki, K. Kusakabe, and Y. Kaburagi, Phys. Rev. B **71**, 193406 (2005).
[27] F. Sols, F. Guinea, and A. H. Castro Neto, Phys. Rev. Lett. **99**, 166803 (2007).
[28] Y. Niimi, T. Matsui, H. Kambara, K. Tagami, M. Tsukada, and H. Fukuyama, Appl. Surf. Sci. **241**, 43 (2005).
[29] F. Cervantes, S. Piscanec, G. Csanyi, and A. C. Ferrari, Phys. Rev. B **77**, 165427 (2008).
[30] X. R. Wang, X. L. Li, L. Zhang, Y. Yoon, P. K. Weber, H. L. Wang, J. Guo, and H. J. Dai, Science **324**, 768 (2009).
[31] M. Y. Han, B. Ozyilmaz, Y. Zhang, and P. Kim, Phys. Rev. Lett. **98**, 206805 (2007).
[32] Z. Chen, Y.-M. Lin, M. J. Rooks, and P. Avouris, Physica E **40**, 228 (2007).
[33] C. Berger, Z. Song, X. Li, X. Wu, N. Brown, C. Naud, D. Mayou, T. Li, J. Hass, A. N. Marchenkov, E. H. Conrad, P. N. First, and W. A. de Heer, Science **312**, 1191 (2006).
[34] L. Tapaszto, G. Dobrik, P. Lambin, and L. P. Biro, Nature Nanotechnol. **3**, 397 (2008).
[35] L. Weng, L. Zhang, Y. P. Chen, and L. P. Rokhinson, Appl. Phys. Lett. **93**, 093107 (2008).
[36] X. Li, X. Wang, L. Zhang, S. Lee, and H. Dai, Science **319**, 1229 (2008).
[37] A. Vijayaraghavan, C. Sciascia, S. Dehm, A. Lombardo, A. Bonetti, A. C. Ferrari, and R. Krupke, ACS NANO **3**, 1729 (2009).
[38] D. V. Kosynkin, A. L. Higginbotham, A. Sinitskii, J. R. Lomeda, A. Dimiev, B. K. Price, and J. M. Tour, Nature **458**, 872 (2009).
[39] L. Jiao, L. Zhang, X. Wang, G. Diankov, and H. Dai, Nature **458**, 877 (2009).
[40] A. Colli, A. Fasoli, S. Pisana, Y. Fu, P. Beecher, W. I. Milne, and A. C. Ferrari, Nano Lett. **8**, 1358 (2008).
[41] D. Whang, S. Jin, and C. M. Lieber, Nano Lett. **3**, 951 (2003).
[42] Y. Wu, Y. Cui, L. Huynh, C. J. Barrelet, D. C. Bell, and C. M. Lieber, Nano Lett. **4**, 433 (2004).
[43] A. Colli, A. Fasoli, P. Beecher, P. Servati, S. Pisana, Y. Fu, A. J. Flewitt, W. I. Milne, J. Robertson, C. Ducati, S. De Franceschi, S. Hofmann, and A. C. Ferrari, J. Appl. Phys. **102**, 034302 (2007).
[44] M. A. Rafiq, H. Mizuta, A. Colli, P. Servati, A. C. Ferrari, Z. A. K. Durrani, and W. I. Milne, J. Appl. Phys. **103**, 053705 (2008).
[45] H. Y. Peng, Z. W. Pan, L. Xu, X. H. Fan, N. Wang, C.-S. Lee, and S. T. Lee, Adv. Mater. **13**, 317 (2001).
[46] C. Casiraghi, A. Hartschuh, E. Lidorikis, H. Qian, H. Harutyunyan, T. Gokus, K. S. Novoselov, and A. C. Ferrari, Nano Lett. **7**, 2711 (2007).
[47] A. C. Ferrari, J. C. Meyer, V. Scardaci, C. Casiraghi, M. Lazzeri, F. Mauri, S. Piscanec, D. Jiang, K. S. Novoselov, S. Roth, and A. K. Geim, Phys. Rev. Lett. **97**, 187401 (2006).
[48] A. Colli, S. Pisana, A. Fasoli, J. Robertson, and A. C. Ferrari, Phys. Status Solidi B **244**, 4161 (2007).
[49] X. Wang, Y. Ouyang, X. Li, H. Wang, J. Guo, and H. Dai, Phys. Rev. Lett. **100**, 206803 (2008).
[50] E. H. Nicollian and J. R. Brews, MOS (Metal Oxide semiconductor) Physics and Technology (Wiley, New York, 1982).

 © 2009 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim