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Electronic transport in ambipolar silicon nanowires

A. Colli[*], **S. Pisana, A. Fasoli, J. Robertson,** and **A. C. Ferrari**

Engineering Department, Cambridge University, Cambridge CB3 0FA, UK

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We investigate and compare the electronic transport in ambipolar SiNWs as a function of the metal choosen for contact deposition. The wires are grown by Au-catalyzed vapour-transport and exhibit crystalline cores about 15–20 nm in thickness. The suitability of Ti and Ni contacts on SiNWs is evaluated in terms of contact resistance and band-alignment. The beneficial effect of a rapid-thermal-annealing at mild temperatures (400 °C) is also investigated. We observe that annealed Ni contacts yield the lowest device resistance and highest ON/OFF ratio.

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1 Introduction

Silicon nanowires (SiNWs) have shown in recent years a tremendous potential for the development of future nano-electronics [1, 2]. A key step to assess the suitability of SiNWs for applications is to investigate their electrical properties. It is often claimed that the use of SiNWs would result in transistor performance (e.g., carrier mobility) well above existing technologies [2–4]. However, the reported values for SiNW hole mobility are so far widely scattered from ~10 cm^2/Vs to 1350 cm^2/Vs (see, for example, Refs. [2–5]). A variety of different metals have been tested to contact SiNWs, such as Al/Au, Ni, Ti/Al, Ti/Au, Cr/Au [1, 4, 6–8], and different annealing treatments have been implemented [1, 4, 6–8]. Because of this, scattered parameters for SiNW-based transistors have been reported [7].

Ambipolar SiNWs by Au-seeded growth were recently reported [3, 9]. Here, we fabricate planar field-effect transistors (FETs) using ambipolar SiNWs grown by Au-catalysed vapour-transport [9]. We present a comparative assessment of the electronic transport in such SiNW FETs by using leads made of different metals. As-deposited and annealed Ti and Ni contacts are evaluated in terms of contact resistance and band-alignment. The higher ON/OFF ratio observed for Ni contacts indicates a higher Schottky barrier for positive carriers.

2 Experimental

Au-catalyzed growth of SiNWs is achieved by means of a thermal evaporation process in a furnace [9–11]. Pure Si powders are placed in an alumina boat and heated to 1250 °C. The Si vapour is carried downstream by a 100 sccm Ar flow and condenses along the colder regions (750–850 °C) of the furnace tube where the Au-coated substrates are placed. As-produced NWs are characterized by field-emission scanning electron microscopy (SEM), and high-resolution transmission electron microscopy (TEM). Three-terminals FETs are fabricated by dispersing SiNWs on a 200 nm thick SiO_2 layer thermally grown on a degenerate p-doped Si wafer, used as back-gate. Source and drain contacts are defined by e-beam

[*] Corresponding author: e-mail: ac458@cam.ac.uk

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lithography with a typical channel length of 1 µm. After a short etching in buffered HF, Ti/Al (20/90 nm) or Ni (50 nm) contacts are deposited by e-beam evaporation. Further device annealing is carried out on a resistive heater for 30 seconds in formic gas, up to a maximum temperature of 400 °C.

3 Results and discussion

Figure 1a shows SiNWs grown on Au-patterned Si substrates. The SiNWs are tens of microns in length, thus forming a dense "spaghetti-like" forest over the catalyst layer and extending onto the Au-uncoated regions that did not react with the Si vapour. A representative TEM micrograph of a single SiNW is shown if Fig. 1b. The wire is uniform in diameter and exhibits a highly-crystalline Si core, about 18 nm in diameter, surrounded by an amorphous, oxidized shell (8 nm). Such a thick oxide shell cannot be attributed to wire oxidation upon exposure to atmosphere at room temperature (that gives no more than 1–2 nm of native oxide for chemical-vapour-deposition-grown SiNWs [12]), but must be a by-product of the vapour-transport technique itself [9, 10]. If the shell is not removed by etching in buffered HF, no contacts to the NW core can be fabricated.

After synthesis, NWs are mechanically transferred onto separate substrates for contact deposition. Aligned NW arrays (Fig. 2a) are obtained by gently sliding the as-grown substrate to the receiving one [13]. The final density of transferred NWs is roughly proportional to the pressure applied to keep the source and receiving chips into contact. With a suitable contact geometry, a statistical distribution of devices including large number of NWs down to a single one can be obtained (Fig. 2b).

Figure 3a and 3b compare representative transfer curves ($I_{DS}-V_{GS}$) at room temperature for SiNW FETs fabricated using Ti and Ni, respectively, as source-drain contact leads. We observe that our SiNW show ambipolar behaviour [9], i.e., hole injection occurs for negative gate voltages whereas electron injection occurs for positive gate voltages, irrespective of which metal is used. However, we note that ambipolar devices with Ti contacts cannot be completely turned off, but a residual current is detected at room temperature for intermediate gate voltages. Such residual "plateau" current (independent of V_G) is due to thermionic emission [9] and is found to increase by increasing V_{DS}. Conversely, Ni contacts allow for a proper OFF state, where no measurable current is detected for any V_{DS} (even if only for a narrow range of gate voltages, Fig. 3b).

The lack of thermionic emission for Ni-based devices may be related to a different Schottky barrier between the metal lead and the SiNW. We measured a Schottky barrier (for holes) of only 0.08 eV in Ref. [9] using Ti, whereas other groups inferred that Ni contacts on SiNWs leads to a barrier (for holes) of 0.55 eV [8]. This is qualitatively consistent with the results reported in Fig. 3. We also observe that

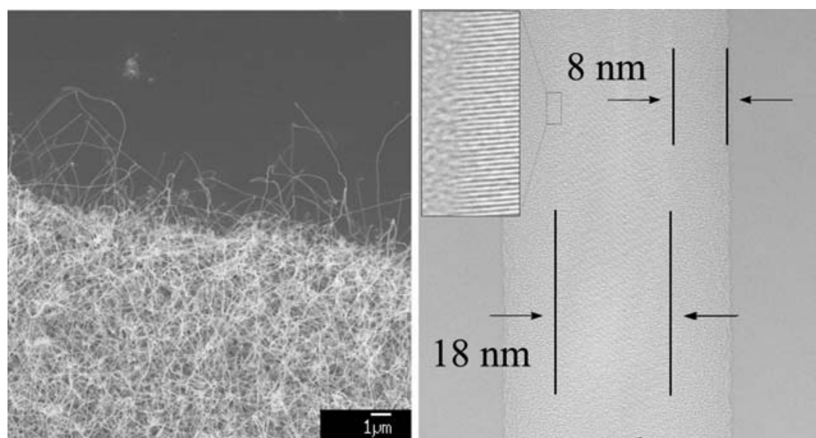

Fig. 1 (a) SEM image of SiNWs grown by vapour transport on a Au pattern. (b) TEM micrograph of a SiNW, showing the crystalline core and the thick amorphous shell.

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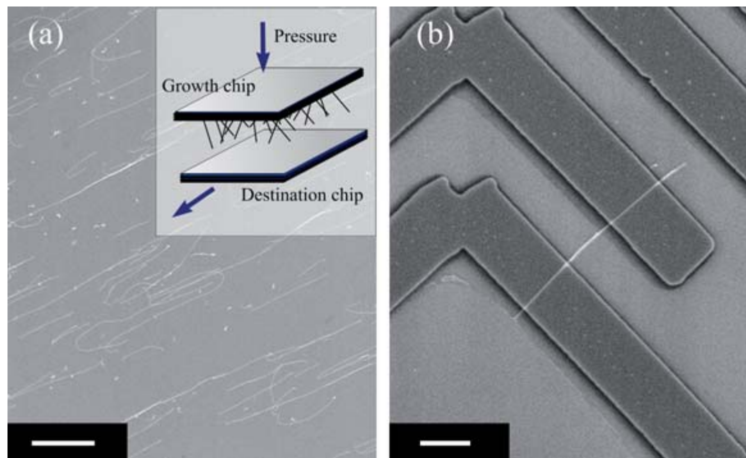

Fig. 2 (online colour at: www.pss-b.com) (a) Transferring of as-grown SiNWs onto oxidized chips for device fabrication. Shear forces align the wires along the sliding direction. (b) Contact deposition on individual or multiple SiNWs. Scalebars: 1 µm.

the *relative* separation between hole and electron threashold voltages is roughly the same in both cases (~5 V), because this is a function only of the semiconductor bandgap and not of the particular band alignment.

Figure 4 plots the output curves ($I_{DS}-V_{DS}$) for all types of SiNW devices, measured for gate voltages corresponding to the ON state for holes (as indicated on the representative ambipolar transfer curves in the inset). For Ni contacts, a remarkable increase in the output current is seen when annealing the device at 400 °C. It has been shown that NiSi formation occurs at this temperature at the metal/SiNW interface [7], while the temperature required for the formation of Ti silicides is much higher [14]. This can be the reason why no difference is seen by annealing the Ti-based devices at 400 °C (the single curve shown for Ti is representative of both cases, as-prepared and annealed). Curves in Fig. 4 correspond to devices with 10, 11 and 24 SiNWs (for Ni-annealed, Ni-not-annealed and Ti contacts, respectively). Even if more wires are connected in parallel for the Ti case, we observe that the total device resistance is more than one order of magnitude higher than for the best Ni-based device (red curve). This underlines the importance of contact fabrication in determining the performance of SiNWs FET devices.

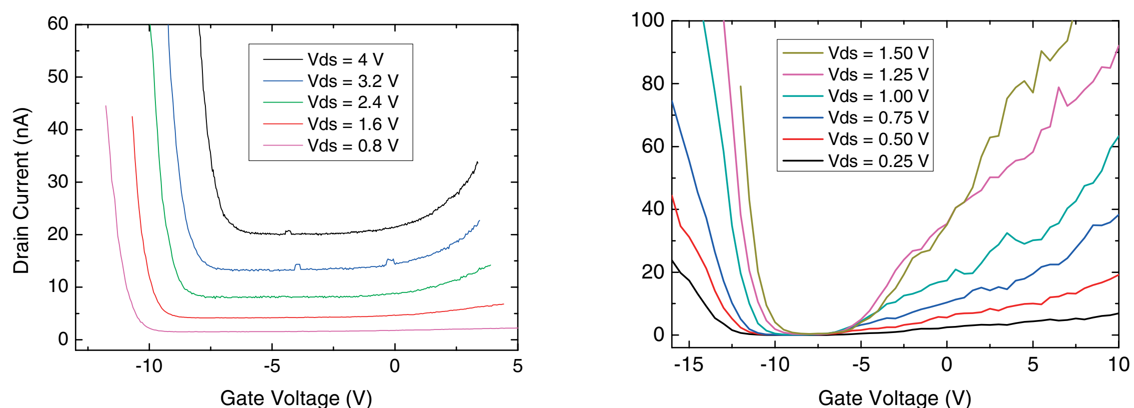

Fig. 3 (online colour at: www.pss-b.com) Representative transfer curves ($I_{DS}-V_{GS}$) for SiNWs FETs using Ti (left) and Ni (right) contacts. Ambipolar behaviour is seen in both cases, though the ON and OFF currents are different.

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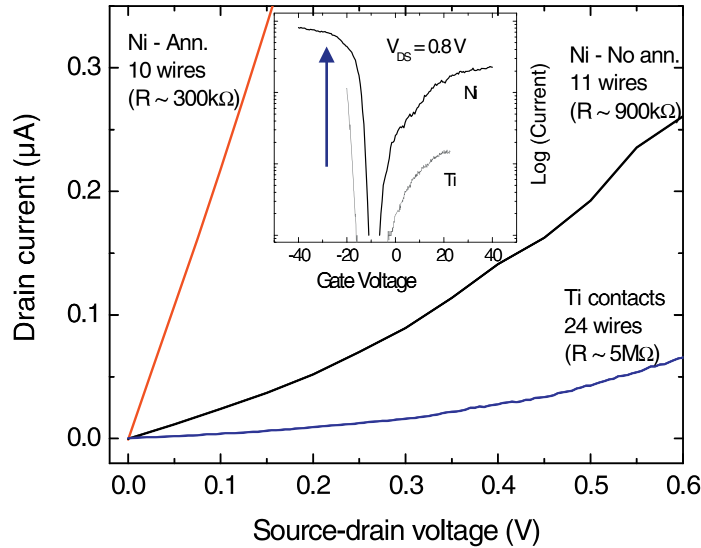

Fig. 4 (online colour at: www.pss-b.com) Output curves ($I_{DS}-V_{DS}$) measured for gate voltages corresponding to the ON state for hole population (–30 V, see inset), showing the effect of different metals and annealing treatment on device resistance. Curves correspond to devices with 10, 11 and 24 SiNWs (red, black, and blue, respectively).

4 Conclusion

Electronic transport in ambipolar SiNWs was studied for Ni and Ti contacts. The use of Ni contacts yields a lower device resistance and an improved ON/OFF ratio. A rapid-thermal-annealing at 400 °C is further beneficial for the performance of ambipolar SiNW devices.

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