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Nanowire Lithography on Silicon

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ABSTRACT

Nanowire lithography (NWL) uses nanowires (NWs), grown and assembled by chemical methods, as etch masks to transfer their one-dimensional morphology to an underlying substrate. Here, we show that SiO_2 NWs are a simple and compatible system to implement NWL on crystalline silicon and fabricate a wide range of architectures and devices. Planar field-effect transistors made of a single SOI-NW channel exhibit a contact resistance below 20 kΩ and scale with the channel width. Further, we assess the electrical response of NW networks obtained using a mask of SiO_2 NWs ink-jetted from solution. The resulting conformal network etched into the underlying wafer is monolithic, with single-crystalline bulk junctions; thus no difference in conductivity is seen between a direct NW bridge and a percolating network. We also extend the potential of NWL into the third dimension, by using a periodic undercutting that produces an array of vertically stacked NWs from a single NW mask.

Nanowires (NWs) and nanotubes are at the center of nanotechnology research. On the microscale, they can further increase the integration in electronic components,[1] exploiting novel architectures driven by self-assembly. Vertical NW transistors, for example, have been demonstrated,[2] while NW organization into stacked layers with well-defined alignment is being actively pursued for next-generation three-dimensional (3D) nanoelectronics.[3,4] On the macroscale, NWs represent a new class of materials for thin-film-transistors (TFTs),[5,6] sensors,[7,8] and transparent flexible electronics.[6,9,10]

Nanowire lithography (NWL) uses chemically synthesized NWs (CS-NWs) or nanotubes as nanomasks to etch conformal one-dimensional (1D) structures into an underlying thin film.[11–15] So far, this method has been applied to metal films[12–15] or SiO_2.[11] However, the application of NWL to crystalline silicon, which has a wide technological interest, remains surprisingly unexplored. In particular, silicon-on-insulator (SOI) films are a promising platform for extreme device scaling and to further push Moore's law toward its ultimate limits.[1,16] NWs in SOI layers (SOI-NWs) were recently produced,[17–19] but this either involved conventional top-down lithography[19] or pattern-transferring relying on stamp preparation.[17,18] To translate the simplicity and cost-effectiveness of NWL into practice, a highly selective and anisotropic process is needed, i.e., the etching recipe for Si must not attack the NW masks nor create appreciable undercutting. While, on one hand, a metallic NW mask could provide the desired selectivity,[13–15,17] on the other hand it requires a further etching step for mask removal, with consequent contamination and compatibility issues.

Here we show that SiO_2 NWs are a simple and compatible system to implement NWL on SOI films and silicon wafers in general. This unique combination of bottom-up and top-down fabrication allows us to achieve nanoscale features on SOI wafers with minimum processing effort. We demonstrate a variety of device concepts and architectures, from highly conductive NW networks to aligned arrays of vertically stacked NWs, showing that the potential of this approach goes far beyond planar ultraminiaturization, extending to very-large-area pattering and 3D electronics.

For large-area macroelectronics, NWs grown from the bottom-up are particularly attractive, since nanostructures can be assembled as films without the need for individual registration. The prototype devices so far presented[5–10] have essentially the same geometry, with multiple NWs (aligned or with random orientations) bridging metallic electrodes. As a limitation, though, large-area device up-scaling is constrained by the maximum NW length (typically not exceeding a few hundreds micrometers[5,7,10]). Hence, a truly wafer- or panel-scale active NW surface has to rely on an electrically conducting percolating network. Light-emitting diodes and logic gates have been demonstrated overlapping complementary NWs.[20,21] However, the junction of two juxtaposed NWs has high point resistance, due to the small contact area and partially oxidized surfaces, and is prone to mechanical instability. Indeed, longitudinal[22] or radial[23] NW heterostructures with high-quality epitaxial interfaces have been recently shown to outperform the crossed NW architecture.[22,23]

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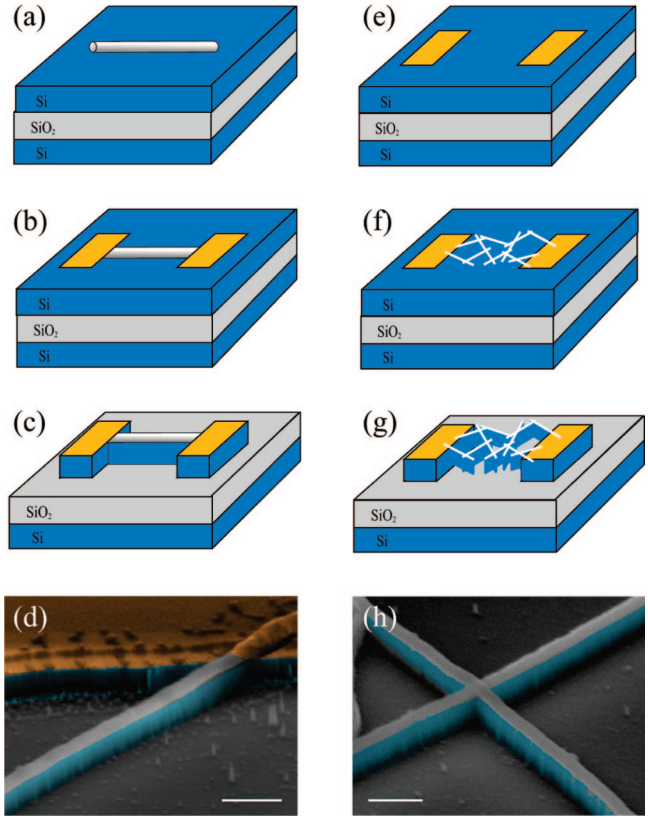

Figure 1. Complementary fabrication routes for direct-bridge (left) and network-like (right) NW devices using NWL on SOI layers. (a) Dispersion of fully oxidized SiNWs. (b) Lithographic patterning of metal contacts. (c) Etching of SOI by DRIE to define NW channels. (d) SEM micrograph of the final architecture. Different colors indicate different materials (gray = SiO_2; blue = Si; yellow = metal). Scale bar is 200 nm. (e) Patterning of metal pads on SOI. (f) Deposition of SiO_2 NW network from solution by spin-casting or ink-jet printing. (g) Etching of SOI by DRIE. A monolithic Si network with single-crystalline bulk junctions is carved into the SOI layer. (h) SEM micrograph of a monolithic Si junction with overlapping NW masks (gray = SiO_2; blue = Si). Scale bar is 200 nm.

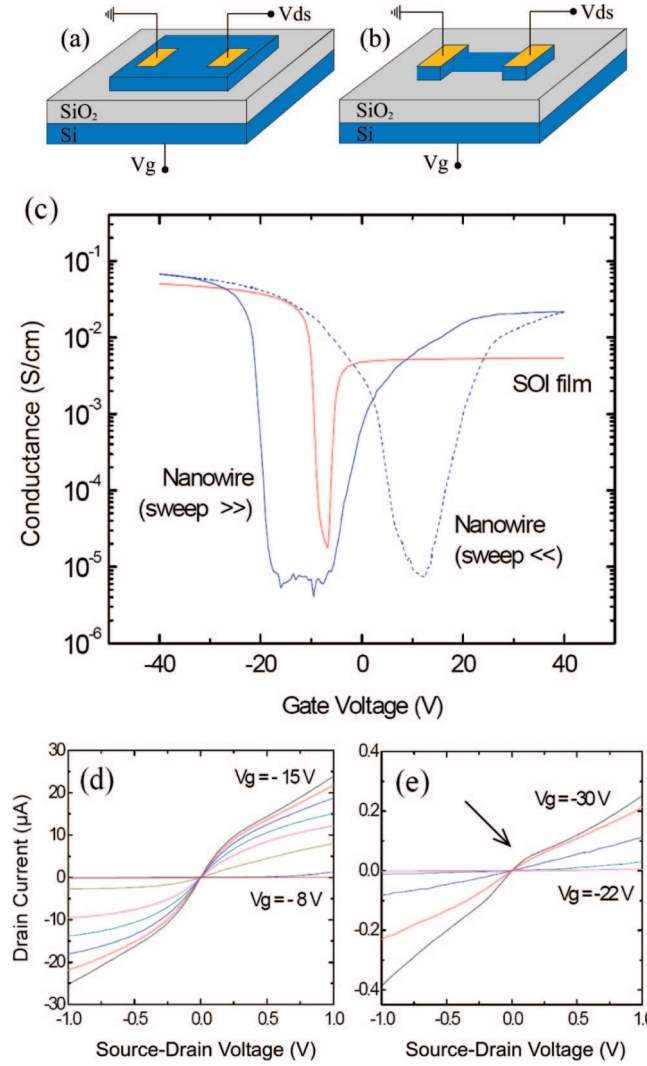

Figure 2. (a) Device schematic for transport measurement of SOI films. (b) Device schematic for individual SOI-NW channels. (c) Plot of channel conductance as a function of gate voltage for both device geometries. The conductance is normalized by the channel width. Ambipolar behavior is observed for both film and NW devices. NW devices manifest a visible hysteresis due to charge trapping at the NW surface. (d) Output curves for the SOI-film device. (e) Output curves for the SOI-NW device.

The use of CS-NWs as nanomasks for SOI lithography has in principle several advantages over their direct implementation as active device elements. For example, even by using a poorly conducting network of CS-NWs as mask, the resulting conformal network etched into the underlying wafer would be monolithic, with single-crystalline bulk junctions, allowing maximum performance. Also, a precise control over the doping concentration and crystallographic direction of CS-NWs is still lacking,[24] while for SOI-NWs these parameters would be accurately determined by the initial properties of the SOI substrate and the relative orientation of the NWL mask.

Figure 1 schematizes the steps for our NWL approach to make SiNW-based devices on SOI layers. The etching masks are SiNWs grown by vapor transport, by either Au-seeded or oxide-assisted growth.[25] These SiNWs, originally synthesized as single-crystalline structures, are fully converted to SiO_2 by furnace annealing in O_2 atmosphere at 950 °C for 10 min. The oxidation state of our SiNW masks is probed by Raman spectroscopy. Typical Raman spectra of SiNWs[26] are observed for pristine NW masks, but this signal disappears upon oxidation. Furthermore, FET channels made of oxidized NW masks are totally insulating. See Supporting Information for more details.

The final NW masks have lengths up to several micrometers and diameters between 20 and 40 nm. To fabricate single-NW devices (Figure 1a−d), oxidized NWs are dispersed on top of the SOI structure (Figure 1a) and contacted by Ni leads defined by e-beam or UV lithography (Figure 1b). We use a commercial SOI wafer (University Wafers) made of a Si (100 nm)/SiO_2 (150 nm)/Si (500 μm) structure. Both the substrate and the top Si layer are lightly p-doped (boron, resistivity ~10 Ω·cm). After mask deposition, the SOI layer is etched by deep-reactive-ion-etching (DRIE),[27,28] leading to a single-crystalline Si structure formed by two contact pads connected by a NW channel (Figure 1c). The Si substrate is used as a third terminal in a back-gate FET

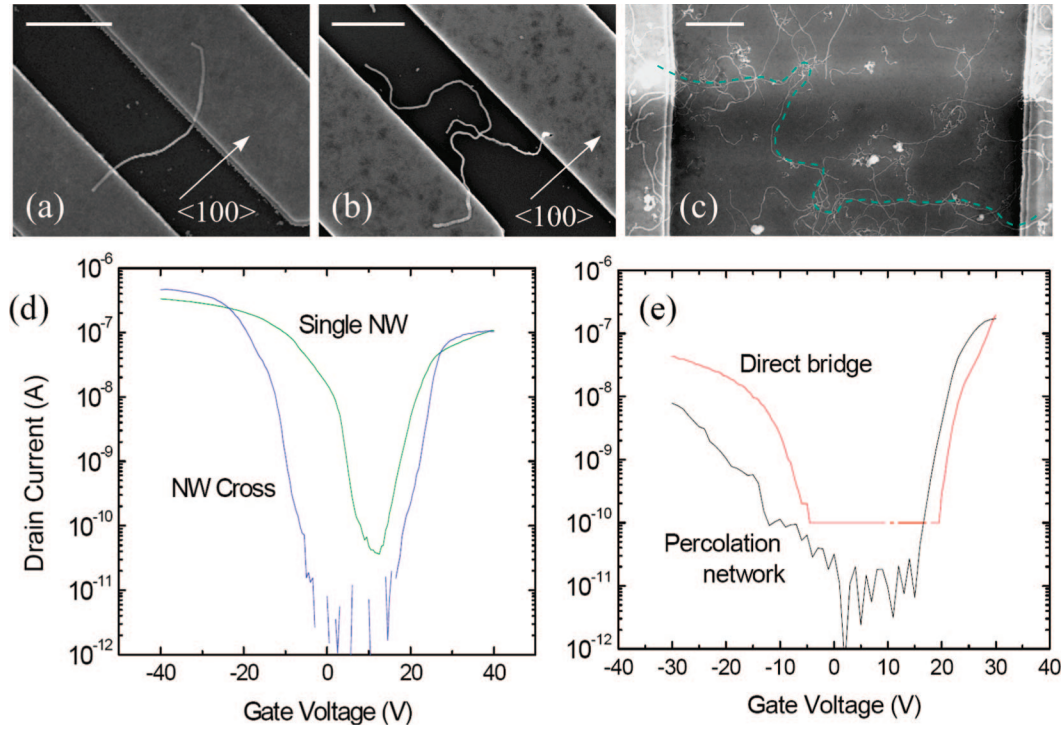

Figure 3. Electrical transport through monolithic NW junctions. (a) Direct bridge device made of an individual NW. (b) Single junction device made of two crossing NWs. SOI crystallographic direction is shown. (c) Percolation network of SOI-NWs within a 6 μm long electrode gap. A percolation path through several NW-NW junctions is highlighted. All scale bars are 1 μm. (d) Comparison of transfer curves for direct (panel a) and crossed (panel b) NW channel geometries. The ON currents for both holes and electrons are closely comparable. (e) Comparison of transfer curves for direct and percolating channel geometries. For this long-channel (6 μm) device, hole conductance deteriorates.

configuration. Figure 1d shows a SEM micrograph of the final architecture,different colors emphasize the chemical composition of the overall structure. Since the SiO_2 NWs do not conduct, there is no need to remove them at the end of the process, unlike the metal masks in refs 17 and13−15. On the contrary, they can still play an important function for top gating in advanced FET geometries.

A similar and complementary process flow is used to fabricate SOI-NW networks (Figure 1e−h). Here, we first pattern an array of electrodes on the SOI layer (Figure 1e). We then deposit the oxidized NWs on top with a sufficient high density to create percolation paths between both terminals (Figure 1f).[29] The conformal netlike structure is then etched into the SOI (Figure 1g) in the same conditions (Figure 1c). Figure 1h shows an SEM image of two overlapping NW masks and the resulting monolithic crossed junction beneath them. We emphasize that, as a major advantage of the NWL concept, there is no fundamental difference in depositing the mask before or after the patterning of the leads, as far as the quality of the contacts is concerned. This gives us the freedom to choose from case to case the more appropriate assembly strategy for the NW masks, according to the final device geometry and functionality. Shear-force contact printing,[7,30] spin-casting, or ink-jetting of NW suspensions[25,31] are all suitable techniques for large area assembly of single- and multiple-NW masks.

We first characterize a single SOI-NW as the fundamental building block for our architectures. In Figure 2 we compare the electronic transport through a single SOI-NW channel and through the original SOI film, using device geometries illustrated in Figure 2a (SOI film) and Figure 2b (SOI-NW). The source−drain gap (channel length, 1 μm) and the SOI layer thickness (channel height, 100 nm) are the same in both cases. The channel cross section is therefore uniquely determined by the channel width. This is the width of the contact fingers in the SIO film (10 μm), whereas it is set by the diameter of the original SiO_2 NW mask in the NWs (typically ∼40 nm). Figure 2c plots the gate voltage dependence of the channel conductance for both devices, scaled by the corresponding channel width. Since the original SOI layer is almost intrinsic, we always observe ambipolar behavior, i.e., accumulation of both holes and electrons occurs for negative and positive gate voltages, respectively. We also note that the transfer characteristics of the NW devices shift when the gate sweep is reversed, whereas those of the SOI film overlap. This hysteresis effect for NWs is well-known,[5,25,32,33] and is assigned to charge traps at the surface of the nanostructures, especially when measured in air without passivation.

Remarkably, Figure 2c shows that the normalized conductance for the single SOI-NW and the SOI film are comparable. The saturated ON current for holes scales with the channel cross section, indicating that the total resistance is dominated by the channel, not by the contacts. This is further confirmed by the output curves shown in Figure 2d (SOI film) and Figure 2e (SOI-NW). The current flowing through the NW is about 2 orders of magnitude lower than that flowing through the 200 times wider channel of the SOI film.

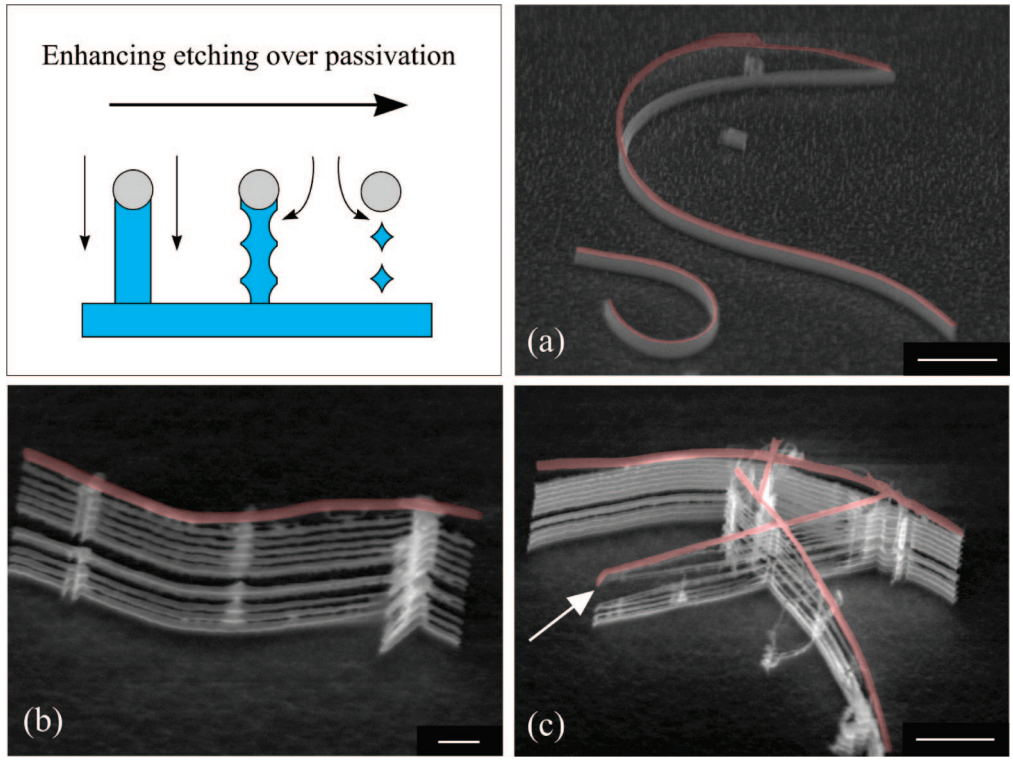

Figure 4. 3D architectures via NWL. (a) Si nanowalls etched into a ⟨100⟩ Si wafer. The oxidized NW mask (pink) is sometimes seen to "lift-off" because of charging effects under the SEM electron beam. Scale bar 2 μm. (b) Vertically stacked SiNWs obtained via controlled mask undercut. NWs height and separation is controlled by the DRIE etching parameters. Scale bar 100 nm. (c) Interconnected arrays of vertically stacked NWs obtained from overlapping NW mask. The arrow points at evidence of NWs mutual interaction, which tends to deform the aligned, parallel array. Scale bar 1 μm. The top-left diagram schematically illustrates the etching mechanisms leading to different architectures.

In addition, the output curves in Figure 2d show partial saturation, and a kink is visible also for the NW case (arrow in Figure 2e). Since the contact geometry is equivalent for SOI NWs and films, we extract the upper limit for the contact resistance (20 kΩ) from the ON state (for holes) of the film-based device. This is much smaller that the several hundred kiloohms commonly observed when depositing metal contacts directly on CS-NWs (with much smaller contact areas).[34,35]

We now consider crossed and netlike NW geometries as illustrated in Figure 3a−c. Figure 3d compares transfer curves measured for a SOI-NW channel, formed under a single NW mask directly bridging source and drain electrodes (Figure 3a), and for a monolithic SOI-NW cross obtained via the juxtaposition of two NW masks (Figure 3b). The contact gap is 1 μm for both devices. We note that the absolute ON currents are essentially the same, indicating that no significant resistance is introduced by the crossed junction geometry. In Figure 3e we assess the electronic transport through a SOI-NW network made of multiple crossing points. Here, we increase the separation between source and drain to 6 μm and compare a channel made of a few parallel NWs directly connecting the leads (direct bridge, similar to Figure 3a) with a NW percolation network etched through NW masks randomly assembled from solution (Figure 3c). Again, the curves are similar. The total current flowing through the SOI network does not degrade significantly. Monolithic networks prepared by NWL show therefore a great potential for highly conducting, large-area sensitive surfaces.

It is noteworthy that, compared with short-channel (1 μm) devices (Figure 3d), the ratio between hole/electron ON currents is reversed for the long-channel (6 μm) devices in Figure 3e. While the hole current is always higher in Figure 3d, the ON current for electrons becomes dominant as the channel length is increased, while the subthreshold slope for hole accumulation becomes less and less steep compared to electrons (from 2.5 V/dec in Figure 3d to 10 V/dec in Figure 3e). Such effects are not seen for devices fabricated on the original SOI layer (as in Figure 2a), and, consistently, are more pronounced for the percolating network (Figure 3e) as in this case the effective channel length is inevitably longer that for the direct bridge geometry. This shows that trapping of *positive* charges occurs at the NW surfaces, which results in a preferential n-type doping of the SOI-NW channels. This is in contrast to that reported in ref 36, where surface states appear to p-dope the Si NWs.

Lastly, we combine NWL with the flexibility of DRIE to achieve more complex 3D architectures. Indeed, we can transfer the morphology of a few nanometer thick SiO_2 NW into a Si wafer to achieve aspect ratios larger than 40. Figure 4a shows 1 μm deep Si nanowalls with their corresponding original NW masks (highlighted in dim pink). The resulting structures uniformly preserve the width of the original NW masks and exhibit very smooth lateral surfaces. The high selectivity of

the process allows etching depths up to 2–3 μm, before the NW masks start to show the onset of damage, due to the prolonged sputtering. If desired, however, a modulated undercutting can be intentionally induced by enhancing the etch step over the passivation one (see diagram in Figure 4). This leads to the formation of vertically stacked NWs, whose width is still controlled by the etching mask, while their height and separation (a few tens of nanometers in Figure 4b) reflect the periodicity of the etching cycles (Figure 4b). Figure 4c shows an interconnected array of stacked NW obtained from overlapping masks using the same process as for Figure 4b. We note that for this architecture the free-standing NW tips often tend to stick together due to mutual interaction (see arrow in Figure 4c). This effect may be suppressed, though, if the stacked NWs are clamped at both ends by a supporting bulk structure (for example, by depositing, before etching, protective pads on top of the masks, as in Figure 1b).

In summary, SiO_2 nanowires prepared by chemical methods represent a simple, compatible, and versatile system to implement nanowire lithography on bulk silicon or SOI structures. The electronic transport in nanowires fabricated by this approach is dominated by the channel geometry rather than by contact effects. Large-area, highly conductive nanowire percolation networks with single-crystalline bulk junctions are also demonstrated. An array of independent, vertically stacked nanowires can be obtained from a single mask by varying the silicon etching conditions. Applying nanowire lithography to silicon is thus an extremely promising and versatile solution to fabricate ultrasmall, large-area, and 3D architectures.

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Supporting Information Available: Figures showing SEM micrographs of nanowire lithography, Raman spectra of Si nanowires, and nanowalls. This material is available free of charge via the Internet at http://pubs.acs.org.

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