Top-Gated Silicon Nanowire Transistors in a Single Fabrication Step

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ARTICLE

ABSTRACT Top-gated silicon nanowire transistors are fabricated by preparing all terminals (source, drain, and gate) on top of the nanowire in a single step via dose-modulated e-beam lithography. This outperforms other time-consuming approaches requiring alignment of multiple patterns, where alignment tolerances impose a limit on device scaling. We use as gate dielectric the 10−15 nm SiO_2 shell naturally formed during vapor-transport growth of Si nanowires, so the wires can be implemented into devices after synthesis without additional processing. This natural oxide shell has negligible leakage over the operating range. Our single-step patterning is a most practical route for realization of short-channel nanowire transistors and can be applied to a number of nanodevice geometries requiring nonequivalent electrodes.

KEYWORDS: silicon nanowires · field-effect transistor · dual-gate · e-beam lithography · dose control

The growing research in silicon nanowires (SiNWs) for nanoelectronics applications has resulted in several NW-based devices, such as p−n junctions,[1,2] inversion- or accumulation-mode field-effect transistors (FETs),[3−7] and tunneling FETs.[2] Top-gated FET geometries, in particular, are crucial to probe the electrical properties of SiNWs because they allow stronger gate coupling when compared to back-gated devices.[2,7−11] However, patterning metal electrodes as FET terminals (source, drain, and gate) on top of a SiNW inevitably requires two lithography steps. After the preparation of source and drain leads, a suitable dielectric must be deposited on the exposed NW channel before a top-gate can be implemented.[2,8,10,12,13] The alignment of the second lithographic pattern is increasingly challenging for decreasing device size. Even small errors in defining the top-gate position can generate structural asymmetries and alter device behavior.[8] Thus, most reports on top-gated SiNW FETs focus on channel lengths well above 1 μm.[2,7,9,10,12−16]

An alternative process flow first produces an insulating shell around as-grown NWs, to serve as gate oxide, then fabricates the metal leads.[9,11,14,16] Such an oxide shell can be (a) conformally deposited by atomic layer deposition or sputtering;[9] (b) grown by postsynthesis thermal or wet oxidation;[11,16] and (c) formed during the growth process itself.[14] The latter is the most coherent solution within the bottom-up approach, where complex nanocomponents self-assemble with as limited intervention as possible from the macroscopic world. However, to ensure that source and drain terminals connect with the crystalline SiNW core, the insulating shell must be locally etched away. The gate electrode cannot thus be patterned in the same step as source and drain, but must be aligned and fabricated via a separate process.

Here, we show that top-gated SiNWs FETs can be achieved in a single patterning step by means of "grayscale" lithography, which exploits a dose-modulated exposure to control the speed of resist development.[17−20] This outperforms time-consuming approaches based on multiple patterns alignment, because downscaling device dimensions does not impose an increased fabrication effort. We use SiNWs with a self-formed oxide shell up to 10−15 nm in thickness, thus ensuring these can be implemented into devices after synthesis without additional processing. The natural oxide shell proves a suitable gate dielectric with negligible leakage over the operating range.

RESULTS AND DISCUSSION

Our detailed process flow to simultaneously fabricate source, drain, and gate terminals on a SiNW via single-pattern e-beam exposure is schematically

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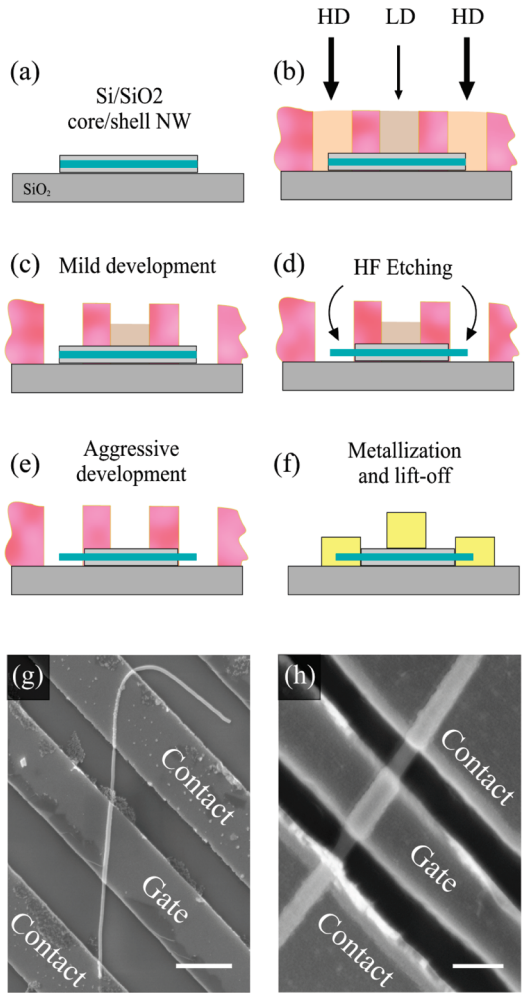

Figure 1. (a−f) Process to simultaneously fabricate source, drain, and gate terminals on a SiNW via single-pattern e-beam exposure. (g) SEM image of a long-channel (3 μm) top-gated SiNW FET. Scalebar: 1 μm. (h) SEM image of a short-channel (400 nm) top-gated SiNW FET. Scalebar: 200 nm.

illustrated in Figure 1. A 500 nm thick polymethyl methacrylate (PMMA) resist layer is spun on top of as-dispersed core−shell SiNWs (Figure 1a) and exposed under the electron beam using two different doses (Figure 1b). A dose of 1.15 mC/cm^2 (high-dose, HD) is used to define the contacts (source and drain), while a dose of 0.7 mC/cm^2 (low-dose, LD) is used to define the top-gate terminal in between. Samples are then developed in a methyl-isobutyl-ketone/2-propanol (MIBK/IPA) 1:3 solution for 20 s. These conditions ensure the HD pattern is fully developed, while the LD features are left partially undeveloped (Figure 1c). As a consequence, a residual resist layer protects the LD pattern from the 10 s etch in buffered HF (buffered oxide etching, BOE), which is used to strip away the oxide shell on the contact regions (Figure 1d). Then, a more aggressive solution (MIBK/IPA 1:1) is used to fully develop the LD features (Figure 1e). Finally, Ni is evaporated at the same time on the SiNW core, to form the source and drain contacts, and on the SiNW oxide shell, to yield a self-aligned top-gate terminal (Figure 1f). The plan-view scanning electron microscopy (SEM) images in Figure 1g,h show two resulting top-gated SiNW FETs with total channel lengths of 3 μm (long-channel) and 400 nm (short-channel), respectively. Note that the metal-covered NW section below the gate electrode is slightly thicker compared to those below the neighboring contacts, because the original oxide shell is still present at the gate in order to isolate the NW from the metal lead.

The process flow described in Figure 1 yields working devices. However, they have a high contact resistance limiting the FET ON current to about 1 nA. This may arise because of ambient reoxidation of the SiNW core after HF etching or because the fresh SiNW crystalline surface is prone to contamination by the aggressive developer solution. We find that, between steps (e) and (f) in Figure 1, a further 2 s BOE etch is effective in restoring a clean Si surface on the HD NW sections prior to metallization, while no significant damage is caused to the >10 nm thick gate oxide on the LD pattern. Our BOE etch calibrations[5] indicate a thinning of the gate oxide of max 2−3 nm. We thus adopt this procedure in the following.

For bottom-gated, Schottky-barrier FETs made of SiNWs synthesized by vapor-transport and contacted with Ni leads, a back-gate sweep generally produces ambipolar transfer characteristics.[5,11,21] Dual-gate FET geometries fabricated with our process (with a top-gate electrode on the NW and the substrate used as bottom-gate) allow a more extensive electrical characterization due to the various combinations offered by the interplay of the gate potentials.[11,15] Figure 2 plots transfer curves (drain current I_D, as a function of gate voltage) recorded by sweeping the bottom-gate voltage (V_{BG}), with the top-gate (V_{TG}) kept between 0.25 and 1.75 V. In all cases, the source-drain voltage (V_{DS}) is set to 1 V. As a convention, we consider the grounded terminal as source and the biased terminal as drain so that V_{DS} represents the drain potential.

Figure 2 shows that we can choose a V_{TG} to selectively suppress hole or electron conduction, transforming a back-gated ambipolar FET in a unipolar n-type or p-type FET, respectively. The insets in Figure 2 schematize the band diagrams corresponding to the ON and OFF states for the highest and lowest V_{TG}. The band pinning at the Schottky contacts due to the back-gate sweep is sufficient to inject either holes or electrons into the NW[5,11,15,21] (see cyan curve, for example), but if V_{TG} is too high (low), a barrier is formed in the center of the NW that hinders the transmission of holes (electrons). A similar trend is reported in ref 15 for SiNW channels fabricated via top-down processing, thus showing the ease of our method in producing effective dual-gated FETs from SiNWs grown by chemical methods.

In Figure 3a,b we plot several output curves (I_D *vs* V_{DS}) for the FET assessed in Figure 2. In particular, we

consider the ON state for holes (Figure 3a, $V_{BG} = -40$ V) and electrons (Figure 3b, $V_{BG} = +40$ V) and investigate the I_D response to the applied bias as a function of the top-gate potential. Note that the fabrication of Schottky contacts on intrinsic SiNWs leads to nonlinear output characteristics.[22,23] Therefore, it is not surprising that in Figure 3 I_D increases exponentially with V_{DS} in the proximity of the origin. However, we note that output curves are strongly nonsymmetric when reversing V_{DS}. In Figure 3a, for example, there is almost no conduction for negative V_{DS} if the top-gate voltage is set to 0.1−0.3 V. A similar effect occurs in Figure 3b for positive V_{DS} as V_{TG} is kept at 0.7−0.9 V. This can be understood by considering the schematic band diagrams for $V_{DS} < 0$ and $V_{DS} > 0$, as shown in the insets of Figure 3. A local band shift occurs where an electric field is applied along the channel. In fact, the band bending induced by the bottom-gate field affects the whole NW. The additional shift (or countershift, to build up a barrier) induced by the top-gate is restricted to the central part of the channel and is thus a function of the *relative* potential difference between the top-gate and the underlying SiNW section. As V_{DS} varies from +1 to −1 V for fixed V_{TG}, the potential at the NW center (V_{CW}) changes as well, reinforcing or compensating for the top-gate field and, therefore, resulting in a different barrier height ($\Delta = f(V_{TG} - V_{CW})$). As a consequence, carrier transport can be suppressed in one direction only. This effect fades as V_{TG} becomes strong enough (lower than 0 V in (a) and higher than 1.0 V in (b)) to lower the barrier below the Fermi level, irrespective of V_{CW}, so conduction resumes in both directions. We thus conclude that, by choosing a proper combination of V_{BG} and V_{TG}, an individual SiNW device can be operated as a diode of controllable and reversible polarity.

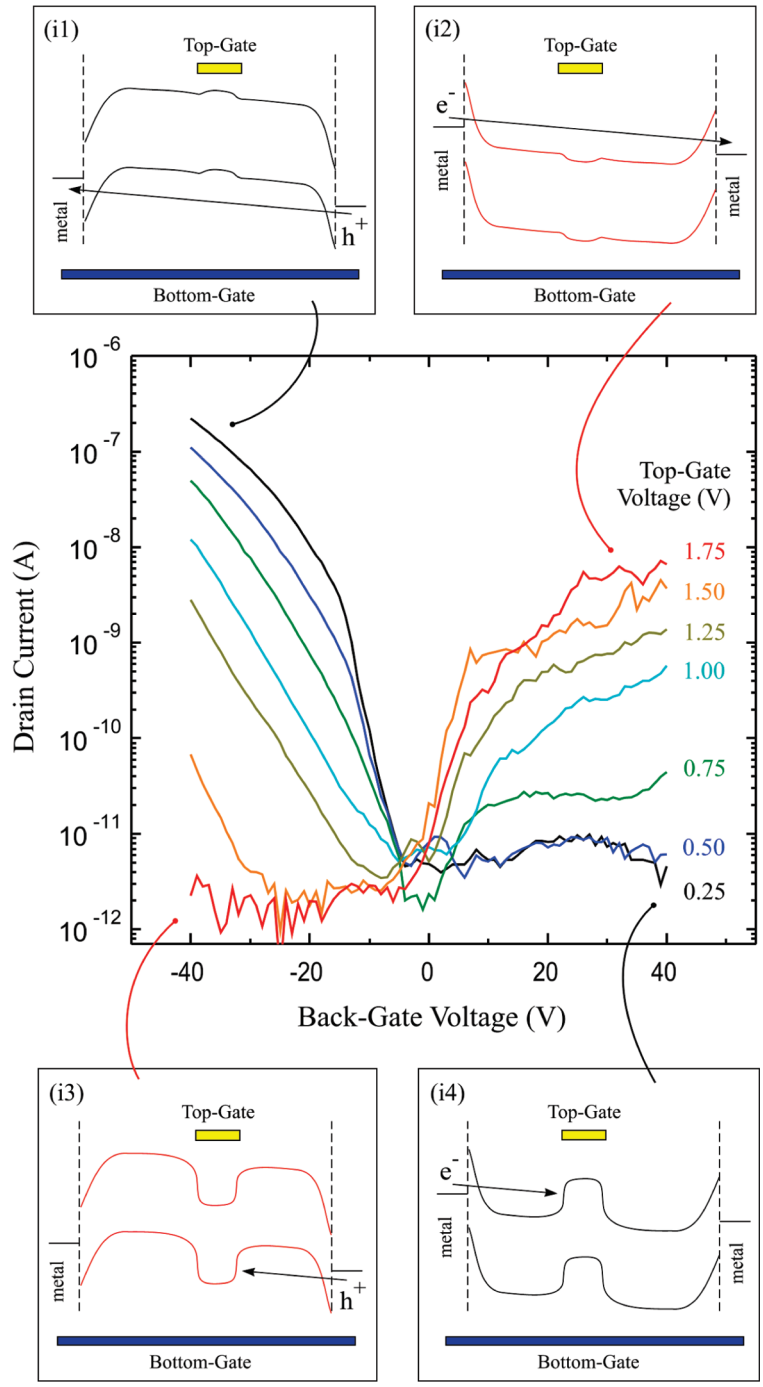

Figure 2. Bottom-gate transfer curves (I_D *vs* V_{BG}) recorded for V_{TG} from 0.25 to 1.75 V, showing a progressive enhancement (suppression) of electron (hole) conduction. Insets (i1−i4): band diagrams corresponding to ON and OFF states for highest and lowest V_{TG}. Channel length = 3 μm. V_{DS} = 1 V.

As an alternative to Figure 2, it is more desirable during operation to switch the FET using the top-gate, as the better coupling ensures lower threshold voltages and steeper subthreshold slopes. In this configuration it is also important to emphasize small differences in electrical behavior due to device scaling. Figure 4a,b plot transfer curves (I_D *vs* gate voltage) recorded by sweeping V_{TG}, while V_{BG} is kept at −40 V and +40 V, respectively. In all cases, V_{DS} is set to 1 V. Both long- and short-channel devices behave as p-type FETs in Figure 4a and as n-type FETs in Figure 4b. For long-channels, the corresponding inverse subthreshold slopes [$dV_{TG}/d(\text{Log } I_D)$] for hole and electron accumulation are 135 and 230 mV/dec, respectively. These are comparable to the best top-gated NW FETs to date.[7−9,11,16] For short-channel devices, we observe a slight ambipolar behavior in Figure 4a,b, coupled with higher OFF currents and a degradation of the p-type subthreshold slope in Figure 4a.

In Figure 4, the fixed bottom-gate voltage controls the type of carriers injected at the contacts[11,15] and can thus transform on-demand the same device either to a hole- or electron-conducting FET. For long-channels (>1 μm), if a top-gate is implemented midchannel, as in Figure 1g, this has negligible effect on the Schottky

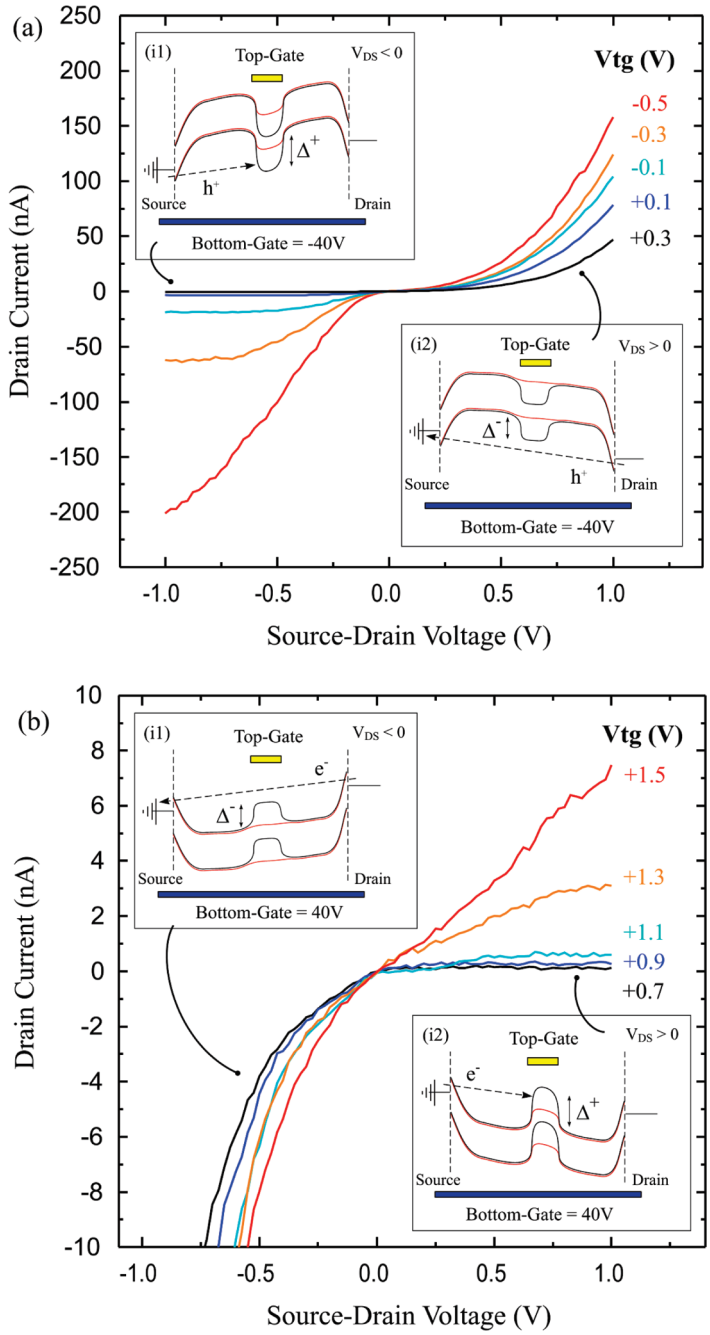

Figure 3. Output curves (I_D *vs* V_{DS}) recorded for fixed V_{BG} of (a) −40 V and (b) +40 V. The top-gate voltage is varied between −0.5 and 0.3 V in (a) and from 0.7 to 1.5 V in (b). The insets show the band diagrams corresponding to the maximum and minimum V_{TG} for both positive and negative V_{DS}. Channel length = 3 μm.

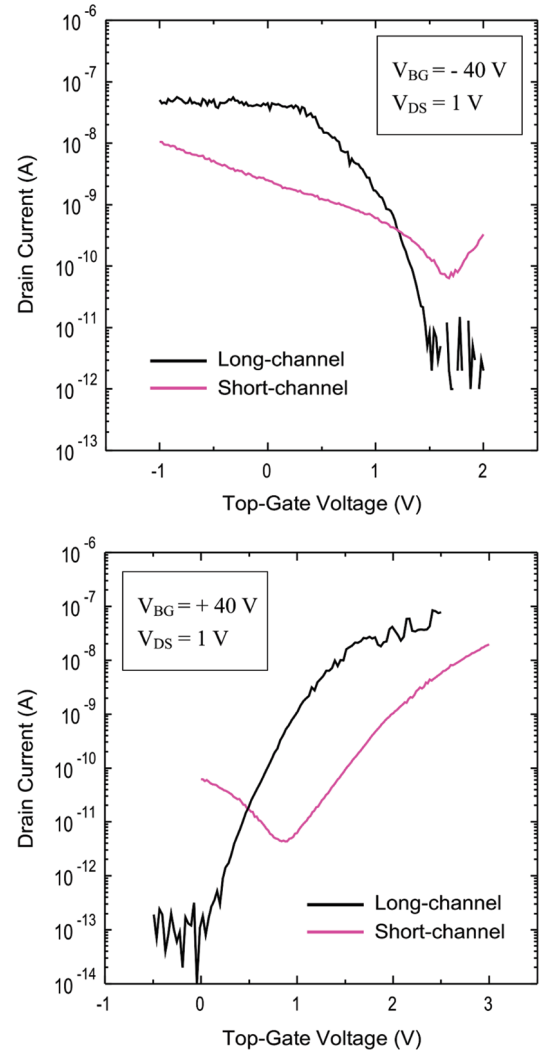

Figure 4. Top-gate transfer curves (I_D *vs* V_{TG}) for a fixed V_{BG} of (a) −40 V and (b) +40 V. In all cases, V_{DS} = 1 V. Both long- and short-channel devices behave as p-type FETs in (a) and as n-type in (b).

barriers but only controls charge accumulation/depletion in the central portion of the NW. However, if the separation between top-gate and contacts becomes too narrow (as, *e.g.*, 100 nm in our short-channel FET in Figure 1h), the top-gate effect on the contacts may be no longer negligible. This is known to yield higher OFF currents and ambipolar behavior,[8] as in Figure 4. The reason for the lower p-type subthreshold slope (Figure 2a), which also leads to a lower ON current, remains unclear. Scaling down device dimensions is likely to result in enhanced mutual screening between terminals, affecting field penetration[23] and making a direct comparison with long-channel SiNW FETs more difficult.

In Figure 5 we investigate the breakdown strength of our SiO_2 dielectric by measuring the leakage current between a gate terminal and a contact (Figure 5a). In such a configuration, our circuit can be seen as a series of three resistors: the oxide gate barrier (R_{OX}), the NW itself (R_W) and the NW-contact junction (R_C; Figure 5b). To ensure the whole potential drops across R_{OX}, we switch ON the NW channel by applying a large voltage (±50 V) to the bottom-gate. This ensures that $R_W + R_C \ll R_{OX}$, no matter if conduction is via holes or electrons.[24] Statistically, we note that our SiO_2 gate dielectric can exhibit two different responses. In one case (device 1 in Figure 5c), the leakage current (I_{TG}) increases continuously and reversibly, roughly following an exponential law, to reach values of several tens of nA when up to 20 V are applied between the terminals. Alterna-

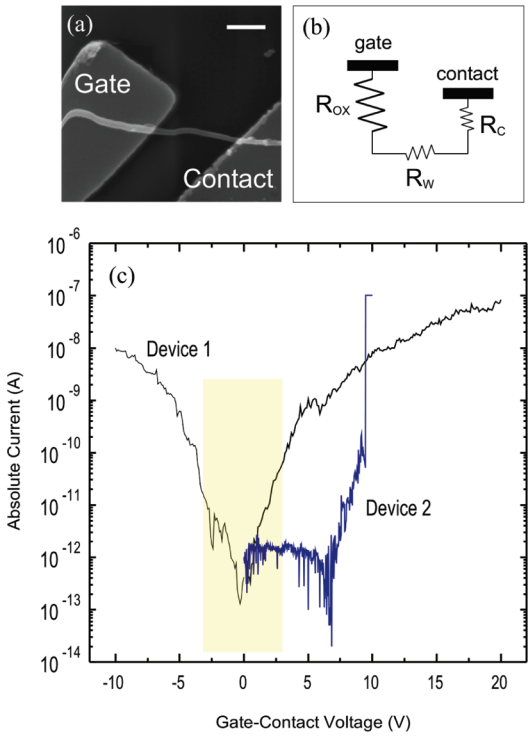

Figure 5. (a) SEM image of a gate-contact NW device used for breakdown measurements. Scalebar: 400 nm. (b) Schematic of the circuit. (c) Breakdown characteristics of the SiNW oxide shell used as gate dielectric. Statistically, leakage through the gate oxide can occur either via a progressive and reversible current ramp (device 1) or via catastrophic, irreversible breakdown (device 2, compliance set to 10^{-7} A). In the FET operational range (yellow bar), the leakage current remains steadily below 100 pA.

tively, some devices (labeled 2 in Figure 5c) initially show a higher resistance but reach breakdown when a critical voltage (>8 V) is exceeded. We, thus, see that, in our operational range (-3 V $< V_{TG} <$ 3 V, highlighted in Figure 5c by the yellow bar), no gate breakdown occurs and the leakage current always remains below 100 pA.

The good electrical properties shown in Figures 4 and 5 indicate the feasibility of using our self-formed SiO_2 shell as the gate oxide, avoiding the necessity for oxide fabrication by conventional methods,[2,11,16] yet achieving comparable dielectric performances. Note that when ref 14 used the Ga_2O_3 amorphous shell surrounding as-grown GaP NWs as a gate dielectric for FET applications, they found a rectifying behavior between gate-source terminals with a leakage current of several nA for a forward bias of 2−3 V.[14] This is not seen for our Si/SiO_2 core/shell NWs, because a bias sweep toward negative voltages produces a symmetric response (Figure 5c, device 1). We also note that, for a shell thickness of ~10 nm, an ~8 V breakdown voltage corresponds to a field of $\sim 8 \times 10^6$ V/cm. This is close to the standard breakdown field reported for SiO_2 ($\sim 10^7$ V/cm [25]), indicating the high-quality of our intrinsic oxide shell.

CONCLUSIONS

We have shown how to fabricate top-gated SiNW FETs with simple and minimal processing. This is achieved by using as gate dielectric the SiO_2 shell naturally formed during the vapor-transport growth of SiNWs and preparing all FET terminals in a single patterning step via dose-modulated e-beam lithography. Our results demonstrate that this approach does not introduce fundamental drawbacks in terms of device performance and, thus, represents a most practical strategy toward large-scale and high-throughput fabrication of short-channel SiNW devices. Our single-step patterning could be generalized to several nanodevice geometries requiring nonequivalent electrodes, including radial NW heterostructures[26,27] or more advanced FET configurations with, for instance, high-k or polymer-based gate dielectrics.[8,28]

EXPERIMENTAL SECTION

We grow SiNWs by Au-catalyzed vapor-transport as described in ref 22. These samples were thoroughly investigated before, as reported in refs 5, 21, 22, 29, and 30. This method naturally results in Si/SiO_2 core/shell NWs with a ratio of roughly 1:1 between the crystalline core radius (r_C) and the oxide shell thickness (t_{OX}).[5,22,31] Unlike SiNWs grown by chemical-vapor deposition, where a ~1−2 nm thick native oxide layer is formed upon exposure to atmosphere,[22,32] our thick oxide shell arises from phase-separation of SiO into Si and SiO_2 when the precursor vapor condenses to form SiNWs at temperatures around 800 °C.[22,31] In this study, we use SiNWs with $r_C = t_{OX} = 10-15$ nm.[5] The overall NW diameter is thus in the 40−60 nm range, as can be deduced from the SEM image in Figure 1h. Figure 6 is a representative high-resolution transmission electron microscopy (TEM) micrograph showing the core/shell Si/SiO_2 structure of our SiNWs. After synthesis, SiNWs are mechanically transferred[21,33] onto a 200 nm thick SiO_2 layer thermally grown on top of a heavily doped Si wafer, used as bottom gate. FET terminals are then defined on top of individual SiNWs by e-beam lithography, followed by evaporation of 70 nm of Ni. Electrical measurements are taken with a Cascade Microtech probe station coupled to an Agilent B1500A device analyzer.

Our devices are annealed at 400 °C in forming gas for 4 min prior to measurements. References 11 and 23 pointed out that upon annealing Ni can diffuse in the SiNW to form silicide contacts. Even if ref 11 reported that this effect is significant for annealing temperatures as low as 290 °C, we have evidence (see Supporting Information) that no exposed section of our NW is converted to nickel silicide at 400 °C. We do detect silicidation at 470 °C instead, as for ref 23. Consequently, in the present work, any improvement to the contact quality as a result of annealing is therefore restricted to the metallurgical interface. Yet, the formation of silicide contacts of controllable length may be an effective strategy to allow superposition of the contacts with the top-gate terminal. Coupling between top-gate and contact barriers can also be achieved with small (<100 nm) gaps between the terminals, as seen in Figure 4 for short-channel devices. Hence, the fact that our one-step fabrication strategy does not allow a physical superposition of the metal leads is not a fundamental limitation. One or more top-gates can effectively operate the NW device without need for a bottom-gate, which is

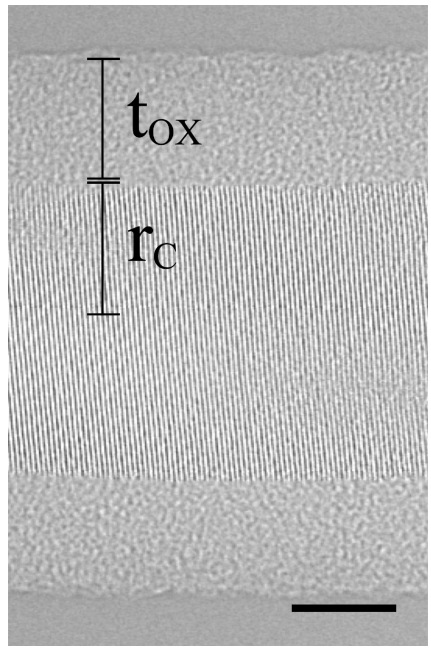

Figure 6. High-resolution TEM micrograph of a SiNW showing the crystalline core and the thick amorphous shell. Scale-bar is 10 nm.

convenient for basic electrical characterization but unpractical for scaled-up device applications.

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Supporting Information Available: Discussion on the effect of annealing on nickel/silicon nanowire contacts and additional figures. This material is available free of charge *via* the Internet at http://pubs.acs.org.

REFERENCES AND NOTES

1. Huang, Y.; Duan, X.; Cui, Y.; Lauhon, L. J.; Kim, K.-H.; Lieber, C. M. Logic Gates and Computation from Assembled Nanowire Building Blocks. *Science* **2001**, *294*, 1313–1317.
2. Bjork, M. T.; Knoch, J.; Schmid, H.; Riel, H.; Riess, W. Silicon Nanowire Tunneling Field-Effect Transistors. *Appl. Phys. Lett.* **2008**, *92*, 193504.
3. Li, Y.; Qian, F.; Xiang, J.; Lieber, C. M. Nanowire Electronic and Optoelectronic Devices. *Mater. Today* **2006**, *9*, 18–27.
4. Hayden, O.; Bjork, M. T.; Schmid, H.; Riel, H.; Drechsler, U.; Karg, S. F.; Lortscher, E.; Riess, W. Fully Depleted Nanowire Field-Effect Transistor in Inversion Mode. *Small* **2007**, *3*, 230–234.
5. Colli, A.; Fasoli, A.; Ronning, C.; Pisana, S.; Piscanec, S.; Ferrari, A. C. Ion Beam Doping of Silicon Nanowires. *Nano Lett.* **2008**, *8*, 2188–2193.
6. Colli, A.; Fasoli, A.; Pisana, S.; Fu, Y.; Beecher, P.; Milne, W. I.; Ferrari, A. C. Nanowire Lithography on Silicon. *Nano Lett.* **2008**, *8*, 1358–1362.
7. Ho, T.-T.; Wang, Y.; Eichfeld, S.; Lew, K.-K.; Liu, B.; Mohney, S. E.; Redwing, J. M.; Mayer, T. S. In Situ Axially Doped n-Channel Silicon Nanowire Field-Effect Transistors. *Nano Lett.* **2008**, *8*, 4359–4364.
8. Xiang, J.; Lu, W.; Hu, Y.; Wu, Y.; Yan, H.; Lieber, C. M. Ge/Si Nanowire Heterostructures as High-Performance Field-Effect Transistors. *Nature* **2006**, *441*, 489–493.
9. Zhang, L.; Tu, R.; Dai, H. Parallel Core-Shell Metal-Dielectric-Semiconductor Germanium Nanowires for High-Current Surround-Gate Field-Effect Transistors. *Nano Lett.* **2006**, *6*, 2785–2789.
10. Kim, H.-J.; Lee, C.-H.; Kim, D.-W.; Yi, G.-C. Fabrication and Electrical Characteristics of Dual-Gate ZnO Nanorod Metal-Oxide Semiconductor Field-Effect Transistors. *Nanotechnology* **2006**, *17*, S327−S311.
11. Appenzeller, J.; Knoch, J.; Tutuc, E.; Reuter, M.; Guha, S. Dual-Gate Silicon Nanowire Transistors with Nickel Silicide Contacts. *International Electron Devices Meeting* **2006**, *1*−*2*, 302–305.
12. Wang, D.; Wang, Q.; Javey, A.; Tu, R.; Dai, H.; Kim, H.; Mcintyre, P. C.; Krishnamohan, T.; Saraswat, K. C. Germanium Nanowire Field-Effect Transistors with SiO_2 and High-k HfO_2 Gate Dielectrics. *Appl. Phys. Lett.* **2003**, *83*, 2432–2434.
13. Keem, K.; Kang, J.; Yoon, C.; Yeom, D.; Jeong, D.-Y.; Moon, B.-M.; Kim, S. A Fabrication Technique for Top-Gate ZnO Nanowire Field-Effect Transistors by a Photolithography Process. *Microelectron. Eng.* **2007**, *84*, 1622–1626.
14. Kim, B.-K.; Kim, J.-J.; Lee, J.-O.; Kong, K.-J.; Seo, H. J.; Lee, C. J. Top-Gated Field-Effect Transistor and Rectifying Diode Operation of Core-Shell Structured GaP Nanowire Devices. *Phys. Rev. B* **2005**, *71*, 153313.
15. Koo, S.-M.; Li, Q.; Edelstein, M. D.; Richter, C. A.; Vogel, E. M. Enhanced Channel Modulation in Dual-Gated Silicon Nanowire Transistors. *Nano Lett.* **2005**, *5*, 2519–2523.
16. Liu, B.; Wang, Y.; Ho, T.-T.; Lew, K.-K.; Eichfeld, S.; Redwing, J. M.; Mayer, T. S.; Mohney, S. E. Oxidation of Silicon Nanowires for Top-Gated Field Effect Transistors. *J. Vac. Sci. Technol., A* **2008**, *26*, 370–374.
17. Hu, F.; Lee, S.-Y. Dose Control for Fabrication of Grayscale Structures Using a Single Step Electron-Beam Lithographic Process. *J. Vac. Sci. Technol., B* **2003**, *21*, 2672–2679.
18. Lee, S.-Y.; Anbumony, K. Accurate Control Of Remaining Resist Depth for Nanoscale Three-Dimensional Structures in Electron-Beam Grayscale Lithography. *J. Vac. Sci. Technol., B* **2007**, *25*, 2008–2012.
19. Girgis, E.; Liu, J.; Benkhedar, M. L. Fabrication Of Metallic Air Bridges Using Multiple-Dose Electron Beam Lithography. *Appl. Phys. Lett.* **2006**, *88*, 202103.
20. Gorbachev, R. V.; Mayorov, A. S.; Savchenko, A. K.; Horsell, D. W.; Guinea, F. Conductance of p-n-p Graphene Structures with Air-Bridge Top Gates. *Nano Lett.* **2008**, *8*, 1995–1999.
21. Colli, A.; Pisana, S.; Fasoli, A.; Robertson, J.; Ferrari, A. C. Electronic Transport in Ambipolar Silicon Nanowires. *Phys. Status Solidi B* **2007**, *244*, 4161–4164.
22. Colli, A.; Fasoli, A.; Beecher, P.; Servati, P.; Pisana, S.; Fu, Y.; Flewitt, A. J.; Milne, W. I.; Robertson, J.; Ducati, C.; De Franceschi, S.; Hofmann, S.; Ferrari, A. C. Thermal and Chemical Vapor Deposition of Si Nanowires: Shape-Control, Dispersion and Electrical Properties. *J. Appl. Phys.* **2007**, *102*, 034302.
23. Weber, W. M.; Geelhaar, L.; Graham, A. P.; Unger, E.; Duesberg, G. S.; Liebau, M.; Pamler, W.; Cheze, C.; Riechert, H.; Lugli, P.; Kreupl, F. Silicon-Nanowire Transistors with Intruded Nickel-Silicide Contacts. *Nano Lett.* **2006**, *6*, 2660–2666.
24. An upper limit for $R_W + R_C$ can be extracted from the saturation on currents in Figure 4 ($\sim 10^{-7}$ A at $V_{DS} = 1$ V means $R_W + R_C \sim 10^7\ \Omega$). From Figure 5 we note that $R_{OX} + R_W + R_C > 10^9 - 10^{10}\ \Omega$, thus, the condition $R_{OX} \gg R_W + R_C$ is fulfilled.
25. Sze, S. M. *Physics of Semiconductor Devices*; Wiley: New York, 1981.
26. Lauhon, L. J.; Gudiksen, M. S.; Wang, D.; Lieber, C. M. Epitaxial Core-Shell and Core-Multishell Nanowire Heterostructures. *Nature* **2002**, *420*, 57–61.
27. Qian, F.; Gradecak, S.; Li, Y.; Wen, C.-Y.; Lieber, C. M. Core/Multishell Nanowire Heterostructures as Multicolor, High-Efficiency Light-Emitting Diodes. *Nano Lett.* **2005**, *5*, 2287–2291.

28. Lai, Q.; Li, Z.; Zhang, L.; Li, X.; Stickle, W. F.; Zhu, Z.; Gu, Z.; Kamins, T. I.; Williams, R. S.; Chen, Y. An Organic/Si Nanowire Hybrid Field Configurable Transistor. *Nano Lett.* **2008**, *8*, 876–880.
29. Hofmann, S.; Ducati, C.; Neill, R. J.; Piscanec, S.; Ferrari, A. C.; Geng, J.; Dunin-Borkowski, R. E.; Robertson, J. Gold Catalyzed Growth of Silicon Nanowires by Plasma Enhanced Chemical Vapor Deposition. *J. Appl. Phys.* **2003**, *94*, 6005–6012.
30. Piscanec, S.; Cantoro, M.; Ferrari, A. C.; Zapien, A.; Lifshitz, Y.; Lee, S. T.; Hofmann, S.; Robertson, J. Raman Spectroscopy of Silicon Nanowires. *Phys. Rev. B* **2004**, *68*, 241312(R).
31. Kolb, F. M.; Hofmeister, H.; Scholz, R.; Zacharias, M.; Gosele, U.; Ma, D. D.; Lee, S. T. Analysis of Silicon Nanowires Grown by Combining SiO Evaporation with the VLS Mechanism. *J. Electrochem. Soc.* **2004**, *151*, G472−G475.
32. Cui, Y.; Lauhon, L. J.; Gudiksen, M. S.; Wang, J.; Lieber, C. M. Diameter-Controlled Synthesis of Single-Crystal Silicon Nanowires. *Appl. Phys. Lett.* **2001**, *78*, 2214–2216.
33. Javey, A.; Nam, S. W.; Friedman, R. S.; Yan, H.; Lieber, C. M. Layer-by-Layer Assembly of Nanowires for Three-Dimensional, Multifunctional Electronics. *Nano Lett.* **2007**, *7*, 773–777.