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Resistive Switching Crossbar Arrays Based on Layered Materials

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Resistive switching (RS) devices are metal/insulator/metal cells that can change their electrical resistance when electrical stimuli are applied between the electrodes, and they can be used to store and compute data. Planar crossbar arrays of RS devices can offer a high integration density (>10^8 devices mm^{-2}) and this can be further enhanced by stacking them three-dimensionally. The advantage of using layered materials (LMs) in RS devices compared to traditional phase-change materials and metal oxides is that their electrical properties can be adjusted with a higher precision. Here, the key figures-of-merit and procedures to implement LM-based RS devices are defined. LM-based RS devices fabricated using methods compatible with industry are identified and discussed. The focus is on small devices (size < 9 μm^2) arranged in crossbar structures, since larger devices may be affected by artifacts, such as grain boundaries and flake junctions. How to enhance device performance, so to accelerate the development of this technology, is also discussed.

1. Introduction

Some materials can change electrical resistance between two values when they are exposed to controlled electrical stimuli.[1] This property, called resistive switching (RS), has attracted the attention of the semiconductors industry[2] because it may be used to emulate the ones and zeros of the binary code, therefore to store digital information.[3] In order to use RS materials to fabricate electronic memories that could compete with the mainstream commercial ones (i.e., NAND flash and dynamic random access memory), some technological requirements need to be met. The most important are (**Table 1**): 1) the resistance in high resistive state (HRS, i.e., R_{HRS}) should be at least ten times higher than that of the low resistive state (LRS, i.e., R_{LRS}), so that both can be read reliably;[4–6] 2) the switching time should be <1 ns,[4–6] so that they can be used to store information produced by integrated circuits operating at high clock frequencies (>1 GHz); 3) the switching energy should be <1 pJ,[4–6] so that the overall energy consumption is low (<1 pJ), to minimize ventilation and enable their use in wearable and self-powered technologies; 4) the material should be able to switch between the two resistive states at least 10^{12} times before one of them becomes permanent, i.e., 2×10^{12} transitions, half from HRS to LRS (i.e., set) and half from LRS to HRS (i.e., reset), so that the lifetime of the memory can be in the order of years. This property is often called switching endurance;[4–6] 5) each resistive state needs to be stable for at least 10 years (at 85 °C) if no electrical stimuli are applied, so that no data is lost. This is often called state retention time;[4–6] 6) RS needs to be demonstrated in small areas (<100 nm^2), so that high integration >10^{11} bits cm^{-2} can be achieved.[4–6]

The main parameters of RS devices are: 1) switching voltages (V_{SET}, V_{RESET}), 2) state resistances (R_{HRS}, R_{LRS}), 3) switching times (t_{SET}, t_{RESET}), 4) switching energy (E_{SET}, E_{RESET}), and 5) state retention time (t_{HRS}, t_{LRS}). These can change from one cycle to another (for the same device[5,11]), and from one device to another.[5,11] The variations of these parameters can be quantified by calculating the coefficient of variance (C_V), i.e., the standard deviation divided by the mean value.[12,13] Each RS technology allows a degree of variability of device parameters, and a range of acceptable values (often called operation window).[6,11] The devices that cannot be operated reliably within this window produce failure and reduce yield, i.e., the percentage of devices with parameters within the operation window.[14] In general, most RS technologies require high yields >90%,[15,16] although most studies do not disclose data about the yield pass criteria, hence making reliable comparisons difficult. As of 2022, there is no RS device exhibiting (simultaneously) all the performances required for high-integration electronic memories (see Table 1). For RS memories some parameters are even better than for NAND flash, but the maximum integration

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Table 1. Performance of commercial RS-based memories. "—" means that data is not provided by the manufacturer. To the best of our knowledge, none of the manufacturers discloses yield. Switching energy = power × switching time. The material used as RS medium is indicated in the top row.

	NAND flash	RS memory [magnetic]	RS memory [phase-change]	RS memory [metal oxide]
Manufacturer	Cobham[7]	Everspin[8]	Intel/Micron[9]	Fujitsu[10]
R_{HRS}/R_{LRS}	—	—	—	250
Switching time	20 ns	≈10 ns	10–100 ns	10 ns
Switching energy	<6 nJ	≈10 pJ	≈10 pJ	24 nJ
Endurance	4×10^4	10^{15}	$\approx 10^7$	10^6
Retention time	>10 years	>10 years	>10 years	>10 years
Integration density	4 TB	≈1 GB	256 GB	8 MB

densities achieved are rather poor. For this reason, RS-based electronic memories are still not being used for high-density (>10^8 bits mm^{-2}) non-volatile digital information storage (most products still rely on the NAND flash memory unit[17,7]), and the segment of the memory market covered by RS memories is still very small (≈0.32% in 2020).[4]

State-of-the-art RS devices are made of phase-change materials, metal oxides (MO), or magnetic materials,[4,5,8,9] and these are the only materials used to date by leading companies like Everspin,[8] Intel,[9] TSMC,[18] and IMEC.[19] Organic materials,[20] quantum dots,[21,22] and sulfides[23,24] were also used for RS, however fabrication of crossbar arrays was not reported, which means that they are limited to a proof-of-concept RS observation and their impact in commercial RS technologies is negligible. The material systems that so far have achieved the best performance (i.e., lowest switching time and energy and highest endurance and retention time) when used as RS memories are crossbar arrays of vertical metal/insulator/metal (MIM) nanocells (**Figure 1**a). When an external bias is applied, the conductance of RS devices is modified through atomic rearrangements in the MIM nanocells, which can follow various physical phenomena: 1) phase-change,[25] 2) metallic ion penetration from electrodes,[26,27] oxygen vacancies formation, or electron trapping and de-trapping[28] in metal oxides,[29] 3) spin modification.[30,31] Electrical-field-driven thermal effects can also play a role in accelerating such atomic rearrangements,[32] therefore thermal conductivity is important. The atomic rearrangements can be distributed equally within the entire volume of the RS device,[33] or localized at the interfaces,[34] grain boundaries (GBs),[35–36] across a conductive nanofilament (CNF),[1] or at a single atomic dislocation.[37] To the best of our knowledge, the exact materials composition of commercial RS products (i.e., memories) is unknown, because companies do not reveal such information.

As of 2022, all RS devices still suffer from a too high device-to-device variability, meaning that for a large (>10^6) population of devices it is still impossible to ensure that the minimum R_{HRS} ($R_{HRS.MIN}$) will be greater than ten times the maximum R_{LRS} ($R_{LRS.MAX}$), for all cycles in all devices (see **Figure 2**). Every time one cycle of one device does not meet this criterion, erroneous data is stored and/or read (see gray arrows in Figure 2c). Reaching $R_{HRS.MIN}/R_{LRS.MAX}$ >10 for all cycles of all devices is easier when the number of devices is lower (<10^6), which has enabled the use of RS devices in sensors,[39] photodetectors,[40,41] and low-density (<100 megabytes) memories.[10,42] However, device-to-device variability is hindering the implementation of RS devices as mainstream memory for high-density (>10^{11} bits cm^{-1}) information storage (in the gigabyte range). Moreover, when one MIM cell within the crossbar array is addressed (by applying electrical stimuli to one row and one column[1]), the surrounding MIM cells are also exposed to part of the electrical stress, which creates additional paths for current flow from one electrode to another (often called sneak paths or sneak currents).[43] In order to control better the current flow across each cell (i.e., minimize variability and sneak currents), one common solution is to connect additional electronic devices in series to each MIM-like RS device in the crossbar array, such as transistors[44,45] (leading to 1-transistor–1-resistor [1T1R] configurations[44]) or selectors

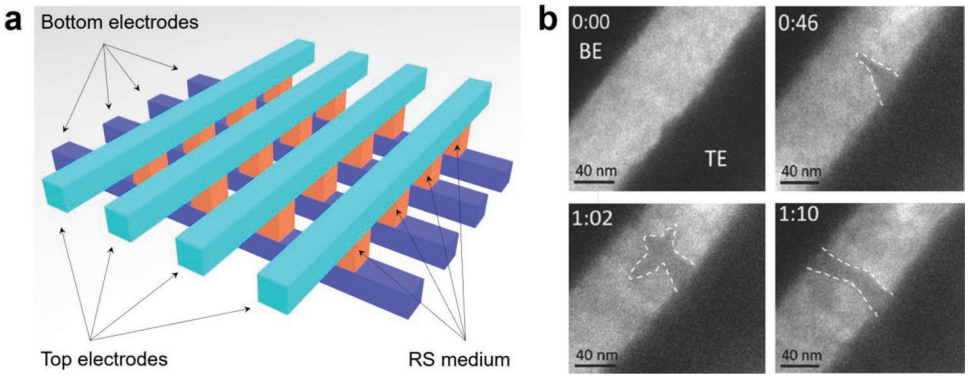

Figure 1. Structure of state-of-the-art RS crossbar arrays based on metal/MO/metal cells. a) Schematic of crossbar array. b) Cross-sectional TEM images of RS device at different times (top-left number in each panel), in which the CNF formation process is seen. BE = bottom electrode; TE = top electrode. b) Reproduced with permission.[38] Copyright 2013, American Chemical Society.

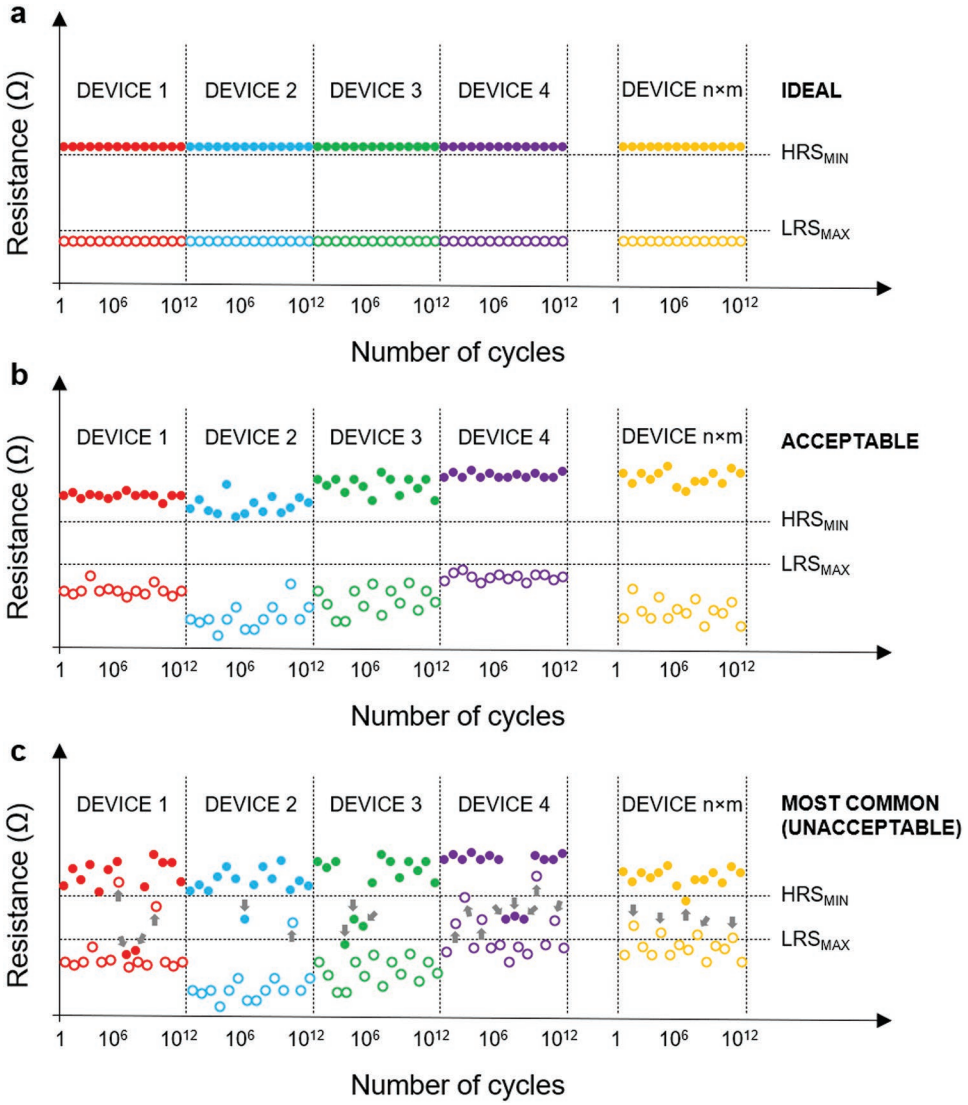

Figure 2. Main challenge of RS-based technologies: device-to-device variability. Schematic resistance versus cycle plots for crossbar arrays of MIM nanocells with *n* rows and *m* columns. a) ideal; b) acceptable characteristics; c) most common (but unacceptable) characteristics, where the resistive states producing errors are indicated with a gray arrow. The key challenge is for HRS_{MIN} to be at least ten times more resistive than LRS_{MAX}.

(leading to 1-selector-1-resistor [1S1R] configurations[46]). These elements can also serve as immediate current limitations (i.e., without delay time), which is beneficial to avoid undesired overshoot current (i.e., a short-time current above the pre-set current limitation until this enters in operation), enhancing the lifetime of the devices. The integration of crossbar arrays of MIM-like RS devices with these additional elements (or with other logic circuits necessary at the system level) does not necessary represent an increase of area, as MIM-like RS devices can be integrated on the back-end-of-line (BEOL) interconnections of the transistors,[47] and selectors are two-terminal devices that can be placed on top/bottom of the RS device.[46] Nevertheless, some companies now consider that overcoming variability and reliability challenges in RS devices is too big, and have stopped/decreased their work on RS-based electronic memories.[48,49]

RS devices exhibiting multiple resistive states may increase the storage capacity from 2^n to $X^{(n\times m)}$, where X is the number of resistive states and $n\times m$ is the number of RS devices used (i.e., the size of the crossbar array, with n rows and m columns).[50–52] However, in this case, distinguishing the resistive state in all cycles for all devices is even more challenging, as the resistance ratio from one state to the adjacent one is narrower than within only two states.[53,54] Refs. [55–57] reported multilevel RS devices using vertical metal/MO/metal nanocells, without providing statistical information on what percentage of devices showed similar resistive states without mismatch (i.e., yield). Therefore, such prototypes are not yet useful as RS-based memory technologies and, as of 2022, there is no commercial (standalone or embedded) non-volatile memory using multilevel RS devices, due to the difficulty in distinguishing all states for all devices, as well as the low yield.

MIM-like RS devices can also be employed to construct electronic neurons and synapses for artificial neural networks (ANNs) and neuromorphic computing.[58] These are novel

circuit architectures that can process and store information in parallel (similar to biological brains) so that no data transmission between the central processing unit and the memory is needed.[59] This is very attractive because it reduces the energy and time required to carry out each operation. E.g., ref. [60] designed an artificial synapse for "brain-on-a-chip" with energy consumption 1000 times smaller than that of traditional chips.[60] In these systems, RS devices can act either as electronic synapses (enabling analogical switching between multiple stable states[61]) or as electronic neurons (enabling highly non-linear (slope <1 mV decade^{-1}) switching between two states with self-recovery after short times <30 s).[62]

The technological requirements of MIM-like RS devices for ANNs and neuromorphic computing are still under debate.[16,63] The current view is that they need to exhibit multiple states (i.e., 2–32,[16] 20–100[63]), but there is no consensus on the stability required (some claim from few seconds to days,[16] while others 10 years[63]). Achieving a low switching energy per state transition (≈10 fJ) is also considered essential, but challenging.[16,63] Other performance requirements are less strict compared to those for non-volatile memories, i.e., operating speeds ≈1 ms,[63] endurance ≈3×10^9[63] potentiation and depression cycles (i.e., switching from the least to most conductive states stopping in all intermediate ones, and back to the least conductive one), R_{HRS}/R_{LRS} ≈4.[16,63] There is also no clear vision yet on device-to-device variability of the number of stable resistive states and their values.

Hundreds of papers have claimed that novel materials (different from phase-change, metal oxides and magnetic) and structures (different from vertical MIM cells) exhibit RS behaviors that make them "promising" for electronic memories,[64–66] ANN,[67,68] and/or neuromorphic computing.[69,70] The most commonly studied are layered materials (LMs)[70–77] MXenes,[78,79] perovskites,[80,81] nanowires,[82] nanotubes,[83] quantum dots,[84,85] and polymers.[86–89] However, many[90–95] only presented proof-of-concept investigations in one or few devices, without information on yield and device-to-device variability, key for viable RS technologies. Refs. [65,90,96–103] used fabrication processes not scalable to the wafer-level (i.e., micromechanical cleavage [MC] of bulk crystals[104,105]), and/or used device structures that are too large (i.e., >10^3 μm^2[71]), therefore not meeting the integration density requirements (256 nm^2 per device).[5,6]

Several reviews summarized the literature on LMs-based RS devices.[70–77,106–110] However, these did not provide a critical vision on the usefulness of each development from an industrial point of view, i.e., they mostly discussed ML-LMs and single devices with large (>10^4 μm^2) size, instead of crossbar arrays of small (<10 μm^2) MIM-like RS devices produced with industry-compatible methods. Therefore, here we focus on crossbar arrays of LMs-based RS devices produced using methods scalable to the wafer-level, with an emphasis on technology-relevant features, such as scalability of the manufacturing process, device size (i.e., integration density), variability, and yield. First, we analyze and summarize state-of-the-art fabrication methods. Second, we discuss the advantages of employing LMs in terms of performance at device level. As reference, we compare with RS devices made of phase-change, metal oxides, and magnetic materials, i.e., those with the highest performance so far.[25,111–116] Third, we discuss yield and variability of devices. Fourth, we analyze multi-device configurations (like one-transistor one-resistor) and circuital metrics (like sneak path currents). Fifth, we describe the most advanced circuit-level implementations using crossbar arrays of RS devices. Finally, we discuss the main challenges and prospects.

2. Device Fabrication

As of 2022, the only device structure being considered by companies working on RS technologies is the crossbar array of vertical MIM nanocells,[5] due to its high integration density ($4F^2$ footprint, where F is the minimum feature,[117] which can be <10 nm[115]). As high-density crossbar arrays of MIM nanocells cover large areas (>10^4 μm^2[76]), MC may not produce large enough LMs.

LMs are solids with highly anisotropic bonding, constituted by sheets internally strongly bonded, but only weakly bonded to adjacent layers. Graphene is a single layer of graphite, with many unique properties, from electronic to chemical and from optical to mechanical.[118] It has opened a floodgate for many other LMs to be studied.[119] These are often referred to as 2D materials. However, we prefer to use the term LMs, since only a few of them are truly one atom thick once exfoliated, e.g., graphene and hexagonal boron nitride (hBN), while most of the others consist of multiple atomic layers,e.g., MoS_2 or WSe_2. For a given material, the range of properties and applications can be tuned by varying the number of layers and their relative orientation. LM hetero-structures with tailored properties can be created by stacking different layers.[120] The number of bulk materials that can be exfoliated runs in the thousands,[119] but only very few have been studied to date.[118]

Scalable methods to produce LMs, such as liquid phase exfoliation (LPE)[121–123] and chemical vapor deposition (CVD),[124,125] or metal–organic CVD (MOCVD)[126–129] are necessary. However, LMs exfoliated by LPE may contain flakes with random orientations and disordered junctions (**Figure 3**a–c),[130] and those deposited by (MO)CVD may contain local defects that propagate from one layer to another[131] (Figure 3f). The most common techniques employed to detect thickness fluctuations, defective bonding, polymer residuals, wrinkles, suspended LMs, and twin boundaries are conductive atomic force microscopy (AFM)[68] and cross-sectional transmission electron microscopy (TEM).[36] Ref. [132] also used time-of-flight secondary-ion mass spectrometry and total-reflection X-ray fluorescence measurements to evaluate the Cu density remaining in LMs after transfer. Any performance observed using MC-LMs needs to be confirmed in LMs obtained via scalable methods (i.e., LPE, (MO)CVD) before claiming it to be "promising" for wafer-scale technologies.

Ref. [133] fabricated crossbar arrays of Al/≈7.5 nm MoS_2–MoO_x/Al by spin coating LPE-MoS_2, and achieved fully coverage of 4″ wafers (Figure 3a), but the lateral size of the devices was 3600 μm^2, too large for extracting conclusions applicable to high-density technologies (i.e., with devices <0.01 μm^2). Refs. [130,134,135] used LPE to exfoliate MoS_2 and achieved smaller sizes (≈2500 μm^2), for smaller crossbar arrays (i.e., just 5×5[134]). When using LPE, the resulting films are usually thicker (≈10 nm[136]) and show larger thickness fluctuations (surface roughness ≈ 3 nm[137]) than CVD-LMs (which

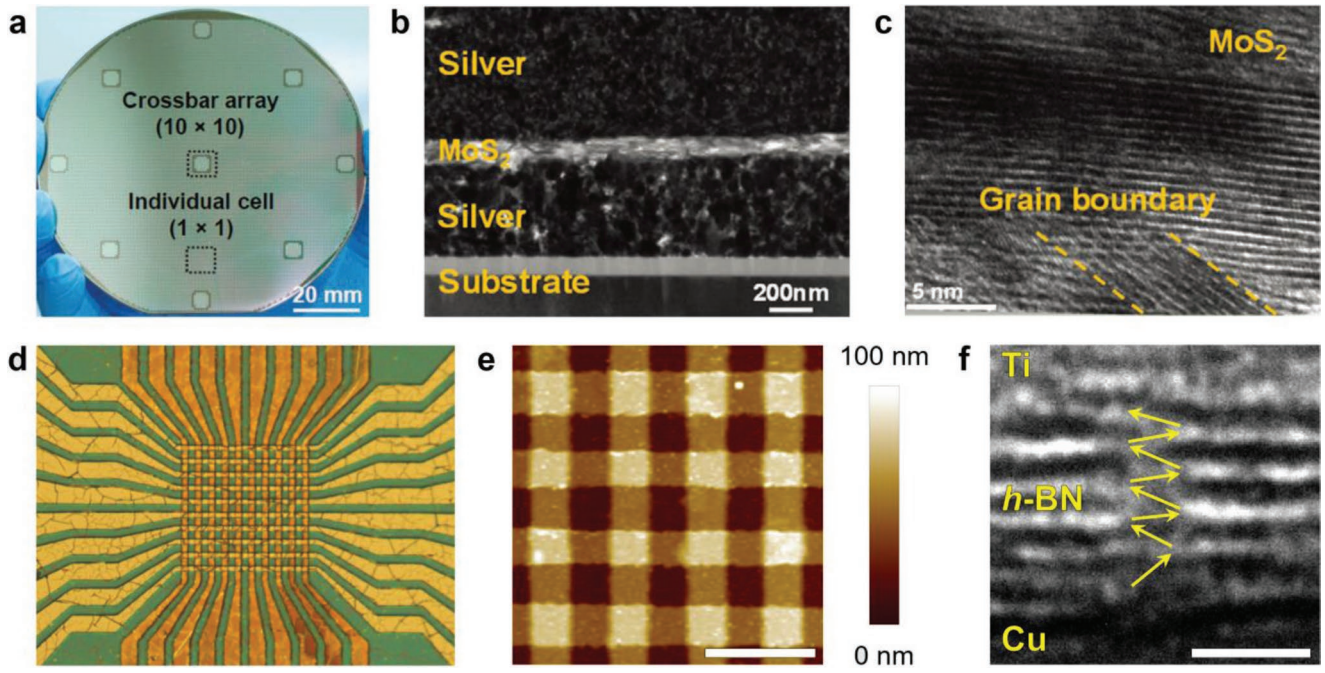

Figure 3. Wafer scale integration of LMs in memristive crossbar arrays. a) 2″ wafer containing multiple crossbar arrays of Al/≈7.5 nm MoS_2–MoO_x/Al RS devices in which the MoS_2 layer was prepared via LPE. Reproduced with permission.[133] Copyright 2016, Wiley-VCH. b,c) Cross-sectional TEM images of an Ag/≈154 nm LPE-MoS_2/Ag RS device. The defective junctions between flakes can be observed. b,c) Adapted with permission.[130] Copyright 2019, Wiley-VCH. d) Optical microscopy image of a 10 × 10 crossbar array of 5 µm × 5 µm Au/15–18L-hBN/Au RS devices with CVD hBN. e) Topographic map of 16 Au/15–18L-hBN/Au RS devices with lateral sizes 750 nm × 750 nm embedded in a crossbar array, showing no wrinkles. d,e) Reproduced with permission.[68] Copyright 2020, The Authors, published by Springer Nature. f) Cross sectional TEM image of Ti/15–18L-hBN/Cu RS device, showing a percolating defect that propagates vertically. Reproduced with permission.[131] Copyright 2018, The Authors, published by Springer Nature.

can be <1 nm[138] and peak-to-valley distances <150 pm[138]). The presence of flakes with random orientations and defective junctions in insulating LPE-LM films (Figures 3b,c), increases the inhomogeneity of the MIM cells, resulting in a higher variability of state resistances and switching voltages[133] than CVD devices.[68]

The (MO)CVD synthesis of LMs usually requires high temperatures >850 °C.[67,118,139–141] Graphene growth at low temperatures compatible with CMOS technologies has been reported,[142,143] but those methods either resulted in a lower quality or are still not widely employed.[142,143] Thus, at present, LMs are not grown directly on wafers containing patterned circuits, but on an optimized substrate (e.g., single crystal or polycrystalline metals[144]), and then transferred[145–147] onto the patterned wafers. Some LMs (e.g., graphene, hBN) often require Cu substrates for CVD,[147,148] which could contaminate patterned wafers even if the growth temperature would fit front-end-of-line (FEOL) and BEOL thermal budgets (<450 °C).[149] MOCVD was used for hBN on (Cu-free) SiO_2/Si wafers.[150]

There are different transfer processes: wet,[151] dry,[152,153] and semi dry.[154] All consist of four main steps:[118] 1) deposit a scaffold (normally a polymer) on the LM, 2) detach the scaffold/LM from the substrate (either by etching the substrate or by delamination), 3) attach the scaffold/LM to the target substrate, and 4) remove the scaffold and clean the resulting LM/substrate. These processes introduce contamination into the LM, either from the substrate (10^{13} to 10^{15} Cu atoms cm^{-2}[132]), or scaffold (poly(methyl methacrylate)[123]), and can produce cracks (especially in monolayer (1L)-LMs), wrinkles, and folds.[155] Transfer-free LMs and electronics were also reported,[156–158] however, the use of low (300 °C[143]) temperature results in LMs with lattice distortions, missing bonds, interstitials, and amorphous regions, resulting in worse materials properties.[156–158] Wafer-scale ultraclean and wrinkle-free transfer processes were developed.[159–161] The effect of wrinkles and contaminants on MIM-like RS devices is not as severe as in other devices, such as field-effect transistors (FETs), since, unlike FETs (in which the current flows homogeneously in-plane), the out-of-plane currents driven by RS devices flow only across the most conductive spots.[162] Therefore, wrinkles and polymer residues locations have a higher out-of-plane electrical resistance compared to clean ones,[163] meaning that CNFs do not form there,[164] see **Figure 4**. On the contrary, LM atomic defects (when used as dielectric) produce dangling bonds across which the trapping of electrons is easier, and where the energy needed to generate the filament is lower.[28] Therefore, these locations are prone to host the CNFs when an electric field is applied.

If the area covered by the wrinkles and contaminants is low (i.e., <10%), device-to-device variability is negligible.[163] Ref. [68] reported that, when the width of the wires in the crossbar array and the distance between them is reduced from 3 µm to 750 nm (for both), the amount of wrinkles in the LM is reduced (see Figure 3d,e) probably due to an increase of surface roughness, since this would enable strain to be released by adapting to the rougher contour of the sample surface.[165,166] The transfer process can also result in uncontrollable cracks due to the introduction of biaxial strain,[167] which can short-circuit a group of devices,[5] decreasing yield.[6] The thicker the LM the lower the

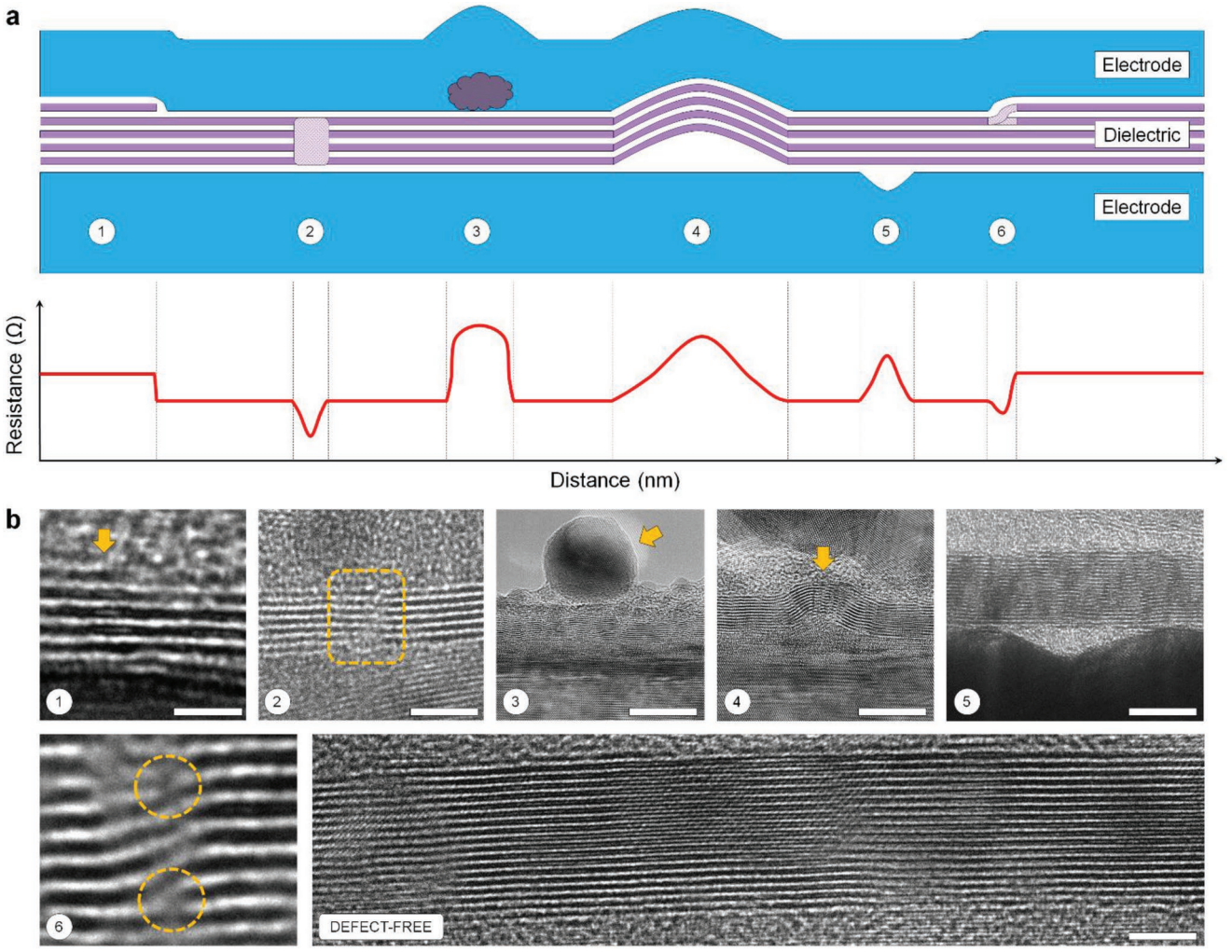

Figure 4. Local vertical resistance of different defects in LM-based RS cells. a) Schematic RS device with a vertical electrode/dielectric/electrode structure, in which different local defects and their resistance are highlighted: 1) thickness fluctuations, 2) defective bonding, 3) polymer residuals, 4) wrinkles, 5) suspended LMs, 6) twin boundaries. Dielectric breakdown (therefore, RS) takes place at the least resistive (weakest) location, i.e., the thinnest and most defective site. Breakdown and/or RS does not happen below wrinkles and/or contaminants. b) Cross-sectional TEM of multilayer (ML)-hBN illustrating the defects numbered in (a), plus one image showing defect-free hBN. The TEM images were collected for different samples (compiling all types of defects observed), with thickness 5–20L. a,b) Reproduced with permission.[163] Copyright 2021, Wiley-VCH.

amount of cracks produced during transfer.[163] Refs. [92,168] fabricated Au/hBN/Au devices using transferred 1L-hBN and observed large on/off ratio (up to 10^7) and fast switching (<15 ns), but the maximum yield was 50%.[168] Ref. [68] fabricated Au/hBN/Au using transferred ≈18L-hBN, and achieved a yield ≈98% (102 out of 104 devices worked correctly).

RS devices made of LMs synthesized by CVD[68] or LPE[169] exhibit RS. Refs. [26,32,35] investigated the switching mechanism combining cross-sectional TEM images with nanochemical measurements (e.g., electron energy loss and energy-dispersive X-ray spectroscopies) or atomistic calculations (e.g., first principles and molecular dynamics).[131] In multilayer (ML)-hBN, RS is enabled by the penetration of metallic ions from the electrodes, favored by the migration of B vacancies.[131] This is very similar to TMDs,[37,170] although in these the penetration of metal may not be necessary, as the generation of chalcogen vacancies leaves behind a metallic CNF,[65] not happening in hBN after the generation of B vacancies.[131] When the material is 1L, RS can be produced by the migration of a single atom (i.e., B in hBN[168] and S in MoS_2[170]), without metal penetration. In graphene oxide (GO), RS can be enabled both by the migration of oxygen (when using stable electrodes[27,171]) or by the penetration of metal (when using active electrodes[27,74,157]). Refs. [171,172] illustrated possible RS mechanisms using cartoons and schematics, but not backed by direct measurements or computation.

3. Advantages of LMs over TMO for RS Devices

A few studies on RS devices made of LMs[68,131,173,174] reported performances not yet achieved with phase-change, metal oxide, or magnetic materials (see **Figures 5–10**). Ref. [107] summarized

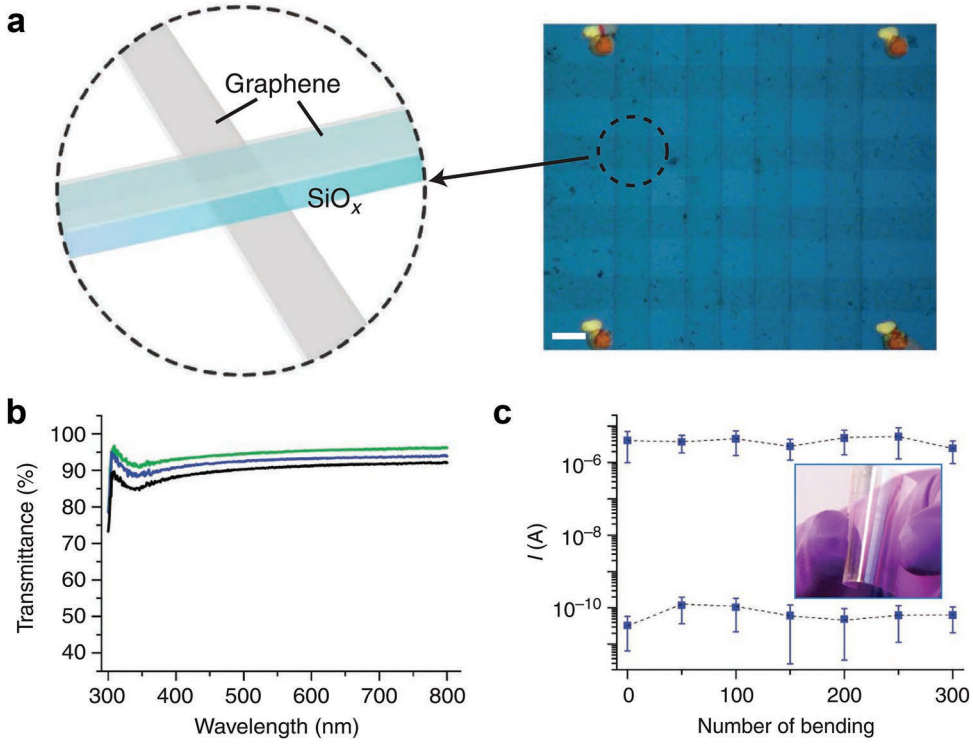

Figure 5. Transparency of LMs-based memristive crossbar array. a) Schematic and optical image of a transparent and flexible crossbar array of 2LG/SiO_x/2LG RS devices, with light transmittance shown in (b). c) Current of devices in panel (a) in HRS, and LRS currents after up to 300 bending cycles (R = 0.6 cm). a–c) Reproduced with permission.[174] Copyright 2012, Springer Nature.

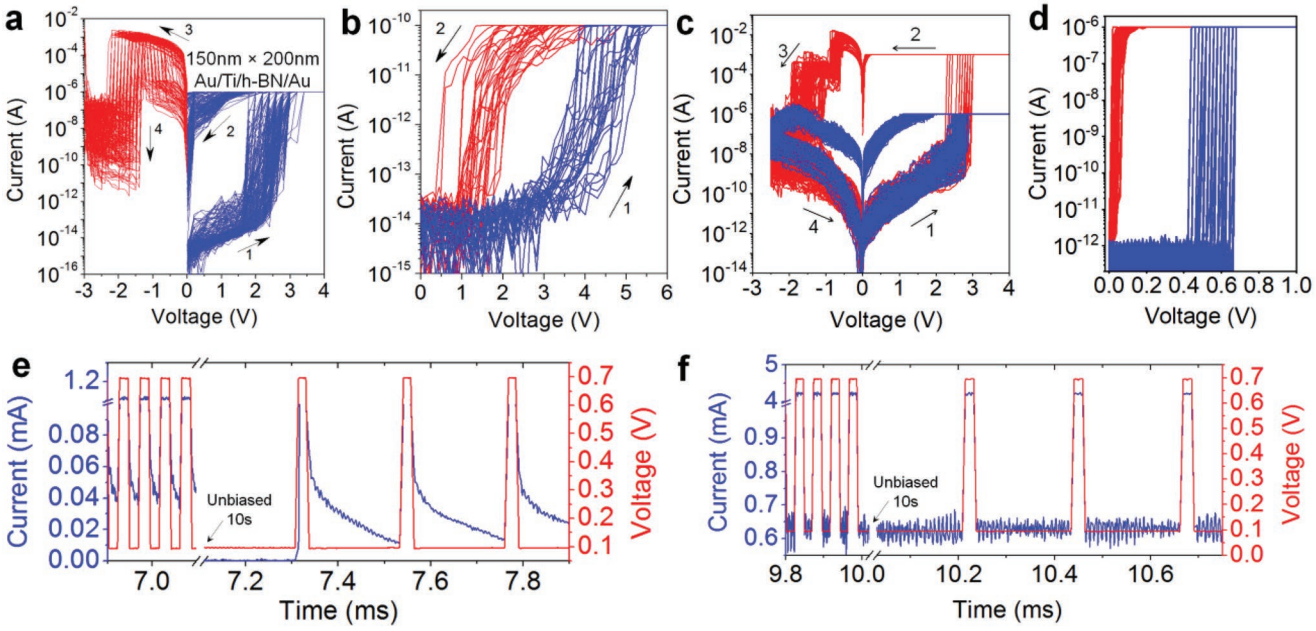

Figure 6. Typical non-volatile and volatile RS in LMs-based RS devices under RVS and PVS. a,c) Typical non-volatile bipolar and b,d) volatile RS observed in Au/hBN/Au synapses with different sizes. The current limitations are 10^{-10} A in (b), 1 µA (blue), 1 mA (red) in (c), and 10^{-6} A in (d). e,f) I–t plots applying pulsed voltage stresses to an Au/Ti/15–18L-CVD-hBN/Au RS device, showing initially volatile RS (e), followed by non-volatile RS (f) as the stress proceeds. a,b,e,f) Reproduced with permission.[131] Copyright 2018, The Authors, published by Springer Nature. c,d) Reproduced with permission.[68] Copyright 2020, The Authors, published by Springer Nature.

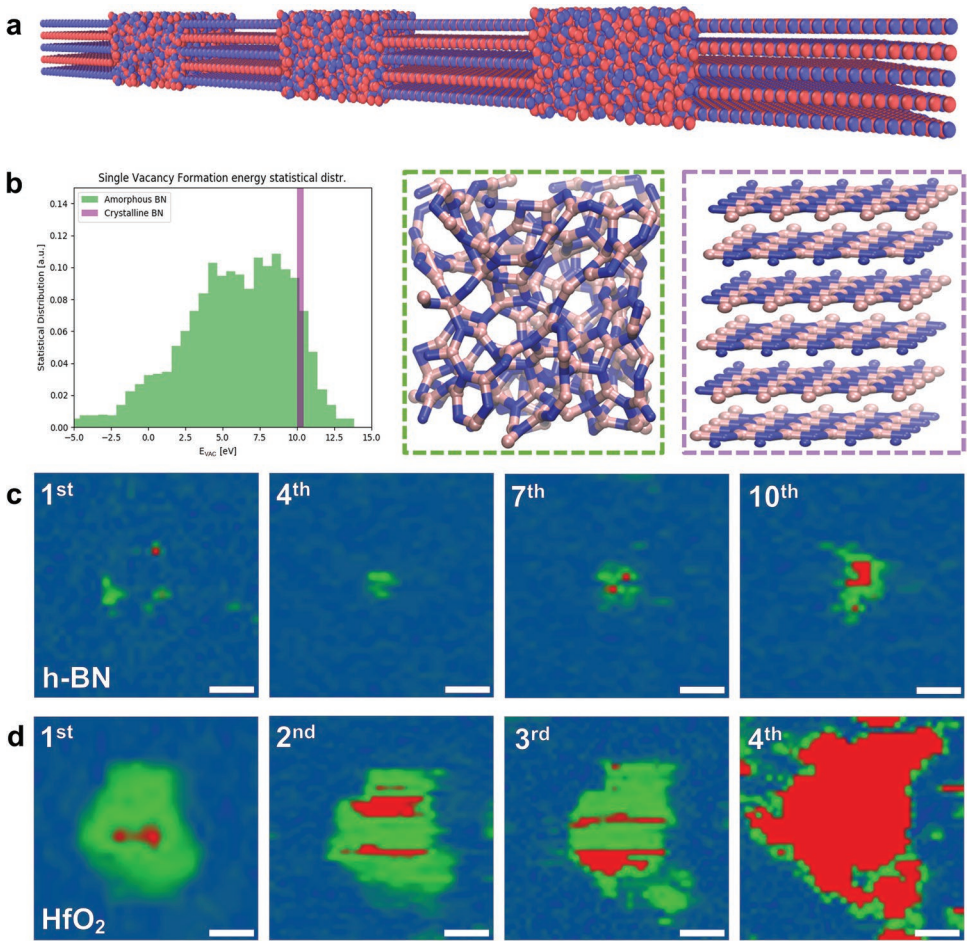

Figure 7. Working principle of ML-LMs-based RS devices produced by CVD. a) Schematic of a CVD-grown ML-hBN, with layered regions and few-atoms-wide amorphous defects (in agreement with Figure 4b). b) Single vacancy formation energy in the amorphous and crystalline regions of (a), calculated by molecular dynamics. c,d) Current maps collected with a conductive atomic force microscope (working in vacuum) on a single defect for CVD-grown ML-hBN and HfO_2, in both cases by applying the minimum voltage to observe current above the noise level. Big lateral propagation of the HfO_2 defect is observed, while very little lateral propagation is seen in hBN, indicating a confinement effect. a–d) Reproduced with permission.[28] Copyright 2021, Wiley-VCH.

proof-of-concept RS in different materials, including MoS_2, TaS_2, $MoTe_2$, WS_2, hBN, and WSe_2, without advantages with respect to phase-change, metal oxide and magnetic materials in terms of switching time, switching energy, endurance, state retention time, and/or integration capability.[5,175–178] Refs. [179–181] are not only inferior to RS devices made of phase-change, metal oxide, or magnetic materials in terms of single device performance, but also have more complex fabrication process,[179,180] higher device-to-device variability,[68,181] and lower yield.[37,158]

The properties of LMs-based RS devices that are superior to phase-change, metal oxide, or magnetic materials RS devices are: 1) Controllable transparency. This can be adjusted by changing the number of layers[174] (see Figure 5), and may be useful to integrate memristors in transparent products (cameras[187]) and to activate the devices via light.[188] 2) Controllable RS regime. The operation of hBN-based RS devices is possible in both threshold (i.e., volatile[189]) and bipolar (i.e., non-volatile[1]) regimes (see Figure 6). The control of the regime can be achieved by tuning the current limitation of the semiconductor parameter analyzer,[36] by changing the gate voltage of a series transistor,[190,191] or the value of the series resistor.[190] This cannot be done with RS devices made of phase-change, metal oxide, or magnetic materials (they may show some degree of coexistence, but the characteristics are erratic and disappear after some cycles),[61] while with hBN these two regimes are programmable and very stable.[68,131] Controllable RS adds versatility to the devices, as they could be employed as both electronic synapses and electronic neurons in deep neural networks, or as both memristors and selectors in electronic memories. 3) Controllable potentiation. Refs. [61,182–184] reported erratic potentiation in RS devices made of traditional (HfO_2, SiO_2, TiO_2, SiN_x) materials, whereby the upwards trend showed sudden decrease of conductance at some specific pulses (see Figure 8a–d). This is not observed for hBN-based RS devices (see Figure 8e,f). Controllable potentiation can be used to precisely recognize the states during the analogue training, which should be helpful to program the memristors at the exact weights required in deep neural networks based on the back-propagation algorithm. 4) Controllable relaxation. Ref. [61] reported erratic relaxation in RS devices made of traditional materials, whereby the

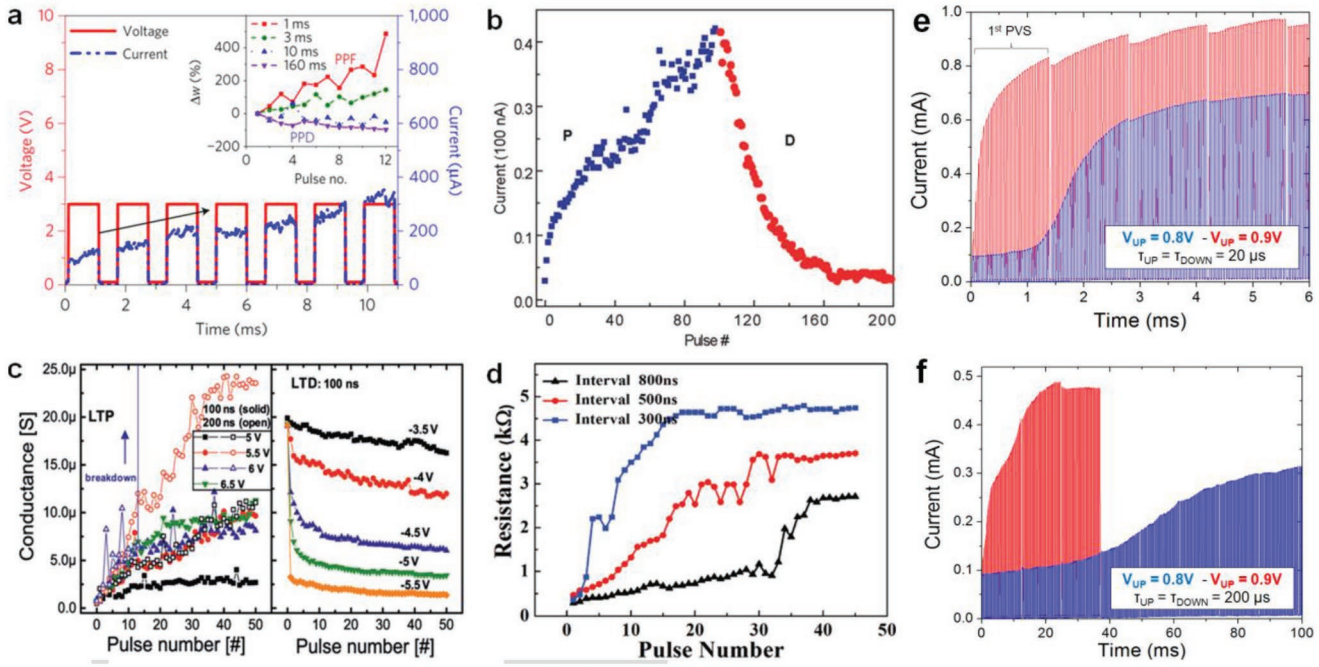

Figure 8. Potentiation behaviors in metal oxides and LMs-based synapses. a) Experimental data demonstrating short-term synaptic paired-pulse facilitation (PPF) and paired-pulse depression (PPD) with diffusive SiO_xN_y:Ag RS device. The inset shows the weight versus pulse number data for different intervals. b) Potentiation and depression in Cr-Pt nanowire/Ag:Si/a-Si/Si/W nanowire RS device. c) Conductance modulation of Ni/SiN_x/AlO_y/TiN RS device in an identical pulse response. d) Conductance modulation of Ag/TiO_2:Ag/Pt RS device with different pulse train intervals. e,f) Progressive synapse potentiation in metal/hBN/metal synapse under different up voltages. a) Reproduced with permission.[61] Copyright 2016, Springer Nature. b) Reproduced with permission.[182] Copyright 2010, American Chemical Society. c) Reproduced with permission.[183] Copyright 2017, American Chemical Society. d) Reproduced with permission.[184] Copyright 2017, Wiley-VCH. e,f) Reproduced with permission.[131] Copyright 2018, The Authors, published by Springer Nature.

downwards trend showed sudden increase of conductance over time, and the relaxation time had large cycle-to-cycle variability (see Figure 9a). This is not observed for hBN-based RS devices (see Figure 9b). Controllable relaxation can be applied to ensure the correct return to the initial state of electronic neurons for deep neural networks after firing, which helps reduce the probability to get stuck in a conductance state higher than the initial, hence improving reliability. 5) Ultralow energy consumption per state transition, down to 8.8 zJ (see Figure 10c). This property can be useful to integrate the devices in wearable and self-powered products, especially for the Internet of Things.

Refs. [169,173,174] fabricated crossbar arrays of MIM cells with high (up to 97.4%) transparency, which could be interesting for sensors integrated in solar cells, lenses, cameras, and contact lenses. Ref. [169] used ≈16 nm thick LPE reduced GO (RGO) as dielectric in crossbar arrays of RS devices with Pt electrodes. However, the Pt electrodes (i.e., the wires) reduced the transparency of the array. Ref. [173] fabricated MIM-like RS devices using a mixture of polyimide (PI) and 6-phenyl-C61 butyric acid methyl ester (PI:PCBM) as insulator, highly transparent (92%) multilayer graphene (MLG) prepared by wet transfer as top electrode, and Al as bottom one. Refs. [173,174] did not disclose the transparency of the entire device (only that of MLG), which is unfortunate, since the 50-nm-thick bottom Al electrode reduces the overall transmittance. Ref. [174] achieved ≈90% transmittance using bilayer graphene (2LG), fabricated by layer-by-layer transfer, coupled with SiO_x deposited by electron beam evaporation, see Figure 5. Ref. [192] reached ≈97.4% transmittance by using doped monolayer graphene (1LG, CVD grown, <1 kΩ sq^{-1}).[192] Refs. [169,173] reported large-area (>10^4 μm^2) dot-like RS devices with the assistance of a shadow mask, and applied mechanical stresses using bending radiuses (R) ranging from 4.2 mm to 1.2 cm.[169,173] Accurate control of light transmittance across LMs-based RS devices cannot be done when employing phase-change, metal oxide, or magnetic materials. This offers one important tool for the design of RS devices for optoelectronic applications.

LMs were also used to fabricate RS devices with both threshold (i.e., volatile) and bipolar (i.e., non-volatile) RS, depending on the electrodes (Ag for threshold[68,193] and Au for bipolar[68,163]), and sometimes simultaneously (using Ti),[36] see Figure 6a–d. This is useful for electronic synapses and neurons,[133] and difficult to achieve in RS devices made of phase-change, metal oxides, or magnetic materials. Ref. [36] reported both threshold and bipolar RS in 50 μm × 50 μm Au/Ti/≈18L-CVD-hBN/Cu dot-like devices fabricated with the assistance of a shadow mask. Ref. [68] also achieved this for Au/Ti/≈18L-CVD-hBN/Au cross-point devices with sizes ≈5 μm × 5 μm (fabricated via photolithography) and 150 nm × 150 nm (fabricated via electron beam lithography [EBL]). Ref. [131] used ≈5–7L hBN to fabricate memristive electronic synapses. Threshold RS was used to emulate short-term plasticity (STP, i.e., volatile conductance changes that self-recover in few ms,[194] Figure 6e), and bipolar RS was used to emulate long-term plasticity (LTP, i.e., non-volatile conductance changes stable for minutes/hours,[195]

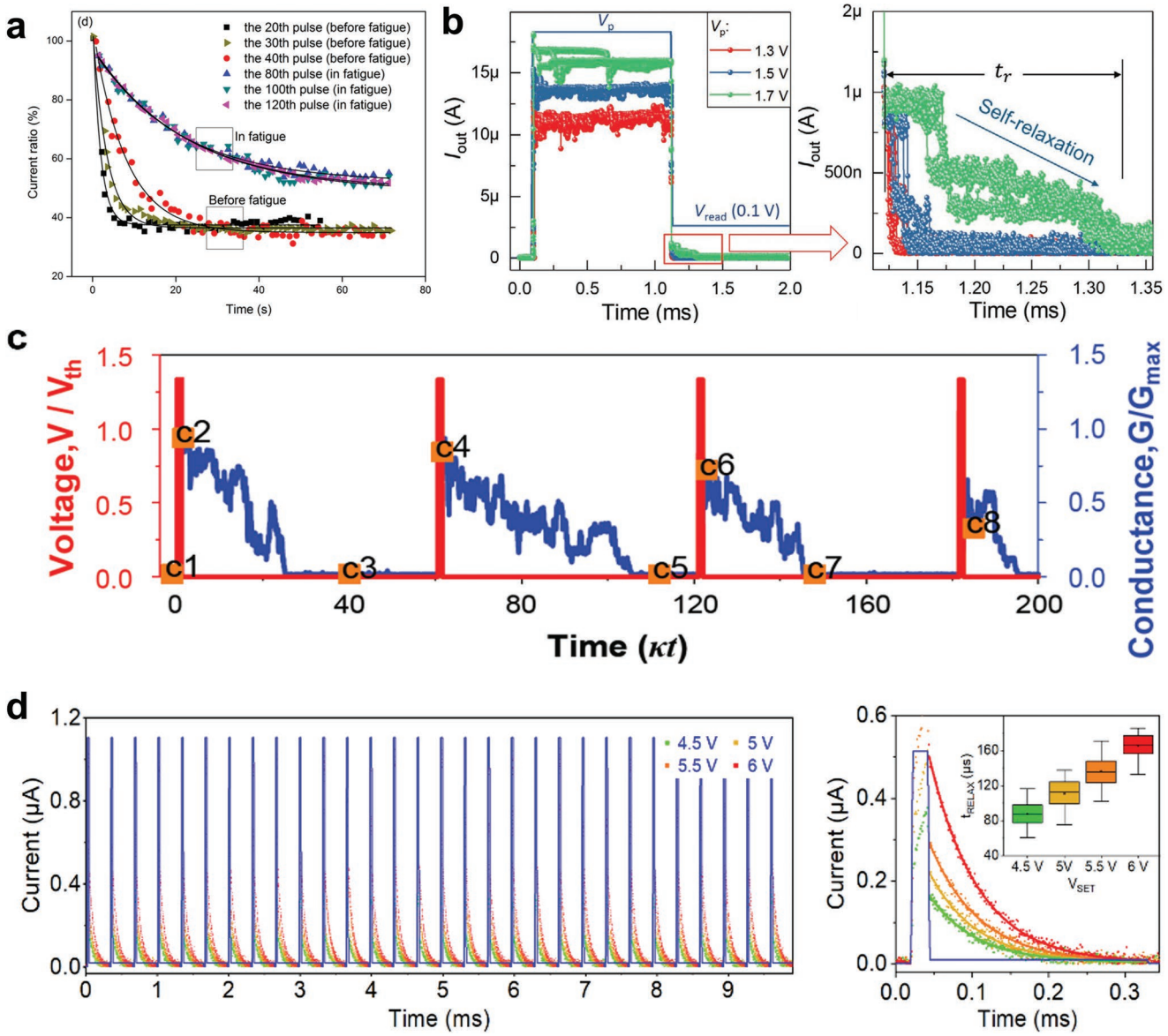

Figure 9. Relaxation behaviors in metal oxides and LMs-based RS devices. a–c) Voltage and conductance versus time showing erratic relaxation of Au/Ti/IGZO/HfO_2/Al, Ag/HfO_2/Pt, Ag/SiO_x:Ag/Ag RS devices, respectively. d) Current versus time plots showing relaxation of Ag/h-BN/Ag RS device when applying PVS of different amplitude. c) Dispersion of t_{RELAX} depending on the pulse amplitude (V_{SET}). a) Reproduced under the terms of the CC-BY Creative Commons Attribution 4.0 International license (https://creativecommons.org/licenses/by/4.0).[185] Copyright 2017, The Authors, published by Springer Nature. b) Reproduced under the terms of the CC-BY Creative Commons Attribution 4.0 International license (https://creativecommons.org/licenses/by/4.0).[186] Copyright 2022, Wiley-VCH. c) Reproduced with permission.[61] Copyright 2016, Springer Nature. d) Reproduced with permission.[68] Copyright 2020, The Authors, published by Springer Nature.

Figure 6f). The coexistence of both regimes in a single device simplifies the design of ANNs and neuromorphic systems, usually requiring two[61] or more[196,197] RS devices and complex algorithms[198] to emulate STP and LTP. The threshold RS in hBN-devices was so reproducible that relaxation followed an exponential curve with low (≈8.52%) cycle-to-cycle variability of the relation time (t_{RELAX}), Figure 6e,[68,131] outstanding compared to RS based on SiO_x[61] and metal oxides.[199,200] Previous experiments demonstrated that metal oxides, such as HfO_2 and CuO, do not offer the possibility of switching from one RS regime to another, with coexistence of both RS regimes erratic and lasting for few cycles.[36,131]

Apart from the inherent and versatile operation of LMs-based RS devices in both volatile and non-volatile modes, the conductance can be more accurately controlled than in metal/MO/metal devices, both when it is increased and decreased (i.e., the device is potentiated and depressed, or relaxed). Refs. [61,182–184] showed the typical potentiation behavior for metal/MO/metal and metal/SiO_x/metal RS devices when a sequence of pulses is applied (Figure 8a–d), and observed that the currents/conductance increase (or resistance decrease) erratically, i.e., in some pulses the device exhibits a lower conductance than in one/few of its

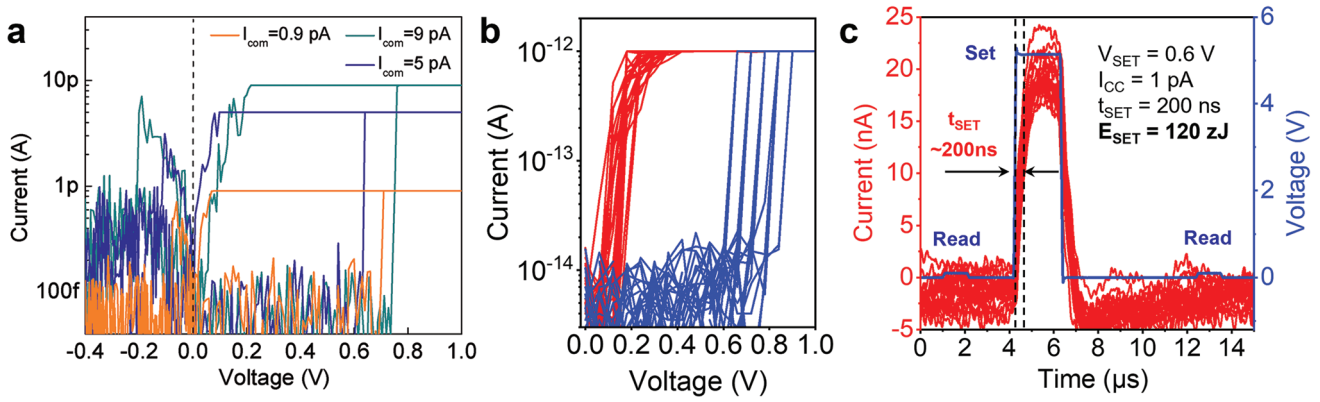

Figure 10. Threshold RS in LMs-based RS devices. a) *I–V* plot for one Ag/0.9 nm BNO_x/5LG threshold RS device (fabricated via MC) showing bipolar RS at $I_{CC} \approx$ 0.9, 5 and 9 pA. Stable switching over 100 cycles and ≈14% variability of the set voltage is demonstrated for operating currents of 5 pA. Reproduced with permission.[90] Copyright 2017, Wiley-VCH. b) *I–V* plots for an Ag/15–18L-CVD-hBN/Ag RS device showing reproducible threshold RS for I_{CC} ≈1 pA. c) *I–V* curves applying pulsed voltage stresses to an Ag/15–18L-CVD-hBN/Ag RS device, showing a switching time ≈200 ns, with energy consumption per state transition ≈8.8 zJ.[68] b,c) Reproduced with permission.[68] Copyright 2020, The Authors, published by Springer Nature.

predecessors. On the contrary, ref. [131] demonstrated that in metal/hBN/metal RS devices the current undergoes a very smooth increase with number of pulsed voltages, with all pulses showing more current than all their predecessors (see Figure 8e,f). The superior controllability of potentiation and depression processes in CVD ML-hBN (compared to metal oxides and phase-change materials) may be related to the lower number of atoms involved in the switching.[28] The RS in ML-hBN is produced by CVD and is driven by few-atoms-wide amorphous defects embedded in the crystalline lattice (see Figure 2b, image 2);[68] these local defects are confined within a crystalline hBN in each layer, which is not involved in the switching due to the higher energy for vacancy formation (as demonstrated by first principles calculations[28]). These stable atoms in the crystalline lattice result in a confinement effect that prevents lateral propagation of the CNF that produces the switching (as demonstrated via conductive AFM,[28] see Figure 7).

A similar observation can be made for the relaxation of RS devices. When MIM-like RS devices are operating in non-volatile (i.e., threshold) regime and the voltage is switched off, the current across the devices reduces progressively until zero, due to the partial/complete disruption of the CNF across the insulator. Refs. [61,182–184] showed that when the insulator is a metal oxide or SiO_x the current reduces in an erratic manner, with current upward/downward trends and with different relaxation times (i.e., time since the voltage is reduced until the current is zero), Figures 8a–c. However, ref. [68] showed that, when using metal/LMs/metal RS devices, the relaxation of the currents takes place in a much smoother manner, and the relaxation time follows an exponential law and increases with the voltage applied during the pulse (see Figures 8b,c). This can be beneficial when fabricating leaky integrate-and-fire electronic neurons for neuromorphic applications.[4–6]

Ref. [68] used 15–18L-CVD-hBN to fabricate threshold RS devices with ultralow energy consumption. Ref. [90] reported threshold RS between two ultralow current levels with 5LG/0.9 nm BNO_x/Ag (fabricated via MC), with HRS = 10 fA and LRS = 5 pA, Figure 10a. Ref. [68] demonstrated switching between 10 fA (HRS) and 110 fA (LRS), with >2000 cycles in six Ag/15–18L-CVD-hBN/Ag. The estimated energy consumption per state transition was ≈8.8 zJ, Figures 10b,c, while the previous record in metal/MO/metal devices (i.e., TiN/Hf/HfO_x/TiN and Al/Ti/Al_2O_3/s-CNTs, where s-CNTs = semiconducting carbon nanotubes) was 0.1 pJ per transition.[115,201] State transition energies in the zJ range were not reported to date in RS devices made of phase-change, metal oxide, or magnetic materials.

Ref. [65] fabricated MIM-like RS devices using MLG electrodes and ≈40 nm MoS_2 as dielectric layer (all obtained by MC), and reported stable bipolar RS operation during >100 cycles at ≈300 °C. This was included in the IRDS[6] as a potential advantage of LMs-based RS devices. However, this finding was achieved using MC[65] and not yet reproduced. The 10^6 cycles in ref. [65] were based on one data point per decade. Ref. [202] suggested that one data point per cycle is more reliable.[202] Hence, the superior thermal stability of LMs-based RS devices needs to be further demonstrated statistically in devices fabricated using scalable methods (LPE, CVD, MOCVD).

4. Yield and Variability of LMs-Based RS Devices

RS devices made of phase change and metal oxide materials show variability (within a single device) related to the stochasticity of the switching mechanism (CNF formation across the metal oxide and melting in phase-change).[1] The variability from one device to another is related to imperfections in the fabrication process (which produce inhomogeneity), resulting in devices with different microstructures (e.g., thickness fluctuations and different densities of defects).[5]

Refs. [203–215] analyzed the variability of metal/MO/metal RS devices (see **Tables 2** and **3**), most of them coming from companies. As of 2022, the best performances for a single device were reported by refs. [205,210], with C_V of V_{SET} and V_{RESET} ≈1% and 1.62%, respectively. However, only one device was presented,[205,210] and device-to-device variability was not discussed.[210] Ref. [211] reported ITO/Eu_2O_3/ITO/PET with device-to-device

Table 2. Cycle to cycle variability of RS devices. C_V for V_{SET} and V_{RESET} of RS devices (made of any material) from one cycle to another. The size of the cells and the value of the current in LRS are also indicated, to evaluate how competitive the devices are in terms of integration density and energy consumption. The table shows that many studies on metal/MO/metal RS devices have quantified the cycle-to-cycle variability of V_{SET} and V_{RESET}, but for metal/LMs/metal RS devices such analysis is often not reported.

Ref.	Device structure	Device size	I_{LRS} [at 0.1 V]	C_V [V_{SET}]	C_V [V_{RESET}]
[203]	TiN/Hf:SiO_2/Pt	$1 \times 1\ \mu m^2$	≈5 µA	5.05%	4.78%
[204]	W/HfO_x/TiN	$400 \times 400\ nm^2$	0.1 mA	—	3.15%
	W/Hf/HfO_x/TiN		0.1–0.5 mA	—	2.61%
[205]	Ag/Pd/SiGe/pSi	$5 \times 5\ \mu m^2$	≈10 pA	1%	—
[206]	Al/Cu/GeO_x/W	$1.2 \times 1.2\ \mu m^2$	≈0.1 nA	14.3%	39.4%
[207]	Ag/CZTSe/Mo	Ø 500 µm	≈0.3 mA	2.5%	—
[208]	Pt/Cu^{2+}DNA/FTO	Ø 100 µm	≈0.1 µA	22.5%	24.2%
[209]	Ni/Ti/Al_2O_3/SiO_2/p^+ Si	—	≈1 µA	29%	20%
	Ni/Ti/Al_2O_3/p^+ Si		≈0.2 mA	19%	38%
[210]	Pt/VOx/Pt	—	10 mA	< 5%	≈1%
[211]	ITO/Eu_2O_3/ITO/PET	$50 \times 50\ \mu m^2$	≈10 µA	1.44%	1.68%
		$200 \times 200\ \mu m^2$	≈0.1 mA	3.18%	3.91%
[212]	Pt/Ti/N-doped HfO_2/Pt	$100 \times 100\ \mu m^2$	≈2 µA	7.0%	6.0%
[213]	TiN/SiO_2/FeO_x/FePt	Ø 100 µm	≈10 µA	8.38%	10.03%
[214]	TiN/Al:HfO_2/Pt	$100 \times 100\ \mu m^2$	≈5 µA	19.2%	—
[215]	PET/ITO/HZO/Ag	$100 \times 100\ \mu m^2$	≈0.3 µA	25%	43%
[217]	Pt/ZnO/Pt	Ø 50 µm	≈10 µA	5.0%	9.0%
[68]	Au/15–18L-CVD hBN/Au	$3 \times 3\ \mu m^2$	0.2 pA–1 nA	2.02%	9.61%
				1.53%	6.21%

Table 3. Device-to-device variability of RS devices. C_V for V_{SET} and V_{RESET} of RS devices (made of any material) from one cycle to another and from one device to another. Variability increases with number of cycles and devices. "—" means "not mentioned." Size of cells and current in LRS are also indicated, to evaluate how competitive the devices are in terms of integration density and energy consumption. Many studies on metal/MO/metal RS devices quantified the cycle-to-cycle variability of V_{SET} and V_{RESET}, but for metal/LMs/metal RS devices such analysis is often ignored.

Ref.	Device structure	Device size	# cycles/# devices	I_{LRS} [at 0.1 V]	C_V [V_{SET}]	C_V [V_{RESET}]
[211]	ITO/Eu_2O_3/ITO/PET	$50 \times 50\ \mu m^2$	3000 cycles/—	≈10 µA	1.44%	1.68%
		$200 \times 200\ \mu m^2$		≈0.1 mA	1.44%	1.84%
[218]	Pt/TiO_x/TiO_2/W	$250 \times 250\ nm^2$	—/50 devices	≈0.2 µA	—	—
	Pt/TiO_x/TiO_2/W	$250 \times 250\ nm^2$	—/50 devices	≈0.2 mA	—	—
[219]	TiN/MnO_2/Pt	Ø 120 µm	—/50 devices	≈80 µA	—	—
[220]	TiN/TiO_x/Al_2O_3/IrO_x	—	5000 cycles/5 devices	≈100 nA	8%	—
[221]	TiW/Al/Ge/TaO_x/Pt	$9\ \mu m^2$	—	≈50 nA	19.2%	30.2%
[222]	Pt/Cu/AlO_x/Al_2O_3/Pt	Ø 30 µm	—/50 devices	≈10 nA	6.2%	9.5%
[223]	Pt/Al_2O_3/TiO_{2-x}/Ti/Pt	$200 \times 200\ nm^2$	—/400 devices	≈1 µA	≈13%	≈11.5%
[224]	Pt/TiN/TiO_{2-x}/Al_2O_3/Pt	$350 \times 350\ nm^2$	—/100 devices	≈1 µA	16%	24%
[216]	Ti/Pt/$[Ru(L)_3]^{2+}$/Au NPs/ITO	60 nm^2 (nanodot)	50 cycles/5 devices	≈1 nA	≈10%	≈5%
		$1–9\ \mu m^2$	500 cycles/50 devices	—	5.77%	7.27%
	Ti/Pt/$[Ru(L)_3]^{2+}$/Au/ITO	$1–10^4\ \mu m^2$	3210 cycles/321 devices	—	5.32%	4.59%
[225]	TiN/Al/Ti/Al_2O_3/TiO_{2-x}/TiN/Al/Ti	$250 \times 250\ nm^2$	—/4051 devices	≈0.5 µA	26%	27%
[68]	Au/15–18-layer CVD hBN/Au	$3 \times 3\ \mu m^2$	750 cycles/48 devices	0.2 Pa–1 nA	6.06%	29.07%
			317 cycles/16 devices		5.74%	12.37%

variabilities similar to cycle-to-cycle ones (C_V [V_{SET}] ≈ 1.44% and C_V [V_{RESET}] ≈ 1.68%). The area of the devices in ref. [186] was 50 μm × 50 μm, too large to meet the integration density requirements of memristive technologies (<100 nm^2).[3] For <1 μm^2, the device-to-device variability increases,[216] and the best performances as of 2022 are ≈10%[216] and 5%.[216]

Refs. [169,226] reported 25 devices (each) using ≈16 nm RGO and ≈15 nm GO, prepared by LPE, as dielectric (respectively), and claimed similar yields ≈72% and 80%. The yield of Au/Ti/15–18L-CVD-hBN/Ni RS devices with different sizes was discussed in ref. [158]. When the area decreased from 100 × 100 to 25 × 25 μm^2, the yield increased from ≈10% to 60%, probably due to a lower amount of defects under the top electrodes (e.g., less defective GBs of CVD-grown hBN between electrodes). Therefore, scaling down may be one effective approach to increase yield. This was verified in ref. [68], for devices down to 5 × 5 μm^2, leading to an increase of yield up to 98%, not reported in other LM-based crossbar arrays.[91,158,168,169,226,227] Ref. [68] also showed low device-to-device variability (C_V of V_{SET} ≈ 5.74%) and cycle-to-cycle variability (C_V of V_{SET} ≈ 1.53%), close to the best performances of MO-based RS devices.[205] Ref. [163] indicated that, when up to 25% of the surface of a 5 × 5 μm^2 Au/15–18L-CVD-hBN/Au device is covered by wrinkles and/or polymer transfer residuals, the electrical characteristics of the devices is unaltered. Ref. [163] also found that the presence of overshoot currents across the device during forming or reset events is one of the main reasons reducing the yield in Au/15–18L-CVD-hBN/Au devices with lateral size of 320 nm × 420 nm. Wafer-scale transfer is still challenging for LMs-based RS devices.

5. Access to the MIM Cells and Sneak Path Currents

So far, very few studies constructed crossbar arrays of MIM-like memristors using LMs. **Table 4** summarizes the performance of LMs-based crossbar arrays of RS devices. Ref. [163] reported a crossbar with 10 000 devices (100 × 100) with small size (0.1344 μm^2),[163] but only tested 11 devices. Refs. [65,228] claimed very high endurances (>10 million cycles) in small crossbar arrays (<36 devices/crossbar) of Ti/Pt-LPE MoS_2-Ti/Pt (size > 25 μm^2 per device) and SLG/MC $MoS_{2-x}O_x$/SLG (size > 25 μm^2 per device). However, the endurance plot only showed 22 and 73, datapoints. Thus, a demonstration in all cycles in multiple devices (as that recommended in refs. [5,202] and carried out in ref. [68]) is necessary.

In crossbar arrays of RS devices, electrical stimuli can be applied to each MIM cell selecting one row and one column.[1] However, using this approach, the surrounding MIM cells are also exposed to part of the electrical stress, which creates additional paths for current flow from one electrode to another (often called sneak paths or sneak currents).[43] In order to minimize this, one common solution is to include additional elements adjacent to each MIM-like RS device in the crossbar array, such as transistors[44,45] (leading to 1T1R configurations[44]) or selectors (leading to 1S1R configurations[45]). Ref. [44] fabricated 1T1R structures using LMs, i.e., a transistor made of WO_3 on and 4L-MC-WSe_2 connected in series to a RS device with Ag/≈400 nm-printed WSe_2/Ag.

Ref. [191] integrated CVD-1L-MoS_2 FETs with HfO_x-based RS devices to form a ternary content addressable memory, that allows high speed information search thanks to its ability to ignore data bits.[232] Due to the ultralow leakage current in 1L-MoS_2 FETs ≈1–2 fA μm^{-1},[191,233] ref. [191] claimed that the sneak paths could be cut off, while maintaining a large resistance ratio (up to 8.5 × 10^5), although the sneak path current was not characterized. In ref. [190] the set voltage of RS devices in 1T1R cells was <1 V, achieved by replacing the HfO_x-based RS devices with forming-free 10–13L-CVD-hBN-based ones, **Figures 11**a–c. Similar to ref. [191], the 1T1R cells fabricated by transferring 1L-CVD-MoS_2 and 10–13L-CVD-hBN in ref. [190] showed low sneak currents (≈1 pA μm^{-2}). Although 1L-MoS_2 FETs can reduce the sneak currents between RS devices, 1T1R require good matching between switching voltages and currents driven by transistor and RS device,[234] which increases cell size,[235] thus reducing integration density.

Ref. [46] fabricated a 12 × 12 crossbar array of 1S1R cells with vertical Au/h-BN/Gr/h-BN/Ag devices. By using EBL and three transfer steps, ref. [46] fitted the 144 devices within ≈225 μm^2 (i.e., the overlapped area of the 3 MC-flakes, see Figure 11d).

Table 4. Comparison of performance of crossbar arrays of memristors.

Ref.	Device structure	Device size [μm^2]	Crossbar size	Devices measured	V_{SET} [V]	R_{HRS}/R_{LRS}	Endurance claimed [cycles]	Endurance [data points presented]	Retention [s]
[65]	Gr/$MoS_{2-x}O_x$/Gr	1	4 × 4	—	3	10^6	2×10^7	73	10^5
[68]	Au/h-BN/Au	9	4 × 4	104	3	10^3–10^6	>1500	—	>10^3
[130]	Ag/MoS_2/Ag	10000	10 × 10	—	0.18	10^7	—	100	4×10^4
[133]	Al/MoS_2 MoO_x/Al	900	10 × 10	—	−5	10^9	100	11	10^4
[163]	Au/h-BN/Au	9	4 × 4	100	≈3	≈10^8	50	50	—
		0.1344	100 × 100	11	≈3	≈10^4	1	1	—
[174]	Gr/SiOx/Gr	400	4 × 4	—	4.2	10^6	400	99	—
[226]	Al/G-O film/Al	2500 μm^2	5 × 5	—	−2.5	>10^2	≈100	21	10^5
[229]	Al/PS/Gr/PS/ITO	1000000	6 × 6	3	1.5	10^7	5	4	10^6
[230]	Cu/pV_3D_3/MLG/Al	3600 μm^2	5 × 5	—	3	10^4	100	101	—
[231]	ITO/$MoSe_2$/Bi_2Se_3/Ag	25 × 600 μm^2	12 × 12	10	0.68	2.83×10^3	10^3	—	10^6
[228]	Ti/Pt-MoS_2-Ti/Pt	25 μm^2	6 × 6	73	1	10^2	10^7	22	10^3

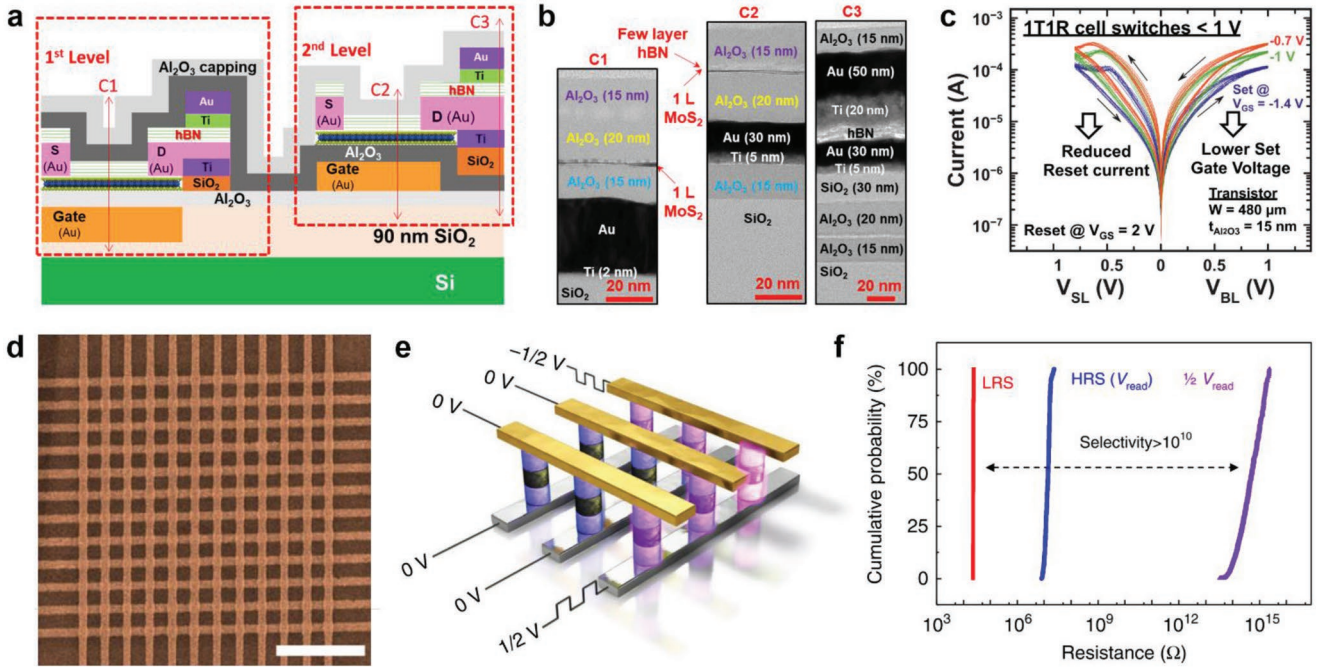

Figure 11. Access to MIM cells and sneak path currents. a) Schematic 1T1R cell comprising a 1L-CVD-MoS_2 transistor and a 10–13L-CVD-hBN RS device. b) TEM images of the sections highlighted in (a). c) *I–V* curves showing that V_{SET} can be <1 V, and that the current across 10–13L-CVD-hBN can be controlled by the 1L-CVD-MoS_2 transistor. a–c) Reproduced with permission.[190] Copyright 2018, IEEE. d) Top-view SEM image of a 10 × 10 crossbar array of RS devices with Au/≈7.6 nm MC-MLG/≈13 nm MC-hBN/≈14.6 nm MC-MLG/Au structure. e) Schematic sneak path disturbance of half-selected RS devices in crossbar array. f) Resistance in HRS (blue) and LRS (red) for a selected device in the crossbar array, and for a half selected device (purple). d–f) Reproduced under the terms of the CC-BY Creative Commons Attribution 4.0 International license (https://creativecommons.org/licenses/by/4.0).[46] Copyright 2019, The Authors, published by Springer Nature.

Ref. [46] also investigated the sneak path currents using V/2 and V/3 schemes. Figure 11e,f, reported current across unselected cells <10 fA (very low, meeting the technological specifications for both non-volatile memories and electronic synapses/neurons[4–6,63]), even without a series transistor. However, the working mechanism proposed in ref. [46] is questionable, because MC-ML-hBN does not exhibit stable bipolar RS,[131,236] and the TEM images reveal amorphous material (probably polymer residuals from the transfer) embedded between MC-ML-hBN and MC-MLG (which may generate RS).[236,237] Therefore, it is probable that the RS is induced by defects in MLG, not due to the MC-ML-hBN. Ref. [46] analyzed sneak path currents in LM-based crossbars. Similar studies should be done for LPE/CVD/MOCVD samples.

6. Circuit-Level Applications

Vertical MIM cells exhibiting RS were used to fabricate electronic circuits, including logic gates, non-volatile memories, electronic synapses, and neurons.[59] Multiple logic operations, including NOR,[238] AND,[238,239] and NAND gates,[238] as well as material implication (a binary truth functional operator that returns "true" unless its first argument is true and its second argument is false),[240–242] have been realized. Their main advantages compared to their counterparts made of CMOS transistors are easier fabrication, potential for 3d integration, reduced size,[238,240] and lower power consumption.[243] 3d-hybrid CMOS/RS field programmable gate array (FPGA) architectures showed a six-times-higher integration density[242] and ≈16.7% lower standby power consumption than static random-access memories with 1T1R arrays.[243,244] Large-scale (up to 1600 cells) hybrid CMOS/RS-device circuits[245–247] were demonstrated with a storage capacity of 16GB.[248] Standalone CMOS/RS-device-based memories require more efforts because of the sneak path currents.[249] Refs. [216,220–225] prepared RS-devices designed to exhibit multiple resistive states, and nearly analogue RS was used to emulate ANNs[250–255] and spiking neural networks,[256,257] for image classification,[251–255] and to encode neuronal spiking activities by compressing the spike amplitude and firing rate.[256] Most works[253,254,256] characterized one/few devices applying *I–V* curves or pulsed voltage stresses (PVS), and used conductance as weight of the electronic synapses in simulated ANNs (using TensorFlow,[258] PyTorch,[259] and Python[260]). Thus, refs. [253,254,256] did not fabricate an ANN, but only simulated what would be the classification accuracy of a system exhibiting such RS performance. Refs. [252,255,261–263] faced the hardware implementation of an ANN, but many challenges remain, such as reducing resistance level instability,[253,254] sneak path currents,[253] device-to-device[252,253] and cycle-to-cycle variabilities,[254,261,264] and implementation of extreme machine learning algorithms.[265]

When using LM-based RS devices, the number of circuit-level demonstrations is much scarcer. Ref. [266] presented an array of dot-like devices made of Zn/tetrakis(4-carboxyphenyl) porphyrin, and used it to store different digits, matching the

letters "S" and "Z," in the form of resistive states, and this pattern was stable for >5000 s. LPE was used in ref. [266] to fabricate crossbar arrays of RS devices, to store information generated by a near-infrared emission system. Using LPE, ref. [133] fabricated (on 4″ wafers) crossbar arrays of Al/@7.5 nm LPE-MoS_2–MoO_x/Al devices connected to pressure sensors and light emitting diodes, to store information in the form of mechanical impulses, and display it as light. Refs. [97,266–268] employed the word "programming" to refer to the operation they carried out, but all they did is store data. This may be misleading, because "programming" denotes data processing and/or computation,[269] not carried out in refs. [97,266–268].

Ref. [267] presented simple computations using crossbar arrays of Ag/PO_x/33L-MC black phosphorus/Au devices with lateral sizes ≈100 nm × 100 nm to build OR and AND logic gates. Ref. [190] fabricated a 2 × 2 crossbar array of 1T1R cells using 1L-CVD MoS_2 transistors and Au/Ti/hBN/Au RS devices, and claimed it could be used to implement matrix vector multiplication, **Figures 12**a–c, but an experimental demonstration was not presented. The use of LM-based RS devices to emulate ANNs was also explored.[93–95,178] Refs. [93–95,175] fabricated isolated RS devices with dot-like[93,175] or cross-point structure[94,95] using LPE or CVD. They measured one[93–95]/few[175] devices, and used the data to emulate a NN, using software.[258–260] This was also realized using planar RS devices,[270] and is even less competitive from an integration point of view, due to the larger lateral size and complex 3d integration. As of 2022, the only emulations of ANNs using data collected in LM-based RS devices fabricated using LPE or CVD and integrated in a crossbar network are in ref. [68]. This fabricated crossbar arrays of Au/15–18L-hBN/Au, and used them to build a multilayer perceptron (a basic type of ANN) with ≈98% accuracy in image recognition from the Modified National Institute of Standards and Technology (MNIST[271]) dataset, Figures 12d,e. Ref. [68] also simulated the disturbance (i.e., intentioned change of conductance) of half-selected cells (see Figure 11e) within the crossbar array of MIM-like RS cells, and confirmed this to be <10%, Figures 12f,g.

7. Challenges and Prospects

The main challenges of LMs-based RS devices are endurance, variability, and yield. Refs. [228,272–274] claimed high endurance (>10^6 cycles) in RS devices using CVD-1LG as impermeable blocking layer,[272,273] ≈10-nm-thick MoS_2-based RS devices produced by LPE,[228] and CVD-1L-h BN.[274] However, refs. [228,272–274] only recorded one single data point per decade in one single device, instead of one data point per cycle per state for a few (≈5) devices,[275] which is a reliable method to evaluate endurance.[202] The RS phenomenon requires one material between the electrodes that can block the current in

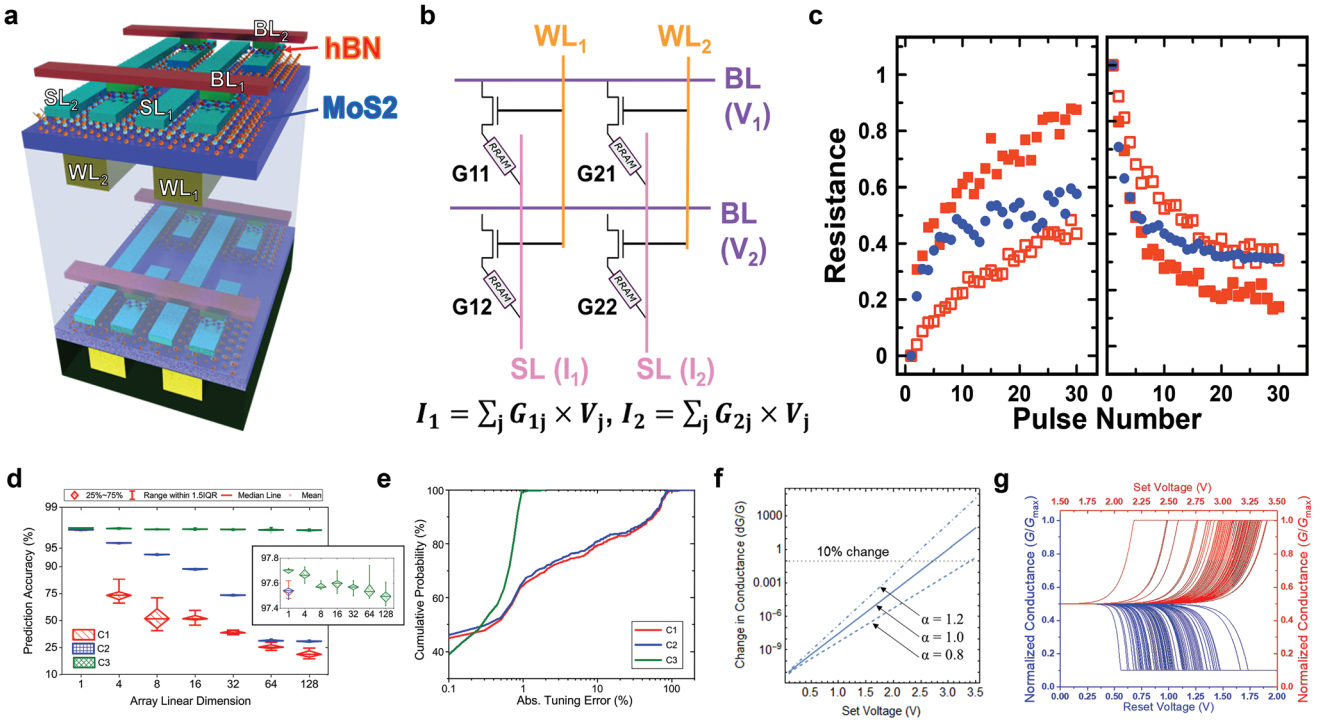

Figure 12. RS crossbar arrays for neuromorphic applications. a) Schematic two-level stacked 2 × 2 back-gated 1T1R array with Au/Ti/10–13L-hBN/Au RS devices and 1L-CVD-MoS_2 transistors. b) Schematic 2 × 2 back-gated 1T1R, indicating how matrix-vector multiplication is carried out. c) Normalized resistance changes with pulse number for set and rest processes in RS device and 1T1R cells with same pulse conditions, showing 1T1R cells have better linearity and a higher resistance window. a–c) Reproduced with permission.[190] Copyright 2018, IEEE. d) Simulations for ex situ trained ANNs showing adverse influence of increase of linear dimensions of the crossbar on half-select disturbance and classification accuracy. e) Device conductance statistics for a 64 × 64 crossbar array after modifying the accuracy in tuning algorithm to 1%. f) Relative conductance change versus V_{SET} with multiplicative factor α. g) Normalized conductance after applying set/reset pulses for 100 devices randomly chosen from a 64 × 64 crossbar array. d–g) Reproduced with permission.[68] Copyright 2020, The Authors, published by Springer Nature.

HRS, meaning that insulators (band gap >5 eV, like hBN) are preferred. However, its structure needs to be modified in a reversible manner to reach LRS. As defect-free hBN has hard bonds difficult to break (minimum energy for atomic migration >10 eV[28]), it requires the application of high energy that results in permanent damage.[131] For this reason, defect-rich CVD-hBN shows one of the best performance at the device level,[68,131,163,168] although semiconductors like MoS_2[65,228] also revealed competitive properties (see Table 4). Variability was rarely discussed,[68] Ref. 163 discussed yield-pass criteria;[163] however, these may be different to those used by companies, since these do not disclose information about the criteria they use. Clear guidelines are needed, similar to those for solar cells[276] or lasers,[277,278] requiring the publication of all necessary figures of merit.

Many RS observations were made in MIM-like devices that are very large (>100 μm^2).[133,207,222,238] The fact that one such device shows reliable RS does not mean that this will behave the same for a size <100 nm^2,[279] required in most RS technologies.[6]

Insulators without vacancies, interstitial atoms, or impurities, do not exhibit RS.[280] The reason is that in such materials the energy required to form the CNF (i.e., dielectric breakdown) is higher than in materials containing vacancies,[28] and results in an irreversible phenomenon (no reset after breakdown[131]). That is why, in most cases,[56,57] the current during the CNF formation must be limited. However, even with that, if the intrinsic concentration of native defects is very low (e.g., ≈10^{11} cm^{-2} for the field oxide charge density in SiO_2 grown by thermal oxidation with an annealing at 500 °C[281]), an electric field will result in irreversible atomic rearrangements. For example: 1) SiO_2 grown by thermal oxidation of Si has no vacancies nor impurities, but no RS.[280] Only when SiO_x is produced by other deposition methods that result in a higher density of dangling bonds (e.g., by sputtering[282]), it displays RS.[283] 2) The MC-64L-MoS_2 in ref. [65] only showed RS after exposure to an oxidative treatment to introduce O impurities. 3) hBN flakes prepared by MC do not show RS,[212] while CVD-grown ones were reported with excellent RS,[68,133] e.g., yield >98%,[68] C_V of V_{SET} <1.53%,[68] and I_{HRS}/I_{LRS} >10^{11}.[68] 4) High-k dielectrics like HfO_2 and TaO_x exhibit much better RS than thermal SiO_2, as they host a larger amount of defects.[111,115] 5) HfO_2 samples grown by atomic layer deposition only show RS when they are subjected to thermal annealing >400 °C.[284,285] This induces poly-crystallization and generates defects at GBs, the only sites that promote RS.[286,287] However, if materials contain too many defects, this can ease the lateral propagation of CNFs,[288] and result in erratic RS for few (≈45) cycles,[289] or poor endurances[66,289] (<100 cycles).

Therefore, LMs for RS should contain vacancies, interstitial atoms, and impurities, but not too many (i.e., the layered structure should be maintained and defects should be embedded). The density of defects needed to induce stable RS over millions of cycles has not been quantified for any material. Not all defects are similar. Some are clusters,[285] as the probability to form a defect in the vicinity of another is larger than when there are no other defects nearby.[290]

In MIM-like devices with large lateral size (e.g., 10^3 μm^2), the probability to find more and larger defects in the insulator increases. Ultrasmall (<100 nm^2) devices may not include enough defects to enable RS. For example, for the metal/polycrystalline HfO_2/metal systems in ref. [285], with lateral sizes ≈10^4 μm^2, devices exhibited bipolar RS, but when the lateral size was ≈50 nm^2, only ≈15% exhibited RS. It may be that devices with large lateral size (>10^4μm^2) host too many defects that results in erratic RS,[291] while smaller ones (25 μm^2) do not host such defects and show better RS.[292]

Therefore, in LMs for RS technologies it is important to ensure small (<10 nm) inter-defect distances while maintaining a high ratio between the non-defective volume (V_{ND}) and the defective volume (V_D), i.e., $V_{ND}/V_D \geq 5$,[36] not only to provide the devices with the properties of LMs (i.e., high flexibility, mechanical strength, and in-plane thermal conductivity) but also to avoid unwanted lateral expansion of CNFs toward irreversible dielectric breakdown.

CVD-grown LMs are normally polycrystalline, with grains ranging from 5 μm[179] to 1 mm.[293] GBs contain atomic defects.[294,295] Single-crystal 1L-LM can be grown at wafer scale.[144,293] Although RS devices with 1L-LMs were demonstrated,[36,296] pinholes and cracking during transfer (compared to >10L-LMs) result in a lower yield (e.g., 50% for 1L-hBN[37] vs >98% for ≈18L-hBN[68]), as even one missing atom can short RS devices, because the current flows out of plane (this is different when the current flows in-plane,[161] in which case one missing atom does not produce device failure). Controlling grain size and defects in LMs with thicknesses suitable for RS (i.e., between ≈2 and 30 nm) is challenging. Therefore, large (>10^3μm^2) devices made of CVD-LMs containing GBs, **Figure 13**a, might exhibit excellent RS with low device-to-device variability of the electrical performance (because the relative difference of V_D from one device to another is low) and high yield. On the contrary, small devices (<300 nm^2) made of CVD-LMs without local defects (Figure 13b) may not show RS, or exhibit erratic RS with very high device-to-device variability (because the relative difference of V_D from one device to another is high) and low yield. Figure 13a,b indicates that yield and device-to-device variability of large and small devices can be different.

In LPE-LMs RS devices, the flakes have diameters ranging from 0.2[25] to ≈100 μm,[118] and form junctions that contain large amounts of defects, Figures 4b and 13c,d. Similar to GBs in CVD-LMs, these defective junctions can promote out-of-plane leakage current, which could alter the RS characteristics, e.g., in ref. [298]. hBN–poly(vinyl alcohol) (PVOH) RS devices fabricated by LPE showed 4×10^{-9} A for areas 1.4×10^3 μm^2 and 7×10^{-7} A for ≈7.8×10^3 μm^2. Thus, we recommend fabricating RS devices with areas as small as possible.

Large (>10^3 μm^2) dot-like device structures patterned using a shadow mask, Figure 13e–h, used in most cases because they are the simplest to fabricate,[5] should be avoided. In large (>10^3 μm^2) devices the RS active area is exposed to the pressure exerted by the tip of the probe station,[299] which may lead to higher post-DB currents, lower DB voltages, lower variability of post-DB currents (i.e., R_{LRS}), and erratic bipolar RS cycling. As in real chips, RS devices are not exposed to the pressure of probe station tips, and this structure (Figure 13e–h) should be avoided. Ref. [115] reported a RS analysis in small MO-based devices ≈10 nm × 10 nm, fabricated in an industrial facility. Ref. [300] prepared 2 nm × 2 nm MO-based RS prototypes in a university lab, but the variability of V_{SET} was significant. We recommend the study of RS devices with sizes down to 10 nm × 10 nm, although this may be challenging. Focusing on

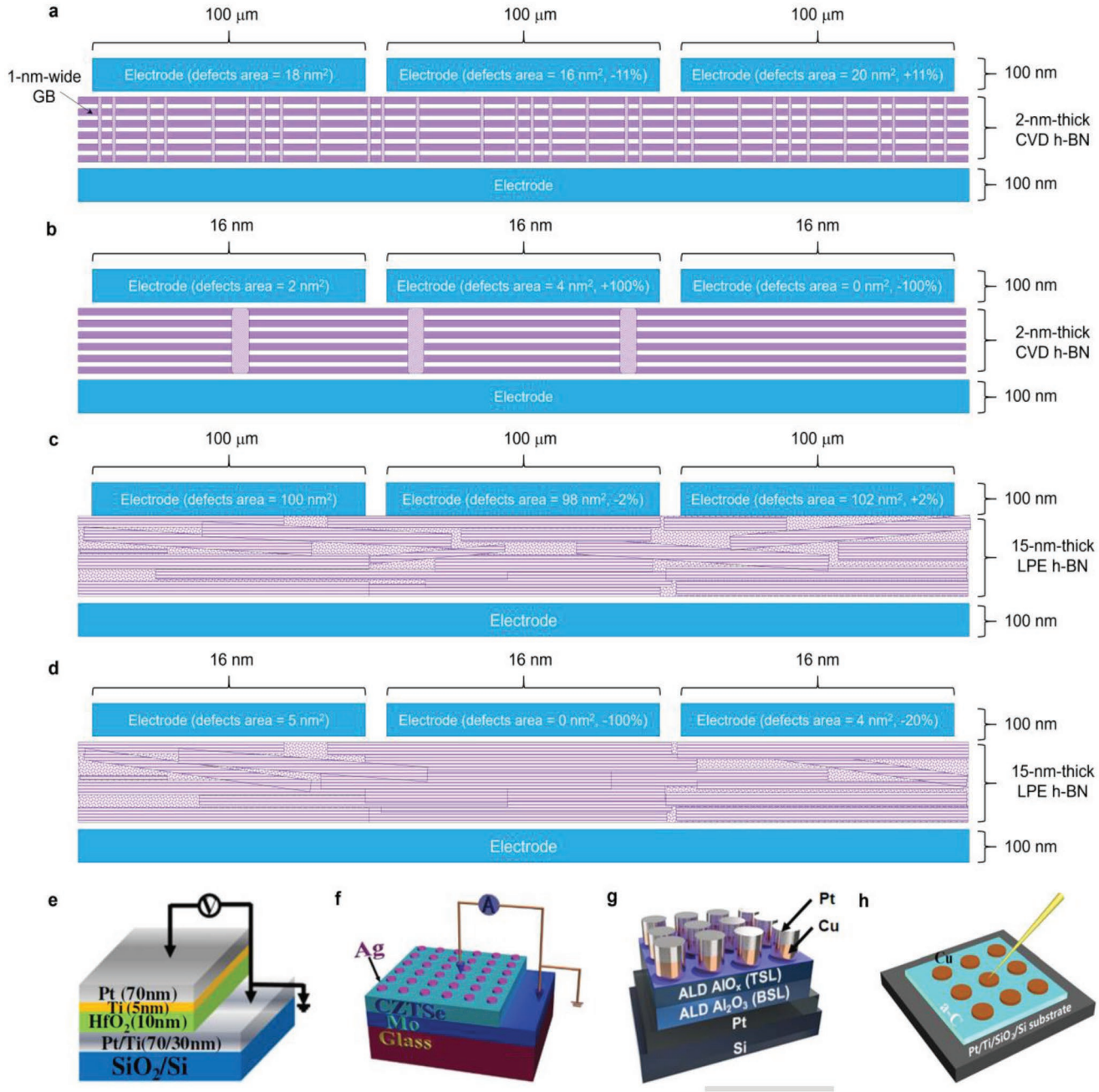

Figure 13. Importance of miniaturization in RS studies. a–d) Schematic cross section of MIM-like RS devices fabricated by a,b) CVD and c,d) LPE with different sizes: (a) and (c) are large (>10^4 μm^2) and (b) and (d) are small (<300 nm^2, the only ones considered by industry[105]). The schematics in (a,b) and (c,d) are inspired by observations made through cross-sectional TEM images presented in refs. [68] and [130], respectively: 1) the volume occupied by defects in the insulator is much smaller than in larger ones (a,c), which will result in different electrical characteristics;[279] and 2) the relative variation of the amount of defects from one device is much larger than in larger ones (a,c). The percentage in the devices in the central and right columns of (a)–(d) indicate the variation of the number of defects compared to the device in the left column. Therefore, the conclusions extracted from experiments conducted in large (>10^4 μm^2) RS devices cannot be extrapolated to miniaturized (<300 nm^2) ones. e–h) Typical scheme using common bottom electrodes to pattern large devices >10^4 μm^2. This should be avoided, as its characteristics will not necessarily be observed in nano (< 1 μm^2)-sized ones. Crossbar arrays like those in Figure 3a are recommended. e) Reproduced with permission.[212] Copyright 2012, IOP Publishing. f) Reproduced with permission.[207] Copyright 2018, Royal Society of Chemistry. g) Reproduced with permission.[222] Copyright 2018, IOP Publishing. h) Reproduced with permission.[297] Copyright 2017, The Authors, published by AIP Publishing.

devices with lateral sizes >5 μm is risky because this is similar to the grain size in CVD ML-LMs, or the flake size in LPE-LMs, and GB defects in CVD-ML-LMs, or nanojunctions in LPE-LMs, and may influence the devices electrical characteristics.

For devices with small (<100 nm^2) sizes, the current densities flowing in LRS could melt the metallic wires. For this reason, we recommend to make them thick enough (>50 nm), and employ metals that are resistant to electromigration (e.g., Pt[301] and W[302])

Table 5. Endurance of LM-based RS devices. Comparison of endurances of LM-based RS devices. Only those works that characterized the resistance in each cycle, either via *I–V* sweeps or current-visible PVS, are considered, because, according to ref. [5], the endurance should be calculated in each cycle, especially when studying prototype RS devices made of novel materials. NASE = nanoimprint-assisted shear exfoliation.[276] The endurance of metal/LMs/metal devices is still far behind than that of metal/MO/metal ones, which have surpassed 10^9 cycles in multiple studies that use the recommended characterization method.[202]

Ref.	Structure	Device size	Yield	# Cycles	Test method	Switching type
[92]	Au/CVD-1L-hBN/Au	$1 \times 1\ \mu m^2$	—	50	IV curves	Bipolar
[188]	Ti/CVD-20L-hBN/Au	$100 \times 100\ \mu m^2$	—	400	IV curves	Bipolar
[303]	Au/CVD-1L-MoS_2/Au	Planar FET channel length (2 μm)	—	15	IV curves	Bipolar
[304]	Au/CVD-1L-MoS_2/Au	Planar FET channel length (1–5 μm)	—	475	IV curves	Bipolar
[100]	Au/MC-3–80nm-Li_xMoS_2/Au	Planar FET channel length (≈5 μm)	—	1000	PVS	Bipolar
[37]	Au/CVD-1L-MoS_2/Au	$2 \times 2\ \mu m^2$	—	150	IV curves	Bipolar
[102]	Ag/MC ≈ 8 nm GaSe/Ag	Planar FET channel length (≈30 μm)	—	5000	IV curves	Bipolar
[102]	Au/Ti/10–15 nm NASE MoS_2/Ti/Au	Planar FET channel length (≈2 μm)	—	6	PVS	Bipolar
[104]	Au/MC ≈ 95 nm-α-In_2Se_3/Au	Planar FET channel length (≈1 μm)	—	100	IV curves	Bipolar
[91]	Cu/CVD-2L-MoS_2/Au	$2 \times 2\ \mu m^2$	—	20	PVS	Bipolar
[168]	Au/CVD-1L-hBN/Au	$0.5 \times 0.5\ \mu m^2$	50% (18/36)	—	IV curves	Bipolar
[169]	Pt/LPE ≈ 16 nm-bilayer-reduced GO/Pt	$60 \times 60\ \mu m^2$	72% (18/25)	1	IV curves	Bipolar
[226]	Al/LPE ≈ 15nm-GO/Al/PES	$50 \times 50\ \mu m^2$	80% (20/25)	100	IV curves	Bipolar
[227]	Ag/ZnO/sputtered 120nm-WS_2/Al	—	83.3% (15/18)	—	PVS	Bipolar
[158]	Au/Ti/CVD-10–12L-hBN/Ni	$25 \times 25\ \mu m^2$	60% (9/15)	100	IV curves	Bipolar
		$100 \times 100\ \mu m^2$	<10%	—	—	Bipolar
[68]	Ag/CVD-15–18L-hBN/Au	$150 \times 150\ nm^2$	98% (47/48)	80000	PVS	Threshold

or, possibly, 1LG. Isolated cross-point RS devices are not exposed to the disturbance in crossbar arrays. Therefore, crossbar structures are preferred as they match the requirements of industrial chips.

Before introducing one MIM-like structure in an industrial RS technology, this must be tested over millions of cycles in thousands of devices, with all parameters (V_{SET}, V_{RESET}, t_{SET}, t_{RESET}, E_{SET}, E_{RESET}, t_{HRS}, t_{LRS}) falling within the acceptable operation windows. The exact value of each parameter, the variability of the operation windows, and the percentage of devices that must fit this requirement are different for each RS technology, and each manufacturer may also use different criteria. While presenting such data is common in industrial reports,[6] very few research articles do it.[68,111] This is most accentuated in RS papers using novel materials. In some cases authors claimed the observation of RS that could be "promising" for RS technologies by presenting just one *I–V* curve in one device.[169,176] Therefore, it is essential to consider what is the minimum number of data to reach reliable conclusions.

To understand the intrinsic electrical characteristics of MIM-like RS devices (without considering degradation), we recommend to always present electrical information (either *I–V* plots or PVS plots) of least 100 cycles for at least five devices. The reason is that CNF-based RS is a phenomenon that needs to be analyzed statistically, and such a population of devices and cycles can provide an estimate of device parameters variability. The more cycles and devices analyzed, the more reliable the conclusions will be. One could expect that the more cycles and devices measured, the higher the deviation of parameters registered, because the probability to induce changes (i.e., defects) in the dielectric would be higher. In many cases the difference in variability when considering 10^2 or 10^6 cycles is very low (e.g., <2%[68]). Analyzing at least 3 batches of samples is recommended in order to evaluate manufacturing process variability.

It is also important to define what the acceptable operation windows for each device parameter are, and to disclose how many devices were measured and how many worked well, so that the yield can be calculated. We emphasize that, for any device parameter, claiming the measurement of many (>10^7) cycles and showing data corresponding to one/few cycle/s per decade, as in refs. [38,93,94,97,144], is not acceptable.[5] RS must be characterized in every cycle,[61,88,111,216] otherwise one cannot ensure that the device has switched. Misleading characterization approaches (i.e., claiming operation >10^7 cycles while showing data for one/few cycles per decade) were employed.[65,174] **Table 5** summarizes the structure and properties of LMs-based RS devices characterized in all cycles.[68,91,92,100–102,158,168,169,181,226,227,303–305]

8. Conclusions

Most RS technologies (i.e., NVM and ANN) use the crossbar array architecture due to its high integration density, therefore, RS studies employing LMs (and other novel materials) should use it too. Producing LMs using scalable methods (i.e., LPE, CVD, and MOCVD) is important for industrial applications. By analyzing the literature on crossbar arrays of RS devices fabricated using scalable methods, we concluded that LMs can provide performances not achieved with traditional materials (i.e., phase-change, metal oxide, and magnetic), such as high transparency up to 97.4%, stable I_{LRS}/I_{HRS} >10^5 for 10^4 s

for 10^4 bending cycles down to 4.2 mm radius of curvature, threshold RS with ultralow energy consumption per transition (≈8.8 zJ), variability of the relaxation time ≈8.52%, and coexistence of bipolar and threshold RS that enables the implementation of STP and LTP in the same device. Other properties, such as thermal stability up to ≈300 °C should be further confirmed statistically. High yield up to 98%, low variability (C_V of V_{SET} ≈1.53%) for >100 devices, and low sneak path currents <10 fA have been achieved. RS devices made of LMs were used in logic gates, and 1T1R cells. Studies on crossbar arrays of RS devices should aim for smaller areas (ideally <10 nm × 10 nm but, as that may be too challenging for most academics, here we propose <100 nm × 100 nm, which is achievable via EBL[68]) and provide yield and variability information of the main parameters (R_{HRS}, R_{LRS}, V_{SET}, V_{RESET}, t_{SET}, t_{RESET}, E_{SET}, E_{RESET}, retention time). Larger crossbar array sizes (>10 kbit) and hardware-enabled computational operations (i.e., vector matrix multiplication) should be used, not just simulations.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

crossbars, layered materials, memristors, resistive switching

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