Resistive Switching (RS) devices are metal/insulator/metal cells that can change their electrical resistance when electrical stimuli are applied between the electrodes, and they can be used to store and compute data. Planar crossbar arrays of RS devices can offer a high integration density (>10^6 devices mm^-2) and this can be further enhanced by stacking them three-dimensionally. The advantage of using layered materials (LMs) in RS devices compared to traditional phase-change materials and metal oxides is that their electrical properties can be adjusted with a higher precision. Here, the key figures-of-merit and procedures to implement LM-based RS devices are defined. LM-based RS devices fabricated using methods compatible with industry are identified and discussed. The focus is on small devices (size < 9 µm²) arranged in crossbar structures, since larger devices may be affected by artifacts, such as grain boundaries and flake junctions. How to enhance device performance, so to accelerate the development of this technology, is also discussed.

1. Introduction

Some materials can change electrical resistance between two values when they are exposed to controlled electrical stimuli.[1] This property, called resistive switching (RS), has attracted the attention of the semiconductors industry[2] because it may be used to emulate the ones and zeros of the binary code, therefore to store digital information.[3] In order to use RS materials to fabricate electronic memories that could compete with the mainstream commercial ones (i.e., NAND flash and dynamic random access memory), some technological requirements need to be met. The most important are (Table 1): 1) the resistance in high resistive state (HRS, i.e., R_HRS) should be at least ten times higher than that of the low resistive state (LRS, i.e., R_LRS), so that both can be read reliably,[4–6] 2) the switching time should be <1 ns,[4–6] so that they can be used to store information produced by integrated circuits operating at high clock frequencies (>1 GHz); 3) the switching energy should be <1 pJ,[4–6] so that the overall energy consumption is low (<1 pJ), to minimize ventilation and enable their use in wearable and self-powered technologies; 4) the material should be able to switch between the two resistive states at least 10^{13} times before one of them becomes permanent, i.e., 2 × 10^{12} transitions, half from HRS to LRS (i.e., set) and half from LRS to HRS (i.e., reset), so that the lifetime of the memory can be in the order of years. This property is often called switching endurance;[4–6] 5) each resistive state needs to be stable for at least 10 years (at 85 °C) if no electrical stimuli are applied, so that no data is lost. This is often called state retention time.[4–6] 6) RS needs to be demonstrated in small areas (<100 nm²), so that high integration >10^11 bits cm^-2 can be achieved.[4–6]

The main parameters of RS devices are: 1) switching voltages (V_SET, V_RESET). 2) state resistances (R_HRS, R_LRS). 3) switching times (t_SET, t_RESET). 4) switching energy (E_SET, E_RESET). and 5) state retention time (t_HRS, t_LRS). These can change from one cycle to another (for the same device) and from one device to another.[5,11] The variations of these parameters can be quantified by calculating the coefficient of variance (C_V), i.e., the standard deviation divided by the mean value.[12,13] Each RS technology allows a degree of variability of device parameters, and a range of acceptable values (often called operation window).[5,11] The devices that cannot be operated reliably within this window produce failure and reduce yield, i.e., the percentage of devices with parameters within the operation window.[14] In general, most RS technologies require high yields >90%,[15,16] although most studies do not disclose data about the yield pass criteria, hence making reliable comparisons difficult. As of 2022, there is no RS device exhibiting (simultaneously) all the performances required for high-integration electronic memories (see Table 1). For RS memories some parameters are even better than for NAND flash, but the maximum integration
densities achieved are rather poor. For this reason, RS-based electronic memories are still not being used for high-density (>10⁶ bits mm⁻²) non-volatile digital information storage (most products still rely on the NAND flash memory unit[27,28]), and the segment of the memory market covered by RS memories is still very small (~0.32% in 2020).[4]

State-of-the-art RS devices are made of phase-change materials, metal oxides (MO), or magnetic materials,[4,5,8,9] and these are the only materials used to date by leading companies like Everspin,[8] Intel,[9] TSMC,[18] and IMEC.[19] Organic materials,[20] quantum dots,[21,22] and sulfides[23,24] were also used for RS, however fabrication of crossbar arrays was not reported, which means that they are limited to a proof-of-concept RS observation and their impact in commercial RS technologies is negligible. The material systems that so far have achieved the best performance (i.e., lowest switching time and energy and highest endurance and retention time) when used as RS memories are crossbar arrays of vertical metal/insulator/metal (MIM) nanocells (Figure 1a). When an external bias is applied, the conductance of RS devices is modified through atomic rearrangements in the MIM nanocells, which can follow various physical phenomena: 1) phase-change,[25] 2) metallic ion penetration from electrodes,[26,27] oxygen vacancies formation, or electron trapping and de-trapping[28] in metal oxides,[29] 3) spin modification.[30,31] Electrical-field-driven thermal effects can also play a role in accelerating such atomic rearrangements,[32] therefore thermal conductivity is important. The atomic rearrangements can be distributed equally within the entire volume of the RS device,[33] or localized at the interfaces,[34] grain boundaries (GBs),[35–36] across a conductive nanofilament (CNF),[37] or at a single atomic dislocation.[38] To the best of our knowledge, the exact materials composition of commercial RS products (i.e., memories) is unknown, because companies do not reveal such information.

As of 2022, all RS devices still suffer from a too high device-to-device variability, meaning that for a large (>10⁶) population of devices it is still impossible to ensure that the minimum switching energy of RS devices will be greater than ten times the maximum switching energy for all cycles in all devices (see Figure 2). Every time one cycle of one device does not meet this criterion, erroneous data is stored and/or read (see gray arrows in Figure 2c). Reaching R_HRS_MIN/R_LRS_MAX >10 for all cycles of all devices is easier when the number of devices is lower (<10⁶), which has enabled the use of RS devices in sensors[39] and photodetectors,[40,41] and low-density (<100 megabytes) memories.[39,42] However, device-to-device variability is hindering the implementation of RS devices as mainstream memory for high-density (>10¹¹ bits cm⁻³) information storage (in the gigabyte range). Moreover, when one MIM cell within the crossbar array is addressed (by applying electrical stimuli to one row and one column)[35] the surrounding MIM cells are also exposed to part of the electrical stress, which creates additional paths for current flow from one electrode to another (often called sneak paths or sneak currents).[43] In order to control better the current flow across each cell (i.e., minimize variability and sneak currents), one common solution is to connect additional electronic devices in series to each MIM-like RS device in the crossbar array, such as transistors[44,45] (leading to 1-transistor–1-resistor [T1R] configurations) or selectors.
These elements can also serve as immediate current limitations (i.e., without delay time), which is beneficial to avoid undesired over-shot current (i.e., a short-time current above the pre-set current limitation until this enters in operation), enhancing the lifetime of the devices. The integration of crossbar arrays of MIM-like RS devices with these additional elements (or with other logic circuits necessary at the system level) does not necessary represent an increase of area, as MIM-like RS devices can be integrated on the back-end-of-line (BEOL) interconnections of the transistors, and selectors are two-terminal devices that can be placed on top/bottom of the RS device. Nevertheless, some companies now consider that overcoming variability and reliability challenges in RS devices is too big, and have stopped/decreased their work on RS-based electronic memories.

RS devices exhibiting multiple resistive states may increase the storage capacity from \(2^n\) to \(X^{n\times m}\), where \(X\) is the number of resistive states and \(n\times m\) is the number of RS devices used (i.e., the size of the crossbar array, with \(n\) rows and \(m\) columns). However, in this case, distinguishing the resistive state in all cycles for all devices is even more challenging, as the resistance ratio from one state to the adjacent one is narrower than within only two states. Refs. [55–57] reported multilevel RS devices using vertical metal/MO/metal nanocells, without providing statistical information on what percentage of devices showed similar resistive states without mismatch (i.e., yield). Therefore, such prototypes are not yet useful as RS-based memory technologies and, as of 2022, there is no commercial (standalone or embedded) non-volatile memory using multilevel RS devices, due to the difficulty in distinguishing all states for all devices, as well as the low yield.

MIM-like RS devices can also be employed to construct electronic neurons and synapses for artificial neural networks (ANNs) and neuromorphic computing.
circuit architectures that can process and store information in parallel (similar to biological brains) so that no data transmission between the central processing unit and the memory is needed.[39] This is very attractive because it reduces the energy and time required to carry out each operation. E.g., ref. [60] designed an artificial synapse for “brain-on-a-chip” with energy consumption 1000 times smaller than that of traditional chips.[60] In these systems, RS devices can act either as electronic synapses (enabling analogical switching between multiple stable states[60]) or as electronic neurons (enabling highly non-linear (slope < 1 mV decade⁻¹) switching between two states with self-recovery after short times < 30 s).[62]

The technological requirements of MIM-like RS devices for ANNs and neuromorphic computing are still under debate.[16,63] The current view is that they need to exhibit multiple states (i.e., 2–32[62] 20–100[63]), but there is no consensus on the stability required (some claim from few seconds to days,[56] while others 10 years[63]). Achieving a low switching energy per state transition (= 10 fJ) is also considered essential, but challenging.[16,63]

Endurance ≈ 1 ms,[61] ≈ 3 × 10⁶ potentiatio and depression cycles (i.e., switching from the least to most conductive states stopping in intermediate ones, and back to the least conductive one), R_{HRS}/R_{LRS} ≈ 4.[6,61] There is also no clear vision yet on device-to-device variability of the number of stable resistive states and their values.

Hundreds of papers have claimed that novel materials (different from phase-change, metal oxides and magnetic) and structures (different from vertical MIM cells) exhibit RS behaviors that make them “promising” for electronic memories,[64–66] ANN[67,68] and/or neuromorphic computing.[69,70] Other performance requirements are less strict compared to those for non-volatile memories, i.e., operating speeds = 1 ms,[61] endurance ≈ 3 × 10⁶ potentiatio and depression cycles (i.e., switching from the least to most conductive states stopping in intermediate ones, and back to the least conductive one), R_{HRS}/R_{LRS} ≈ 4.[6,61] There is also no clear vision yet on device-to-device variability of the number of stable resistive states and their values.

As of 2022, the only device structure being considered by companies working on RS technologies is the crossbar array of vertical MIM nanocells,[5] due to its high integration density (4F² footprint, where F is the minimum feature,[117] which can be < 10 nm[115]). As high-density crossbar arrays of MIM nanocells cover large areas (> 10⁴ µm²[76]), MC may not produce large enough LMs.

LMs are solids with highly anisotropic bonding, constituted by sheets internally strongly bonded, but only weakly bonded to adjacent layers. Graphene is a single layer of graphite, with many unique properties, from electronic to chemical and from optical to mechanical.[118] It has opened a floodgate for many other LMs to be studied.[119] These are often referred to as 2D materials. However, we prefer to use the term LMs, since only a few of them are truly one atom thick once exfoliated, e.g., graphene and hexagonal boron nitride (hBN), while most of the others consist of multiple atomic layers, e.g., MoS₂ or WSe₂.

For a given material, the range of properties and applications can be tuned by varying the number of layers and their relative orientation. LM hetero-structures with tailored properties can be created by stacking different layers.[120] The number of bulk materials that can be exfoliated runs in the thousands,[119] but only very few have been studied to date.[118]

Scalable methods to produce LMs, such as liquid phase exfoliation (LPE)[121–123] and chemical vapor deposition (CVD)[124,125] or metal–organic CVD (MOCVD)[126–129] are necessary. However, LMs exfoliated by LPE may contain flakes with random orientations and disordered junctions (Figure 3a–c),[130] and those deposited by (MO)CVD may contain local defects that propagate from one layer to another[131] (Figure 3f). The most common techniques employed to detect thickness fluctuations, defective bonding, polymer residuals, wrinkles, suspended LMs, and twin boundaries are conductive atomic force microscopy (AFM)[68] and cross-sectional transmission electron microscopy (TEM).[36] Ref. [132] also used time-of-flight secondary-ion mass spectrometry and total-reflection X-ray fluorescence measurements to evaluate the Cu density remaining in LMs after transfer. Any general observation using MC-LMs needs to be confirmed in LMs obtained via scalable methods (i.e., LPE, (MO)CVD) before claiming it to be “promising” for wafer-scale technologies.

Ref. [133] fabricated crossbar arrays of Al/7.5 nm MoS₂–MoO₃/Al by spin coating LPE-MoS₂, and achieved fully coverage of 4″ wafers (Figure 3a), but the lateral size of the devices was 3600 µm², too large for extracting conclusions applicable to high-density technologies (i.e., with devices < 0.1 µm²).

Ref. [130,134,135] used LPE to exfoliate MoS₂ and achieved smaller sizes (= 2500 µm²), for smaller crossbar arrays (i.e., just 5 × 5[134]). When using LPE, the resulting films are usually thicker (= 10 nm[136]) and show larger thickness fluctuations (surface roughness = 3 nm[137]) than CVD-LMs (which

2. Device Fabrication

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can be <1 nm\textsuperscript{[118]} and peak-to-valley distances <150 pm\textsuperscript{[138]}. The presence of flakes with random orientations and defective junctions in insulating LPE-LM films (Figures 3b,c), increases the inhomogeneity of the MIM cells, resulting in a higher variability of state resistances and switching voltages\textsuperscript{[133]} than CVD devices.\textsuperscript{[68]}

The (MO)CVD synthesis of LMs usually requires high temperatures >850 °C\textsuperscript{[67,118–141]} Graphene growth at low temperatures compatible with CMOS technologies has been reported,\textsuperscript{[142,143]} but those methods either resulted in a lower quality or are not widely employed.\textsuperscript{[142,143]} Thus, at present, LMs are not grown directly on wafers containing patterned circuits, but on an optimized substrate (e.g., single crystal or polycrystalline metals\textsuperscript{[144]}), and then transferred\textsuperscript{[145–147]} onto the patterned wafers. Some LMs (e.g., graphene, hBN) often require Cu substrates for CVD,\textsuperscript{[147,148]} which could contaminate patterned wafers even if the growth temperature would fit front-end-of-line (FEOL) and BEOL thermal budgets (<450 °C).\textsuperscript{[149]} MOCVD was used for hBN on (Cu-free) SiO\textsubscript{2}/Si wafers.\textsuperscript{[150]}

There are different transfer processes: wet,\textsuperscript{[151]} dry,\textsuperscript{[152,153]} and semi dry.\textsuperscript{[154]} All consist of four main steps: 1) deposit a scaffold (normally a polymer) on the LM, 2) detach the scaffold/LM from the substrate (either by etching the substrate or by delamination), 3) attach the scaffold/LM to the target substrate, and 4) remove the scaffold and clean the resulting LM/substrate. These processes introduce contamination into the LM, either from the substrate (10\textsuperscript{13} to 10\textsuperscript{15} Cu atoms cm\textsuperscript{−2}\textsuperscript{[132]}), or scaffold (poly(methyl methacrylate)\textsuperscript{[123]}), and can produce cracks (especially in monolayer (1L)-LMs), wrinkles, and folds.\textsuperscript{[155]} Transfer-free LMs and electronics were also reported,\textsuperscript{[156–158]} however, the use of low (300 °C\textsuperscript{[141]} temperature results in LMs with lattice distortions, missing bonds, interstitials, and amorphous regions, resulting in worse materials properties.\textsuperscript{[156–158]} Wafer-scale ultraclean and wrinkle-free transfer processes were developed.\textsuperscript{[159–161]} The effect of wrinkles and contaminants on MIM-like RS devices is not as severe as in other devices, such as field-effect transistors (FETs), since, unlike FETs (in which the current flows homogeneously in-plane), the out-of-plane currents driven by RS devices flow only across the most conductive spots.\textsuperscript{[162]} Therefore, wrinkles and polymer residues locations have a higher out-of-plane electrical resistance compared to clean ones,\textsuperscript{[163]} meaning that CNFs do not form there.\textsuperscript{[164]} See Figure 4. On the contrary, LM atomic defects (when used as dielectric) produce dangling bonds across which the trapping of electrons is easier, and where the energy needed to generate the filament is lower.\textsuperscript{[128]} Therefore, these locations are prone to host the CNFs when an electric field is applied. If the area covered by the wrinkles and contaminants is low (i.e., <10%), device-to-device variability is negligible.\textsuperscript{[165]} Ref. [68] reported that, when the width of the wires in the crossbar array and the distance between them is reduced from 3 μm to 750 nm (for both), the amount of wrinkles in the LM is reduced (see Figure 3d,e) probably due to an increase of surface roughness, since this would enable strain to be released by adapting to the rougher contour of the sample surface.\textsuperscript{[165,166]} The transfer process can also result in uncontrollable cracks due to the introduction of biaxial strain,\textsuperscript{[167]} which can short-circuit a group of devices,\textsuperscript{[3]} decreasing yield.\textsuperscript{[6]} The thicker the LM the lower the
amount of cracks produced during transfer.[163] Refs. [92,168] fabricated Au/hBN/Au devices using transferred 1L-hBN and observed large on/off ratio (up to $10^7$) and fast switching (<15 ns), but the maximum yield was 50%.[168] Ref. [68] fabricated Au/hBN/Au using transferred ≈18L-hBN, and achieved a yield ≈98% (102 out of 104 devices worked correctly).

RS devices made of LMs synthesized by CVD[68] or LPE[169] exhibit RS. Refs. [26,32,35] investigated the switching mechanism combining cross-sectional TEM images with nanochemical measurements (e.g., electron energy loss and energy-dispersive X-ray spectroscopies) or atomistic calculations (e.g., first principles and molecular dynamics).[131] In multilayer (ML)-hBN, RS is enabled by the penetration of metallic ions from the electrodes, favored by the migration of B vacancies.[131] This is very similar to TMDs,[170] although in these the penetration of metal may not be necessary, as the generation of chalcogen vacancies leaves behind a metallic CNF,[65] not happening in hBN after the generation of B vacancies.[131] When the material is 1L, RS can be produced by the migration of a single atom (i.e., B in hBN[168] and S in MoS$_2$[170]), without metal penetration. In graphene oxide (GO), RS can be enabled both by the migration of oxygen (when using stable electrodes[27,171]) or by the penetration of metal (when using active electrodes[27,74,157]). Refs. [171,172] illustrated possible RS mechanisms using cartoons and schematics, but not backed by direct measurements or computation.

3. Advantages of LMs over TMO for RS Devices

A few studies on RS devices made of LMs[68,131,D3,D4] reported performances not yet achieved with phase-change, metal oxide, or magnetic materials (see Figures 5–10). Ref. [107] summarized
Figure 5. Transparency of LMs-based memristive crossbar array. a) Schematic and optical image of a transparent and flexible crossbar array of 2LG/SiO$_x$/2LG RS devices, with light transmittance shown in (b). c) Current of devices in panel (a) in HRS, and LRS currents after up to 300 bending cycles ($R = 0.6$ cm). a–c) Reproduced with permission.[174] Copyright 2012, Springer Nature.

Figure 6. Typical non-volatile and volatile RS in LMs-based RS devices under RVS and PVS. a,c) Typical non-volatile bipolar and b,d) volatile RS observed in Au/hBN/Au synapses with different sizes. The current limitations are $10^{-10}$ A in (b), 1 µA (blue), 1 mA (red) in (c), and $10^{-6}$ A in (d). e,f) I–t plots applying pulsed voltage stresses to an Au/Ti/15–18L-CVD-hBN/Au RS device, showing initially volatile RS (e), followed by non-volatile RS (f) as the stress proceeds. a,b,e,f) Reproduced with permission.[131] Copyright 2018, The Authors, published by Springer Nature. c,d) Reproduced with permission.[68] Copyright 2020, The Authors, published by Springer Nature.
proof-of-concept RS in different materials, including MoS$_2$, TaS$_2$, MoTe$_2$, WS$_2$, hBN, and WSe$_2$, without advantages with respect to phase-change, metal oxide and magnetic materials in terms of switching time, switching energy, endurance, state retention time, and/or integration capability. Refs. [179–181] are not only inferior to RS devices made of phase-change, metal oxide, or magnetic materials in terms of single device performance, but also have more complex fabrication process [179,180] and higher device-to-device variability [68,181] and lower yield [37,158].

The properties of LMs-based RS devices that are superior to phase-change, metal oxide, or magnetic materials RS devices are: 1) Controllable transparency. This can be adjusted by changing the number of layers [174] (see Figure 5), and may be useful to integrate memristors in transparent products (cameras [187]) and to activate the devices via light [188]. 2) Controllable RS regime. The operation of hBN-based RS devices is possible in both threshold (i.e., volatile [189]) and bipolar (i.e., non-volatile [26]) regimes (see Figure 6). The control of the regime can be achieved by tuning the current limitation of the semiconductor parameter analyzer [36] by changing the gate voltage of a series transistor [190,191] or the value of the series resistor [190]. This cannot be done with RS devices made of phase-change, metal oxide, or magnetic materials (they may show some degree of coexistence, but the characteristics are erratic and disappear after some cycles) [61] while with hBN these two regimes are programmable and very stable [68,131]. Controllable RS adds versatility to the devices, as they could be employed as both electronic synapses and electronic neurons in deep neural networks, or as both memristors and selectors in electronic memories. 3) Controllable potentiation. Refs. [61,182–184] reported erratic potentiation in RS devices made of traditional (HfO$_2$, SiO$_2$, TiO$_2$, Si$_3$N$_4$) materials, whereby the upwards trend showed sudden decrease of conductance at some specific pulses (see Figure 8a–d). This is not observed for hBN-based RS devices (see Figure 8e,f). Controllable potentiation can be used to precisely recognize the states during the analogue training, which should be helpful to program the memristors at the exact weights required in deep neural networks based on the back-propagation algorithm. 4) Controllable relaxation. Ref. [61] reported erratic relaxation in RS devices made of traditional materials, whereby the
downwards trend showed sudden increase of conductance over time, and the relaxation time had large cycle-to-cycle variability (see Figure 9a). This is not observed for hBN-based RS devices (see Figure 9b). Controllable relaxation can be applied to ensure the correct return to the initial state of electronic neurons for deep neural networks after firing, which helps reduce the probability to get stuck in a conductance state higher than the initial, hence improving reliability. 5) Ultralow energy consumption per state transition, down to 8.8 zJ (see Figure 10c). This property can be useful to integrate the devices in wearable and self-powered products, especially for the Internet of Things.

Ref. [169,173,174] fabricated crossbar arrays of MIM cells with high (up to 97.4%) transparency, which could be interesting for sensors integrated in solar cells, lenses, cameras, and contact lenses. Ref. [169] used 16 nm thick LPE reduced GO (RGO) as dielectric in crossbar arrays of RS devices with Pt electrodes. The Pt electrodes (i.e., the wires) reduced the transparency of the array. Ref. [173] fabricated MIM-like RS devices using a mixture of polyimide (PI) and 6-phenyl-C61 butyric acid methyl ester (PI:PCBM) as insulator, highly transparent (92%) multilayer graphene (MLG) prepared by wet transfer as top electrode, and Al as bottom one. Refs. [173,174] did not disclose the transparency of the entire device (only that of MLG), which is unfortunate, since the 50-nm-thick bottom Al electrode reduces the overall transmittance. Ref. [174] achieved ≈90% transmittance using bilayer graphene (2LG), fabricated by layer-by-layer transfer, coupled with SiOx deposited by electron beam evaporation, see Figure 5. Ref. [192] reached ≈97.4% transmittance by using doped monolayer graphene (ILG, CVD grown, ≈1 kΩ sq−1).[192] Refs. [169,173] reported large-area (>104 µm2) dot-like RS devices with the assistance of a shadow mask, and applied mechanical stresses using bending radiiuses (R) ranging from 4.2 mm to 1.2 cm.[169,173] Accurate control of light transmittance across LMs-based RS devices cannot be done when employing phase-change, metal oxide, or magnetic materials. This offers one important tool for the design of RS devices for optoelectronic applications.

LMs were also used to fabricate RS devices with both threshold (i.e., volatile) and bipolar (i.e., non-volatile) RS, depending on the electrodes (Ag for threshold[68,193] and Au for bipolar[68,163]), and sometimes simultaneously (using Ti)[36] see Figure 6a–d. This is useful for electronic synapses and neurons[133] and difficult to achieve in RS devices made of phase-change, metal oxides, or magnetic materials. Ref. [36] reported both threshold and bipolar RS in 50 µm × 50 µm Au/Ti/I=18L-CVD-hBN/Cu dot-like devices fabricated with the assistance of a shadow mask. Ref. [68] also achieved this for Au/Ti/I=18L-CVD-hBN Au cross-point devices with sizes ≈5 µm × 5 µm (fabricated via photolithography) and 150 nm × 150 nm (fabricated via electron beam lithography [EBL]). Ref. [131] used ≈5–7L hBN to fabricate memristive electronic synapses. Threshold RS was used to emulate short-term plasticity (STP, i.e., volatile conductance changes that self-recover in few ms[194] Figure 6e), and bipolar RS was used to emulate long-term plasticity (LTP, i.e., non-volatile conductance changes stable for minutes/hours,[195]
Figure 6f). The coexistence of both regimes in a single device simplifies the design of ANNs and neuromorphic systems, usually requiring two\cite{61} or more\cite{196,197} RS devices and complex algorithms\cite{198} to emulate STP and LTP. The threshold RS in hBN-devices was so reproducible that relaxation followed an exponential curve with low (≈8.52%) cycle-to-cycle variability of the relation time ($t_{\text{RELAX}}$), Figure 6e,\cite{68,131} outstanding compared to RS based on SiO$_x$\cite{61} and metal oxides.\cite{199,200} Previous experiments demonstrated that metal oxides, such as HfO$_2$ and CuO, do not offer the possibility of switching from one RS regime to another, with coexistence of both RS regimes erratic and lasting for few cycles.\cite{36,131}

Apart from the inherent and versatile operation of LMs-based RS devices in both volatile and non-volatile modes, the conductance can be more accurately controlled than in metal/MO/metal devices, both when it is increased and decreased (i.e., the device is potentiated and depressed, or relaxed). Refs. \cite{61,182–184} showed the typical potentiation behavior for metal/MO/metal and metal/SiO$_x$/metal RS devices when a sequence of pulses is applied (Figure 8a–d), and observed that the currents/conductance increase (or resistance decrease) erratically, i.e., in some pulses the device exhibits a lower conductance than in one/few of its
Figure 10. Threshold RS in LMs-based RS devices. a) I–V plot for one Ag/0.9 nm BNOx/SLG threshold RS device (fabricated via MC) showing bipolar RS at $I_{CC} \approx 0.9$, 5 and 9 pA. Stable switching over 100 cycles and ~14% variability of the set voltage is demonstrated for operating currents of 5 pA. Reproduced with permission.[68] Copyright 2017, Wiley-VCH. b) I–V plots for an Ag/15–18L-CVD-hBN/Ag RS device showing reproducible threshold RS for $I_{CC} \approx 1$ pA. c) I–V curves applying pulsed voltage stresses to an Ag/15–18L-CVD-hBN/Ag RS device, showing a switching time $\approx 200$ ns, with energy consumption per state transition $\approx 8.8$ zJ.[68] Reproduced with permission.[68] Copyright 2020, The Authors, published by Springer Nature.

predecessors. On the contrary, ref. [131] demonstrated that in metal/hBN/metal RS devices the current undergoes a very smooth increase with number of pulsed voltages, with all pulses showing more current than all their predecessors (see Figure 8e,f). The superior controllability of potentiation and depression processes in CVD ML-hBN (compared to metal oxides and phase-change materials) may be related to the lower number of atoms involved in the switching.[28] The RS in ML-hBN is produced by CVD and is driven by few-atom-wide amorphous defects embedded in the crystalline lattice (see Figure 2b, image 2).[68] These local defects are confined within a crystalline hBN in each layer, which is not involved in the switching due to the higher energy for vacancy formation (as demonstrated by first principles calculations[28]). These stable atoms in the crystalline lattice result in a confinement effect that prevents lateral propagation of the CNF that produces the switching (as demonstrated via conductive AFM,[28] see Figure 7).

A similar observation can be made for the relaxation of RS devices. When MIM-like RS devices are operating in non-volatile (i.e., threshold) regime and the voltage is switched off, the current across the devices reduces progressively until zero, due to the partial/complete disruption of the CNF across the insulator. Refs. [61,182–184] showed that when the insulator is a metal oxide or SiO$_2$, the current reduces in an erratic manner, with current upward/downward trends and with different relaxation times (i.e., time since the voltage is reduced until the current is zero), Figures 8a–c. However, ref. [68] showed that, when using metal/LMs/metal RS devices, the relaxation of the currents takes place in a much smoother manner, and the relaxation time follows an exponential law and increases with the voltage applied during the pulse (see Figures 8b,c). This can be beneficial when fabricating leaky integrate-and-fire electronic neurons for neuromorphic applications.[4–6]

Ref. [68] used 15–18L-CVD-hBN to fabricate threshold RS devices with ultralow energy consumption. Ref. [90] reported threshold RS between two ultralow current levels with SLG/0.9 nm BNOx/Ag (fabricated via MC), with HRS = 10 fA and LRS = 5 pA, Figure 10a. Ref. [68] demonstrated switching between 10 fA (HRS) and 110 fA (LRS), with >2000 cycles in six Ag/15–18L-CVD-hBN/Ag. The estimated energy consumption per state transition was $\approx 8.8$ zJ, Figures 10b,c, while the previous record in metal/MO/metal devices (i.e., TiN/Hf/HfO$_2$/TiN and Al/Ti/Al$_2$O$_3$/s-CNTs, where s-CNTs = semiconducting carbon nanotubes) was 0.1 pJ per transition.[11,201] State transition energies in the zJ range were not reported to date in RS devices made of phase-change, metal oxide, or magnetic materials.

Ref. [65] fabricated MIM-like RS devices using MLG electrodes and ~40 nm MoS$_2$ as dielectric layer (all obtained by MC), and reported stable bipolar RS operation during >100 cycles at $\approx 300$ °C. This was included in the IRDS[66] as a potential advantage of LMs-based RS devices. However, this finding was achieved using MC[65] and not yet reproduced. The $10^6$ cycles in ref. [65] were based on one data point per decade. Ref. [202] suggested that one data point per cycle is more reliable.[202] Hence, the superior thermal stability of LMs-based RS devices needs to be further demonstrated statistically in devices fabricated using scalable methods (LPE, CVD, MOCVD).

4. Yield and Variability of LMs-Based RS Devices

RS devices made of phase change and metal oxide materials show variability (within a single device) related to the stochasticity of the switching mechanism (CNF formation across the metal oxide and melting in phase-change).[1] The variability from one device to another is related to imperfections in the fabrication process (which produce inhomogeneity), resulting in devices with different microstructures (e.g., thickness fluctuations and different densities of defects).[3]

Refs. [203–215] analyzed the variability of metal/MO/metal RS devices (see Tables 2 and 3), most of them coming from companies. As of 2022, the best performances for a single device were reported by refs. [203,210], with CVs of $V_{SET}$ and $V_{RESET}$ = 1% and 1.62%, respectively. However, only one device was presented[205,210] and device-to-device variability was not discussed.[210] Ref. [211] reported ITO/Eu$_2$O$_3$/ITO/PET with device-to-device
devices quantified the cycle-to-cycle variability of $V_{\text{SET}}$ and $V_{\text{RESET}}$ of RS devices (made of any material) from one cycle to another. The size of the cells and the value of the current in LRS are also indicated, to evaluate how competitive the devices are in terms of integration density and energy consumption. The table shows that many studies on metal/MO/metal RS devices have quantified the cycle-to-cycle variability of $V_{\text{SET}}$ and $V_{\text{RESET}}$, but for metal/LMs/metal RS devices such analysis is often not reported.

Table 2. Cycle to cycle variability of RS devices. $C_v$ for $V_{\text{SET}}$ and $V_{\text{RESET}}$ of RS devices (made of any material) from one cycle to another. The size of the cells and the value of the current in LRS are also indicated, to evaluate how competitive the devices are in terms of integration density and energy consumption. The table shows that many studies on metal/MO/metal RS devices have quantified the cycle-to-cycle variability of $V_{\text{SET}}$ and $V_{\text{RESET}}$, but for metal/LMs/metal RS devices such analysis is often not reported.

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Device structure</th>
<th>Device size</th>
<th>$I_{\text{LRS}}$ [at 0.1 V]</th>
<th>$C_v$ [$V_{\text{SET}}$]</th>
<th>$C_v$ [$V_{\text{RESET}}$]</th>
</tr>
</thead>
<tbody>
<tr>
<td>[203]</td>
<td>TiN/HfSiO$_2$/Pt</td>
<td>1 $\times$ 1 µm$^2$</td>
<td>=5 µA</td>
<td>5.05%</td>
<td>4.78%</td>
</tr>
<tr>
<td>[204]</td>
<td>W/HfO$_2$/TiN</td>
<td>400 $\times$ 400 nm$^2$</td>
<td>0.1 mA</td>
<td>—</td>
<td>3.15%</td>
</tr>
<tr>
<td>[205]</td>
<td>Ag/Pd/SiGe/pSi</td>
<td>5 $\times$ 5 µm$^2$</td>
<td>=10 µA</td>
<td>1%</td>
<td>—</td>
</tr>
<tr>
<td>[206]</td>
<td>Al$_2$O$_3$/GeO$_2$/W</td>
<td>1.2 $\times$ 1.2 µm$^2$</td>
<td>=0.1 nA</td>
<td>14.3%</td>
<td>39.4%</td>
</tr>
<tr>
<td>[207]</td>
<td>Ag/CZTSe/Mo</td>
<td>Ø 500 µm</td>
<td>=0.3 mA</td>
<td>2.5%</td>
<td>—</td>
</tr>
<tr>
<td>[208]</td>
<td>Pt/Cu$^{3+}$/DNA/FTO</td>
<td>Ø 100 µm</td>
<td>=0.1 µA</td>
<td>22.5%</td>
<td>24.2%</td>
</tr>
<tr>
<td>[209]</td>
<td>Ni/Ti/Al$_2$O$_3$/SiO$_2$/p+ Si</td>
<td>—</td>
<td>=1 µA</td>
<td>29%</td>
<td>20%</td>
</tr>
<tr>
<td>[210]</td>
<td>Pt/VOx/Pt</td>
<td>—</td>
<td>10 mA</td>
<td>&lt;5%</td>
<td>—</td>
</tr>
<tr>
<td>[211]</td>
<td>ITO/Eu$_2$O$_3$/ITO/PET</td>
<td>50 $\times$ 50 µm$^2$</td>
<td>=10 µA</td>
<td>1.44%</td>
<td>1.68%</td>
</tr>
<tr>
<td>[212]</td>
<td>Pt/Ti/N-doped HfO$_2$/Pt</td>
<td>100 $\times$ 100 µm$^2$</td>
<td>=2 µA</td>
<td>7%</td>
<td>6%</td>
</tr>
<tr>
<td>[213]</td>
<td>TiN/SiO$_2$/FeO$_x$/FePt</td>
<td>Ø 100 µm</td>
<td>=10 µA</td>
<td>8.38%</td>
<td>10.03%</td>
</tr>
<tr>
<td>[214]</td>
<td>TiN/Al:HfO$_2$/Pt</td>
<td>100 $\times$ 100 µm$^2$</td>
<td>=5 µA</td>
<td>19.2%</td>
<td>—</td>
</tr>
<tr>
<td>[215]</td>
<td>PET/ITO/HZO/Ag</td>
<td>100 $\times$ 100 µm$^2$</td>
<td>=0.3 µA</td>
<td>25%</td>
<td>43%</td>
</tr>
<tr>
<td>[217]</td>
<td>Pt/ZnO/Pt</td>
<td>Ø 50 µm</td>
<td>=10 µA</td>
<td>5.0%</td>
<td>9.0%</td>
</tr>
<tr>
<td>[68]</td>
<td>Au/15-18-layer CVD hBN/Au</td>
<td>3 $\times$ 3 µm$^2$</td>
<td>0.2 pA–1 nA</td>
<td>2.02%</td>
<td>9.61%</td>
</tr>
</tbody>
</table>

Table 3. Device-to-device variability of RS devices. $C_v$ for $V_{\text{SET}}$ and $V_{\text{RESET}}$ of RS devices (made of any material) from one cycle to another. Variability increases with number of cycles and devices. “—” means “not mentioned.” Size of cells and current in LRS are also indicated, to evaluate how competitive the devices are in terms of integration density and energy consumption. Many studies on metal/MO/metal RS devices quantified the cycle-to-cycle variability of $V_{\text{SET}}$ and $V_{\text{RESET}}$, but for metal/LMs/metal RS devices such analysis is often ignored.

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Device structure</th>
<th>Device size</th>
<th># cycles/# devices</th>
<th>$I_{\text{LRS}}$ [at 0.1 V]</th>
<th>$C_v$ [$V_{\text{SET}}$]</th>
<th>$C_v$ [$V_{\text{RESET}}$]</th>
</tr>
</thead>
<tbody>
<tr>
<td>[211]</td>
<td>ITO/Eu$_2$O$_3$/ITO/PET</td>
<td>50 $\times$ 50 µm$^2$</td>
<td>3000 cycles</td>
<td>=10 µA</td>
<td>1.44%</td>
<td>1.68%</td>
</tr>
<tr>
<td>[218]</td>
<td>Pt/TiO$_2$/TiO$_2$/W</td>
<td>250 $\times$ 250 nm$^2$</td>
<td>—/50 devices</td>
<td>=0.2 µA</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>[219]</td>
<td>TiN/MoO$_3$/Pt</td>
<td>Ø 120 µm</td>
<td>—/50 devices</td>
<td>=80 µA</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>[220]</td>
<td>TiN/TiO$_2$/Al$_2$O$_3$/IrO$_x$</td>
<td>—</td>
<td>5000 cycles/5 devices</td>
<td>=100 nA</td>
<td>8%</td>
<td>—</td>
</tr>
<tr>
<td>[221]</td>
<td>Ti/W/Al$_2$O$_3$/Ta$_2$O$_5$/Pt</td>
<td>9 µm$^2$</td>
<td>—</td>
<td>=50 nA</td>
<td>19.2%</td>
<td>30.2%</td>
</tr>
<tr>
<td>[222]</td>
<td>Pt/Cu/Al$_2$O$_3$/Al$_2$O$_3$/Pt</td>
<td>Ø 30 µm</td>
<td>—/50 devices</td>
<td>=10 nA</td>
<td>6.2%</td>
<td>9.5%</td>
</tr>
<tr>
<td>[223]</td>
<td>Pt/Al$_2$O$_3$/TiO$_2$/Pt</td>
<td>200 $\times$ 200 nm$^2$</td>
<td>—/400 devices</td>
<td>=1 µA</td>
<td>=13%</td>
<td>=11.5%</td>
</tr>
<tr>
<td>[224]</td>
<td>Pt/TiN/TiO$_2$/Al$_2$O$_3$/Pt</td>
<td>350 $\times$ 350 nm$^2$</td>
<td>—/100 devices</td>
<td>=1 µA</td>
<td>16%</td>
<td>24%</td>
</tr>
<tr>
<td>[216]</td>
<td>Ti/Pr/([Ru(L)$_2$)$_3$]/Au NPs/ITO</td>
<td>60 nm$^2$ (nanodot)</td>
<td>50 cycles/5 devices</td>
<td>=1 nA</td>
<td>=10%</td>
<td>=5%</td>
</tr>
<tr>
<td>[225]</td>
<td>TiN/Al/Ti/Al$_2$O$_3$/TiO$_2$/Al/Ti</td>
<td>250 $\times$ 250 nm$^2$</td>
<td>—/4051 devices</td>
<td>=0.3 µA</td>
<td>26%</td>
<td>27%</td>
</tr>
<tr>
<td>[68]</td>
<td>Au/15-18-layer CVD hBN/Au</td>
<td>3 $\times$ 3 µm$^2$</td>
<td>750 cycles/48 devices</td>
<td>0.2 Pa–1 nA</td>
<td>6.06%</td>
<td>29.07%</td>
</tr>
</tbody>
</table>
varieties similar to cycle-to-cycle ones ($V_{SET}$ = 1.44% and $V_{VSET}$ = 1.68%). The area of the devices in ref. [186] was 50 $\mu$m $\times$ 50 $\mu$m, too large to meet the integration density requirements of memristive technologies (<100 nm$^2$).[3] For <1 $\mu$m$^2$, the device-to-device variability increases,[216] and the best performances as of 2022 are $\approx$10%[206] and 5%.[216]

Refs. [169,226] reported 25 devices (each) using 16 nm RGO and 15 nm GO, prepared by LPE, as dielectric (respectively), and claimed similar yields $\approx$72% and 80%. The yield of Au/Ti/15–18L-CVD-hBN/Ni RS devices with different sizes was discussed in ref. [158]. When the area decreased from 100 $\times$ 100 to 25 $\times$ 25 $\mu$m$^2$, the yield increased from 10% to 60%, probably due to a lower amount of defects under the top electrodes (e.g., less defective GBs of CVD-grown hBN between electrodes). Therefore, scaling down may be one effective approach to increase yield. This was verified in ref. [68], for devices down to 5 $\times$ 5 $\mu$m$^2$, leading to an increase of yield up to 98%, not reported in other LM-based crossbar arrays.[91,158,168,169,226,227] Ref. [68] also showed low device-to-device variability ($V_{SET}$ = 5.74%) and cycle-to-cycle variability ($V_{SET}$ = 1.53%), close to the best performances of MO-based RS devices.[205] Ref. [163] indicated that, when up to 25% of the surface of a 5 $\times$ 5 $\mu$m$^2$ Au/15–18L-CVD-hBN/Au device is covered by wrinkles and/or polymer transfer residuals, the electrical characteristics of the device is unaltered. Ref. [163] also found that the presence of overshoot currents across the device during forming or reset events is one of the main reasons reducing the yield in Au/15–18L-CVD-hBN/Au devices with lateral size of 320 nm $\times$ 420 nm. Wafer-scale transfer is still challenging for LMs-based RS devices.

5. Access to the MIM Cells and Sneak Path Currents

So far, very few studies constructed crossbar arrays of MIM-like memristors using LMs. Table 4 summarizes the performance of LMs-based crossbar arrays of RS devices. Ref. [163] reported a crossbar with 10,000 devices (100 $\times$ 100) with small size (0.1344 $\mu$m$^2$).[163] but only tested 11 devices. Refs. [65,228] claimed very high endurances (>10 million cycles) in small crossbar arrays (<36 devices/crossbar) of Ti/Pt-LPE MoS$_2$/Ti/ Pt (size > 25 $\mu$m$^2$ per device) and SLG/MC MoS$_2$/O$_x$/SLG (size > 25 $\mu$m$^2$ per device). However, the endurance plot only showed 22 and 73, datapoints. Thus, a demonstration in all cycles in multiple devices (as that recommended in refs. [5,202] and carried out in ref. [68]) is necessary.

In crossbar arrays of RS devices, electrical stimuli can be applied to each MIM cell selecting one row and one column.[1] However, using this approach, the surrounding MIM cells are also exposed to part of the electrical stress, which creates additional paths for current flow from one electrode to another (often called sneak paths or sneak currents).[43] In order to minimize this, one common solution is to include additional elements adjacent to each MIM-like RS device in the crossbar array, such as transistors[44,45] (leading to ITIR configurations[46]) or selectors (leading to 1S1R configurations[45]). Ref. [44] fabricated ITIR structures using LMs, i.e., a transistor made of WO$_3$ on and 4L-MC-WSe$_2$ connected in series to a RS device with Ag/$\approx$400 nm-printed WSe$_2$/Ag.

Ref. [191] integrated CVD-1L-MoS$_2$ FETs with HFO$_x$-based RS devices to form a ternary content addressable memory, that allows high speed information search thanks to its ability to ignore data bits.[222] Due to the ultralow leakage current in 1L-MoS$_2$ FETs $\approx$1–2 fA $\mu$m$^{-1}$,[191,233] ref. [191] claimed that the sneak paths could be cut off, while maintaining a large resistance ratio (up to 8.5 $\times$ 10$^5$), although the sneak path current was not characterized. In ref. [190] the set voltage of RS devices in ITIR cells was $<1$ V, achieved by replacing the HFO$_x$-based RS devices with forming-free 10–13L-CVD-hBN-based ones, Figures 11a–c. Similar to ref. [191], the ITIR cells fabricated by transferring 1L-CVD-MoS$_2$ and 10–13L-CVD-hBN in ref. [190] showed low sneak currents ($\approx$1 pA $\mu$m$^{-2}$). Although 1L-MoS$_2$ FETs can reduce the sneak currents between RS devices, ITIR require good matching between switching voltages and currents driven by transistor and RS device,[234] which increases cell size,[235] thus reducing integration density.

Ref. [46] fabricated a 12 $\times$ 12 crossbar array of 1S1R cells with vertical Au/h-BN/Gr/h-BN/Ag devices. By using EBL and three transfer steps, ref. [46] fitted the 144 devices within $\approx$225 $\mu$m$^2$ (i.e., the overlapped area of the 3 MC-flakes, see Figure 11d).
Ref. [46] also investigated the sneak path currents using V/2 and V/3 schemes. Figure 11e,f, reported current across unselected cells <10 fA (very low, meeting the technological specifications for both non-volatile memories and electronic synapses/neurons[4–6,63]), even without a series transistor. However, the working mechanism proposed in ref. [46] is questionable, because MC-ML-hBN does not exhibit stable bipolar RS,[131,236] and the TEM images reveal amorphous material (probably polymer residuals from the transfer) embedded between MC-ML-hBN and MC-MLG (which may generate RS).[236,237] Therefore, it is probable that the RS is induced by defects in MLG, not due to the MC-ML-hBN. Ref. [46] analyzed sneak path currents in LM-based crossbars. Similar studies should be done for LPE/CVD/MOCVD samples.

6. Circuit-Level Applications

Vertical MIM cells exhibiting RS were used to fabricate electronic circuits, including logic gates, non-volatile memories, electronic synapses, and neurons.[59] Multiple logic operations, including NOR,[238] AND,[238,239] and NAND gates,[238] as well as material implication (a binary truth functional operator that returns "true" unless its first argument is true and its second argument is false),[240–242] have been realized. Their main advantages compared to their counterparts made of CMOS transistors are easier fabrication, potential for 3d integration, reduced size,[238,248] and lower power consumption.[243] 3d-hybrid CMOS/RS field programmable gate array (FPGA) architectures showed a six-times-higher integration density[242] and ≈16.7% lower standby power consumption than static random-access memories with ITIR arrays.[243,244] Large-scale (up to 1600 cells) hybrid CMOS/RS-device circuits[245–247] were demonstrated with a storage capacity of 16GB.[248] Standalone CMOS/RS-device-based memories require more efforts because of the sneak path currents.[249] Refs. [216,220–225] prepared RS-devices designed to exhibit multiple resistive states, and nearly analogue RS was used to emulate ANNs[250–255] and spiking neural networks,[256,257] for image classification,[251–255] and to encode neuronal spiking activities by compressing the spike amplitude and firing rate.[256] Most works[253,254,256] characterized one/few devices applying I–V curves or pulsed voltage stresses (PVS), and used conductance as weight of the electronic synapses in simulated ANNs (using TensorFlow,[258] PyTorch,[259] and Python[260]). Thus, refs. [253,254,256] did not fabricate an ANN, but only simulated what would be the classification accuracy of a system exhibiting such RS performance. Refs. [252,255,261–263] faced the hardware implementation of an ANN, but many challenges remain, such as reducing resistance level instability,[253,254] sneak path currents,[251] device-to-device[252,253] and cycle-to-cycle variabilities,[254,261,264] and implementation of extreme machine learning algorithms.[265]

When using LM-based RS devices, the number of circuit-level demonstrations is much scarcer. Ref. [266] presented an array of dot-like devices made of Zn/tetrakis(4-carboxyphenyl)porphyrin, and used it to store different digits, matching the
letters “S” and “Z,” in the form of resistive states, and this pattern was stable for >5000 s. LPE was used in ref. [266] to fabricate crossbar arrays of RS devices, to store information generated by a near-infrared emission system. Using LPE, ref. [133] fabricated (on 4″ wafers) crossbar arrays of Al/7.5 nm LPE-MoS2–MoOx/Al devices connected to pressure sensors and light emitting diodes, to store information in the form of mechanical impulses, and display it as light. Refs. [97,266–268] employed the word “programming” to refer to the operation they carried out, but all they did is store data. This may be misleading, because “programming” denotes data processing and/or computation,[269] not carried out in refs. [97,266–268].

Ref. [267] presented simple computations using crossbar arrays of Ag/POx/33L-MC black phosphorus/Au devices with lateral sizes ≈100 nm × 100 nm to build OR and AND logic gates. Ref. [190] fabricated a 2 × 2 crossbar array of ITTIR cells using IL-CVD MoS2 transistors and Au/Ti/hBN/Au RS devices, and claimed it could be used to implement matrix vector multiplication. Figures 12a–c, but an experimental demonstration was not presented. The use of LM-based RS devices to emulate ANNs was also explored.[93–95,178] Refs. [93–95,175] fabricated isolated RS devices with dot-like[93,175] or cross-point structure[94,95] using LPE or CVD. They measured one[93–95]/few[175] devices, and used the data to emulate a NN, using software.[258–260] This was also realized using planar RS devices,[270] and is even less competitive from an integration point of view, due to the larger lateral size and complex 3d integration. As of 2022, the only emulations of ANNs using data collected in LM-based RS devices fabricated using LPE or CVD and integrated in a crossbar network are in ref. [68]. This fabricated crossbar arrays of Au/15–18L-hBN/Au, and used them to build a multilayer perceptron (a basic type of ANN) with >98% accuracy in image recognition from the Modified National Institute of Standards and Technology (MNIST[271]) dataset, Figures 12d,e.

Ref. [68] also simulated the disturbance (i.e., intentional change of conductance) of half-selected cells (see Figure 11e) within the crossbar array of MIM-like RS cells, and confirmed this to be <10%, Figures 12f,g.

7. Challenges and Prospects

The main challenges of LMs-based RS devices are endurance, variability, and yield. Refs. [228,272–274] claimed high endurance (>10⁶ cycles) in RS devices using CVD-1LG as impermeable blocking layer,[272,273] ≈10-nm-thick MoS2-based RS devices produced by LPE,[228] and CVD-1L-hBN.[274] However, refs. [228,272–274] only recorded one single data point per decade in one single device, instead of one data point per cycle per state for a few (≈5) devices,[275] which is a reliable method to evaluate endurance.[202] The RS phenomenon requires one material between the electrodes that can block the current in

![Figure 12. RS crossbar arrays for neuromorphic applications. a) Schematic two-level stacked 2 × 2 back-gated 1T1R array with Au/Ti/10–13L-hBN/Au RS devices and 1L-CVD-MoS2 transistors. b) Schematic 2 × 2 back-gated 1T1R, indicating how matrix-vector multiplication is carried out. c) Normalized resistance changes with pulse number for set and rest processes in RS device and 1T1R cells with same pulse conditions, showing 1T1R cells have better linearity and a higher resistance window. a–c) Reproduced with permission.[190] Copyright 2018, IEEE. d) Simulations for ex situ trained ANNs showing adverse influence of increase of linear dimensions of the crossbar on half-select disturbance and classification accuracy. e) Device conductance statistics for a 64 × 64 crossbar array after modifying the accuracy in tuning algorithm to 1%. f) Relative conductance change versus VSET with multiplicative factor α. g) Normalized conductance after applying set/reset pulses for 100 devices randomly chosen from a 64 × 64 crossbar array. d–g) Reproduced with permission.[68] Copyright 2020, The Authors, published by Springer Nature.](https://www.advancedsciencenews.com/doi/10.1002/adma.202101409)
HRS, meaning that insulators (band gap >5 eV, like hBN) are preferred. However, its structure needs to be modified in a reversible manner to reach LRS. As defect-free hBN has hard bonds difficult to break (minimum energy for atomic migration >10 eV[286]), it requires the application of high energy that results in permanent damage.[133] For this reason, defect-rich CVD-hBN shows one of the best performance at the device level.[68,131,163,168] although semiconductors like MoS 2[65,228] also revealed competitive properties (see Table 4). Variability was rarely discussed.[88] Ref. 163 discussed yield-pass criteria;[161] however, these may be different to those used by companies, since these do not disclose information about the criteria they use. Clear guidelines are needed, similar to those for solar cells[276] or lasers,[277,278] requiring the publication of all necessary figures of merit.

Many RS observations were made in MIM-like devices that are very large (>100 μm 2).[113,207,222,238] The fact that one such device shows reliable RS does not mean that this will behave the same for a size <100 nm 2,[279] required in most RS technologies.[6]

Insulators without vacancies, interstitial atoms, or impurities, do not exhibit RS.[280] The reason is that in such materials the energy required to form the CNF (i.e., dielectric breakdown) is higher than in materials containing vacancies,[28] and results in an irreversible phenomenon (no reset after breakdown[110]). That is why, in most cases,[56,27] the current during the CNF formation must be limited. However, even with that, if the intrinsic concentration of native defects is very low (e.g., ≈10 19 cm −2 for the field oxide charge density in SiO 2 grown by thermal oxidation with an annealing at 500 °C[286]), an electric field will result in irreversible atomic rearrangements. For example: 1) SiO 2 grown by thermal oxidation of Si has no vacancies nor impurities, but no RS.[280] Only when SiO 2 is produced by other deposition methods that result in a higher density of dangling bonds (e.g., by sputtering[282]), it displays RS.[283] 2) The MC-64L-MoS 2 in ref.[65] only showed RS after exposure to an oxidative treatment to introduce O impurities. 3) hBN flakes prepared by MC do not show RS,[212] while CVD-grown ones were reported with excellent RS.[68,131,133] e.g., yield >98%,[68] CV of V SET <1.53%,[68] and I hRS/I LRS >10 11,[68] 4) High-k dielectrics like HfO 2 and TaO x exhibit much better RS than thermal SiO 2, as they host a larger amount of defects.[111,115] 5) HfO 2 samples grown by atomic layer deposition only show RS when they are subjected to thermal annealing >400 °C.[284,285] This induces poly-crystallization and generates defects at GBs, the only sites that promote RS.[286,287] However, if materials contain too many defects, this can ease the lateral propagation of CNFs,[286] and result in erratic RS for few (~5) cycles,[289] or poor endurance[66,289] (<100 cycles).

Therefore, LMs for RS should contain vacancies, interstitial atoms, and impurities, but not too many (i.e., the layered structure should be maintained and defects should be embedded). The density of defects needed to induce stable RS over millions of cycles has not been quantified for any material. Not all defects are similar. Some are clusters,[285] as the probability to form a defect in the vicinity of another is larger than when there are no other defects nearby.[290]

In MIM-like devices with large lateral size (e.g., >10 5 μm 2), the probability to find more and larger defects in the insulator increases. Ultrasmall (<100 nm 2) devices may not include enough defects to enable RS. For example, for the metal/poly-crystalline HfO 2/metals systems in ref.[285], with lateral sizes ≈10 μm 2, devices exhibited bipolar RS, but when the lateral size was ~50 nm 2, only ~15% exhibited RS. It may be that devices with large lateral size (>10 5 μm 2) host too many defects that results in erratic RS,[292] while smaller ones (25 μm 2) do not host such defects and show better RS.[293]

Therefore, in LMs for RS technologies it is important to ensure small (<10 nm) inter-defect distances while maintaining a high ratio between the non-destructive volume (V ND) and the defective volume (V D), i.e., V ND/V D ≥5,[16] not only to provide the devices with the properties of LMs (i.e., high flexibility, mechanical strength, and in-plane thermal conductivity) but also to avoid unwanted lateral expansion of CNFs toward irreversible dielectric breakdown.

CVD-grown LMs are normally polycrystalline, with grains ranging from 5 μm[179] to 1 mm.[293] GBs contain atomic defects.[294,295] Single-crystal 1L-LM can be grown at wafer scale.[144,293] Although RS devices with 1L-LMs were demonstrated,[36,296] pinholes and cracking during transfer (compared to >10L-LMs) result in a lower yield (e.g., 50% for 1L-hBN[27] vs >98% for >1L-hBN[68]), as even one missing atom can short RS devices, because the current flows out of plane (this is different when the current flows in-plane,[360] in which case one missing atom does not produce device failure). Controlling grain size and defects in LMs with thicknesses suitable for RS (i.e., between ~2 and 30 nm) is challenging. Therefore, large (>10 3 μm 2) devices made of CVD-LMs containing GBs, Figure 1a, might exhibit excellent RS with low device-to-device variability of the electrical performance (because the relative difference of V D from one device to another is low) and high yield. On the contrary, small devices (<300 nm 2) made of CVD-LMs without local defects (Figure 1b) may not show RS, or exhibit erratic RS with very high device-to-device variability (because the relative difference of V D from one device to another is high) and low yield. Figure 13a,b indicates that yield and device-to-device variability of large and small devices can be different.

In LPE-LMs RS devices, the flakes have diameters ranging from 0.2[45] to >100 μm,[118] and form junctions that contain large amounts of defects, Figures 4b and 13c.d. Similar to GBs in CVD-LMs, these defective junctions can promote out-of-plane leakage current, which could alter the RS characteristics, e.g., in ref.[298], hBN-poly(vinyl alcohol) (PVOH) RS devices fabricated by LPE showed 4 ×10 −9 A for areas 1.4×10 3 μm 2 and 7×10 −7 A for ~78×10 3 μm 2. Thus, we recommend fabricating RS devices with areas as small as possible.

Large (>10 3 μm 2) dot-like device structures patterned using a shadow mask, Figure 13e–h, used in most cases because they are the simplest to fabricate,[5] should be avoided. In large (>10 5 μm 2) devices the RS active area is exposed to the pressure exerted by the tip of the probe station,[299] which may lead to higher post-DB currents, lower DB voltages, lower variability of post-DB currents (i.e., R LRS), and erratic bipolar RS cycling. As in real chips, RS devices are not exposed to the pressure of probe station tips, and this structure (Figure 13e–h) should be avoided. Ref.[115] reported a RS analysis in small MO-based devices ~10 nm ×10 nm, fabricated in an industrial facility. Ref.[300] prepared 2 nm ×2 nm MO-based RS prototypes in a university lab, but the variability of V SET was significant. We recommend the study of RS devices with sizes down to 10 nm ×10 nm, although this may be challenging. Focusing on
devices with lateral sizes >5 µm is risky because this is similar to the grain size in CVD ML-LMs, or the flake size in LPE-LMs, and GB defects in CVD-ML-LMs, or nanojunctions in LPE-LMs, and may influence the devices electrical characteristics.

For devices with small (<100 nm²) sizes, the current densities flowing in LRS could melt the metallic wires. For this reason, we recommend to make them thick enough (>50 nm), and employ metals that are resistant to electromigration (e.g., Pt[301] and W[302]).
or, possibly, 1LG. Isolated cross-point RS devices are not exposed to the disturbance in crossbar arrays. Therefore, crossbar structures are preferred as they match the requirements of industrial chips.

Before introducing one MIM-like structure in an industrial RS technology, this must be tested over millions of cycles in thousands of devices, with all parameters (\(V\_{\text{SET}}, \ V\_{\text{RESET}}, \ t\_{\text{SET}}, \ t\_{\text{RESET}}, \ E\_{\text{SET}}, \ E\_{\text{RESET}}, \ t\_{\text{HRS}}, \ t\_{\text{LRS}}\)) falling within the acceptable operation windows. The exact value of each parameter, the variability of the operation windows, and the percentage of devices that must fit this requirement are different for each RS technology, and each manufacturer may also use different criteria. While presenting such data is common in industrial reports, it is also important to define what the acceptable operation windows for each device parameter are, and to disclose how many devices were measured and how many worked well, so that the yield can be calculated. We emphasize that, for any device parameter, claiming the measurement of many (>100) cycles and showing data corresponding to one/few cycle/s per decade, as in references [38,93,94,97,144], is not acceptable.\(^5\) RS must be characterized in every cycle, and otherwise one cannot ensure that the device has switched. Misleading characterization approaches (i.e., claiming operation >10\(^7\) cycles while showing data for one/few cycles per decade) were employed.\(^6\)\(^5\)\(^7\)\(^4\)\(^3\)\(^2\)\(^1\) Table 5 summarizes the structure and properties of LMs-based RS devices characterized in all cycles.\(^{68,91,92,100–102,158,169,181,226,227,303–305}\)

8. Conclusions

Most RS technologies (i.e., NVM and ANN) use the crossbar array architecture due to its high integration density, therefore, RS studies employing LMs (and other novel materials) should use it too. Producing LMs using scalable methods (i.e., LPE, CVD, and MOCVD) is important for industrial applications. By analyzing the literature on crossbar arrays of RS devices fabricated using scalable methods, we concluded that LMs can provide performances not achieved with traditional materials (i.e., phase-change, metal oxide, and magnetic), such as high transparency up to 97.4%, stable \(I\_{\text{LRS}}/I\_{\text{HRS}} > 10^5\) for 10\(^4\) s

Table 5. Endurance of LM-based RS devices. Comparison of endurance of LM-based RS devices. Only those works that characterized the resistance in each cycle, even via \(I-V\) sweeps or current-visible PVS, are considered, because, according to ref. [5], the endurance should be calculated in each cycle, especially when studying prototype RS devices made of novel materials. NASE = nanoimprint-assisted shear exfoliation.\(^27\) The endurance of metal/LMs/metal devices is still far behind than that of metal/MO/metal ones, which have surpassed 10\(^9\) cycles in multiple studies that use the \(V\_{\text{RS}}\) technology, this must be tested over millions of cycles in

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Structure</th>
<th>Device size</th>
<th>Yield</th>
<th># Cycles</th>
<th>Test method</th>
<th>Switching type</th>
</tr>
</thead>
<tbody>
<tr>
<td>[92]</td>
<td>Au/CVD-1L-hBN/Au</td>
<td>1 x 1 (\mu)m(^2)</td>
<td>—</td>
<td>50</td>
<td>IV curves</td>
<td>Bipolar</td>
</tr>
<tr>
<td>[183]</td>
<td>Ti/CVD-2L-hBN/Au</td>
<td>100 x 100 (\mu)m(^2)</td>
<td>—</td>
<td>400</td>
<td>IV curves</td>
<td>Bipolar</td>
</tr>
<tr>
<td>[303]</td>
<td>Au/CVD-1L-MoS(_2)/Au</td>
<td>Planar FET channel length (2 (\mu)m)</td>
<td>—</td>
<td>15</td>
<td>IV curves</td>
<td>Bipolar</td>
</tr>
<tr>
<td>[304]</td>
<td>Au/CVD-1L-MoS(_2)/Au</td>
<td>Planar FET channel length (1–5 (\mu)m)</td>
<td>—</td>
<td>475</td>
<td>IV curves</td>
<td>Bipolar</td>
</tr>
<tr>
<td>[100]</td>
<td>Au/MC-3–80nm-Li,MoS(_2)/Au</td>
<td>Planar FET channel length (&gt;50 (\mu)m)</td>
<td>—</td>
<td>1000</td>
<td>PVS</td>
<td>Bipolar</td>
</tr>
<tr>
<td>[37]</td>
<td>Au/CVD-1L-MoS(_2)/Au</td>
<td>2 x 2 (\mu)m(^2)</td>
<td>—</td>
<td>150</td>
<td>IV curves</td>
<td>Bipolar</td>
</tr>
<tr>
<td>[102]</td>
<td>Ag/MC = 8 nm GaSe/Ag</td>
<td>Planar FET channel length (&gt;30 (\mu)m)</td>
<td>—</td>
<td>5000</td>
<td>IV curves</td>
<td>Bipolar</td>
</tr>
<tr>
<td>[102]</td>
<td>Au/Ti/10–15 nm NASE MoS(_2)/Ti/Au</td>
<td>Planar FET channel length (&gt;2 (\mu)m)</td>
<td>—</td>
<td>6</td>
<td>PVS</td>
<td>Bipolar</td>
</tr>
<tr>
<td>[104]</td>
<td>Au/MC = 95 nm-(\alpha)-InSe(_2)/Au</td>
<td>Planar FET channel length (&gt;1 (\mu)m)</td>
<td>—</td>
<td>100</td>
<td>IV curves</td>
<td>Bipolar</td>
</tr>
<tr>
<td>[91]</td>
<td>Cu/CVD-2L-MoS(_2)/Au</td>
<td>2 x 2 (\mu)m(^2)</td>
<td>—</td>
<td>20</td>
<td>PVS</td>
<td>Bipolar</td>
</tr>
<tr>
<td>[168]</td>
<td>Au/CVD-1L-Mo(_5)S(_3)/Au</td>
<td>0.5 x 0.5 (\mu)m(^2)</td>
<td>50% (18/36)</td>
<td>—</td>
<td>IV curves</td>
<td>Bipolar</td>
</tr>
<tr>
<td>[169]</td>
<td>Pt/LPE = 16 nm-bilayer-reduced GO/Pt</td>
<td>60 x 60 (\mu)m(^2)</td>
<td>72% (18/25)</td>
<td>1</td>
<td>IV curves</td>
<td>Bipolar</td>
</tr>
<tr>
<td>[236]</td>
<td>Al/LPE = 15nm-GO/Al/PES</td>
<td>50 x 50 (\mu)m(^2)</td>
<td>80% (20/25)</td>
<td>100</td>
<td>IV curves</td>
<td>Bipolar</td>
</tr>
<tr>
<td>[227]</td>
<td>Ag/ZnO/sputtered 120nm-W(_5)S(_3)/Al</td>
<td>—</td>
<td>83.3% (15/18)</td>
<td>—</td>
<td>PVS</td>
<td>Bipolar</td>
</tr>
<tr>
<td>[158]</td>
<td>Au/Ti/CVD-10–12L-hBN/Ni</td>
<td>25 x 25 (\mu)m(^2)</td>
<td>60% (9/15)</td>
<td>100</td>
<td>IV curves</td>
<td>Bipolar</td>
</tr>
<tr>
<td>[168]</td>
<td>Au/CVD-1L-Mo(_5)S(_3)/Au</td>
<td>2 x 2 (\mu)m(^2)</td>
<td>—</td>
<td>100</td>
<td>PVS</td>
<td>Bipolar</td>
</tr>
<tr>
<td>[68]</td>
<td>Ag/CVD-15–18L-hBN/Au</td>
<td>150 x 150 (\mu)m(^2)</td>
<td>98% (47/48)</td>
<td>80000</td>
<td>PVS</td>
<td>Threshold</td>
</tr>
</tbody>
</table>

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for $10^4$ bending cycles down to 4.2 mm radius of curvature, threshold RS with ultralow energy consumption per transition ($\approx 8.8 \times 10^{-12}$), variability of the relaxation time $\approx 8.52\%$, and coexistence of bipolar and threshold RS that enables the implementation of STP and LTP in the same device. Other properties, such as thermal stability up to $\approx 300^\circ C$ should be further confirmed statistically. High yield up to 98%, low variability ($\approx 8.8\%$) for $>100$ devices, and low sneak path currents $<10\,\text{fA}$ have been achieved. RS devices made of LMs were used in logic gates, and ITRI cells. Studies on crossbar arrays of RS devices should aim for smaller areas (ideally $<10\,\text{nm} \times 10\,\text{nm}$ but, as that may be too challenging for most academics, here we propose $<100\,\text{nm} \times 100\,\text{nm}$, which is achievable via EBL$^{[68]}$) and provide yield and variability information of the main parameters ($R_{\text{HRS}}, R_{\text{LRS}}, V_{\text{SET}}, V_{\text{RESET}}, t_{\text{SET}}, t_{\text{RESET}}, E_{\text{SET}}, E_{\text{RESET}}$; retention time). Larger crossbar array sizes ($>10\,\text{kbit}$) and hardware-enabled computational operations (i.e., vector matrix multiplication) should be used, not just simulations.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

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