Gigahertz Multi-Transistor Graphene Integrated Circuits

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Abstract

We review the potential of graphene in ultra-high speed circuits. To date, most of high-frequency graphene circuits typically consist of a single transistor integrated with a few passive components. The development of multi-transistor graphene integrated circuits operating at GHz frequencies can pave the way for applications in which high operating speed is traded off against power consumption and circuit complexity. Novel vertical and planar devices based on a combination of graphene and layered materials could broaden the scope and performances of future devices.

Introduction

Graphene has been in the spotlight of the electron device community since the development of the first back-gated few-layer graphene field-effect transistors (FETs) (1). Graphene has a unique combination of electrical and mechanical properties that make it attractive to complement conventional semiconductors. High mobility (2,3,4) and a saturation velocity much larger than any semiconductor (5,6) have already allowed realization of graphene FETs (GFETs) with cut-off frequencies ~ 350 GHz (7). Being only one atom thick, graphene has a potential to overcome state-of-the-art Si and III-V semiconductors in high-frequency transistors at the ultimate scaling limits (8). Unlike other materials, electrons and holes have the similar mobility, much greater than InP, which currently dominates high-speed electronics (9). High-frequency FETs are also expected to benefit from the mechanical and chemical stability of graphene, as well as its high thermal conductivity (10). Graphene circuits can also be used on transparent and flexible substrates (11,12), inaccessible for conventional semiconductors, allowing new concepts in mobile communications (13).

The absence of a bandgap is a major hurdle in the development of realistic circuits, since this gives a non-zero off state drain current, which leads to considerable static power dissipation. The typical static drain current in graphene inverters (14) is ~270 μA/μm at a supply voltage V_{DD} = 2.5 V, in contrast to the much smaller leakage drain current ~100 nA/μm at V_{DD} = 0.75 V in 22-nm node high-performance Si logic transistors (15). This hinders the use of graphene in highly-integrated low-power digital applications (such as Si CMOS). Graphene can still be used in digital or analog electronic circuits realized in medium to large scale integration technology (transistor count < 10^3) in order to keep chip power density at manageable levels (16). However, this potential has not yet been fulfilled, as the transistor count in typical graphene circuits is one (17), yet again due to the absence of a bandgap. GFETs must have intrinsic voltage gain $A = g_m/g_d>1$ in order to be useful in practical electronic applications, where g_m is the transconductance and g_d the output conductance. Only with $A > 1$ it is possible to realize circuit stages with ac voltage gain $|A_v| > 1$ (18). Cascading such stages, more realistic circuits can be formed without attenuating signal after each stage. However, the intrinsic voltage gain of GFETs is limited by the zero bandgap, which prevents depletion of carriers. This limits the gate voltage control over the drain current, i.e. it reduces g_m with respect to conventional semiconductor FETs, which can be turned off at suitable gate biases (19). Lack of depletion also leads to a weaker drain current saturation regime, which in turn increases g_d (18). Hence, most GFETs to date have intrinsic gain much smaller than unity (20-26) resulting in the inability to directly couple graphene electronic circuits.

Bandgap opening may solve the problems of large static power dissipation and low voltage gain. However, no satisfactory solution has been found so far to open a sufficiently large bandgap without reduction of mobility (11). Bandgap engineering is usually attempted by patterning into graphene nanoribbons (GNRs) (24,11), but GNRs tend to have low mobilities (<200 $cm^2V^{-1}s^{-1}$) (27) as a consequence of carrier scattering on disordered edges (28). To eliminate unwanted scattering, GNRs should have crystallographically smooth edges (28-32) and be deposited on insulating substrates (11). This leads to a fabrication challenge (11), as GNR widths ~1nm are required (33,34) in order to reach the bandgap of Si (~1 eV), necessary for reliable switching. Moreover, thus far, none of the methods for creating smooth GNRs (11) can yet produce a large number of GNRs at pre-defined locations on a chip, a necessary step for the fabrication of integrated circuits.

One technology currently capable of delivering graphene devices with over-unity voltage gain, relies on unconstricted graphene, in which mobility is not reduced by nano-patterning. Here we will discuss the development of graphene devices with $|A_v|>1$ and their integration in realistic high-frequency multi-stage electronic circuits.

Voltage gain in graphene devices

One of main factors which contributed to a low voltage gain in early large-area GFETs was use of back-gated Si/SiO_2.

Such FETs also suffer from large parasitic capacitances (because the gate overlaps with whole circuits rather than just with the transistor channels) and cannot be integrated with other components (because all devices share the same gate). For this reason, top-gated GFETs with thinner gate oxides have been investigated (35)-(42), since $g_m \sim t_{ox}^{-1}$ (43), where t_{ox} is the gate oxide thickens. They were fabricated from micromechanical cleavage (MC) of graphite (35-38), carbon segregation from metals, such as Ni (39), or SiC (41,42), or chemical vapor deposition (CVD) on Cu (40). SiO_x (35), AlO_x (37),(40),(42) and HfO_x (36),(38),(39),(41)have been used as top-gate dielectric.

The first graphene circuits with $|A_v|>1$ ($|A_v|\sim6$) were realized by utilizing ultra-thin AlO_x top-gate dielectrics (43,44). The gate stack was fabricated by evaporation of Al, followed by exposure to air. This naturally forms a very thin (<4nm) AlO_x at the interface between graphene and Al. These FETs, based on MC graphene, exhibited over-unity $|A_v|$ only at cryogenic temperatures [<100 K], as strong hysteresis in their transfer characteristics suppressed $|A_v|$ at room temperature (RT) (39). Hysteretic behavior of GFETs under ambient conditions stems from water charge traps adsorbed on the substrate (25,45,46), with detrimental impact on transconductance, therefore $|A_v|$.

The first $|A_v|>1$ under ambient conditions was obtained using a twisted bilayer graphene (BLG) as the active material, with a solid polymer electrolyte as gate dielectric (48). These devices had $|A_v|>1$ only in dc mode, as a consequence of a large overlap between polymer gate and source/drain contacts. The dc gain is of no interest in realistic electronic applications, as logic gates and voltage amplifiers operate in dynamic, ac mode. A RT ac $|A_v|>1$ was first demonstrated in a 6-finger-gate FET (49). Although the gain was relatively small ($|A_v| = 1.7$) and the fabricated amplifiers were not integrated (requiring external inductors and capacitors to operate), with promising bandwidth (6 GHz).

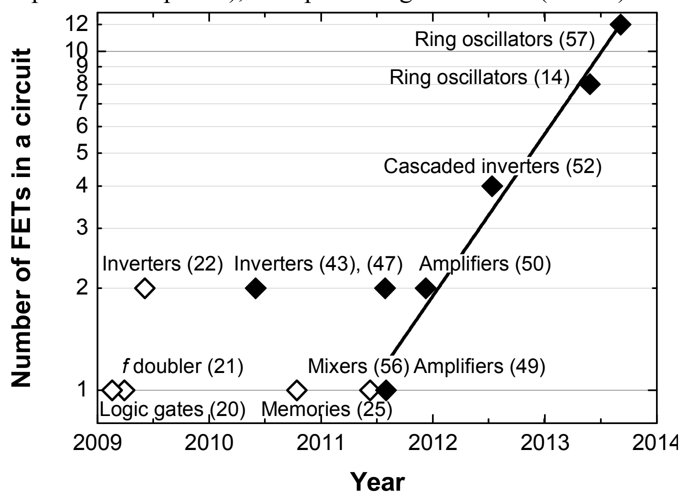

Figure 1: Transistor count in graphene circuits with $|A_v| < 1$ (open symbols) and $|A_v| > 1$ (filled symbols). The linear fit is performed only on circuits with over-unity RT ac $|Av|$. From this, a graphene Moore's law is obtained: the number of GFETs on a chip currently doubles approximately every 8 months. However, it is unlikely that this will hold in the near future.

The first integrated graphene voltage amplifiers exhibited $|A_v| = 3.7$ at RT (50). In contrast to standard GFETs in which there are ungated graphene channel regions on either side of the gate (51), these GFETs did not have ungated parts, due to a self-aligned fabrication process. This approach also screens the charge traps surrounding the channel and eliminates hysteresis in the transfer curves, which can be detrimental to the stability of devices operating at RT (44,47). Such blend of transistor properties combined with very thin gate insulators resulted in a voltage gain that can be utilized both in analog and digital electronics. However, these devices were fabricated from MC graphene, which is difficult to scale for mass production (11).

The self-aligned fabrication process was further extended to wafer-scale graphene. This resulted in the highest $|A_v|=5.3$ to date, for graphene integrated circuits in ambient conditions (46). This $|A_v|$ arises from the large intrinsic gain of the GFETs integrated into digital complementary inverters. These exhibited higher transconductance ($g_m\sim150$ μS/μm), comparable to that obtained in MC-GFETs deposited on MC-h-BN (53), even though MC is not a scalable technology (53,11). The obtained $|A_v|$ was large enough to realize integrated wafer-scale logic gates with digital signal matching under ambient conditions. This allowed cascading of digital graphene inverters (52), with the previous stage capable of triggering the next stage, the first demonstration of an integrated graphene multi-stage circuit.

The highest intrinsic voltage gain $A = 35$ in GFETs was reported in exfoliated AB-stacked BLG (54), where a small bandgap was opened under very large perpendicular electric fields. This improved drain current saturation and reduced the output conductance g_d.

Transistor count in graphene circuits

The development of graphene devices exhibiting over-unity $|A_v|$ is tightly connected to the development of graphene multi-stage (i.e. multi-transistor) circuits. The transistor count in some of the graphene circuits realized so far is shown in Figure 1. The first functional circuits comprised only one GFET (20,21). Their functionality was controlled by dc input biasing, depending on which different types of logic gates (20) or a frequency multiplier (21) were realized. Although these simple circuits demonstrated that graphene can be used to realize functionalities typically found in conventional electronic circuits, they suffered from several drawbacks. Both circuits were made from MC graphene and not integrated (they required external resistors to operate). The GFETs were back-gated, therefore the circuits exhibited a very small $|A_v|$, which resulted in a large attenuation of the output signal. This lead to the inability to directly couple digital logic gates (due to a mismatch between input and output voltage logic levels) or to amplify analog ac signals. Therefore the realized functionalities could not be used in realistic and more complex electronic systems.

The first attempt to increase the transistor count was

the realization of graphene complementary inverters comprised of two GFETs (22). This was the first time a complete functionality was integrated on a single MC graphene flake, and no additional components were required. This integrated circuit also established a simple concept of complementary operation between the Dirac points of the two GFETs connected in series. However, these inverters were also back-gated, therefore exhibited $|A_v|< 1$. The concept of complementary operation was later extended to top-gated inverters, exhibiting over-unity $|A_v|$ at cryogenic (33) and RT (50). However, their transistor count was also 2, and there was no attempt to demonstrate multi-stage circuits, probably because of the use of MC graphene.

The first graphene multi-stage circuit comprised two inverters connected in series, thus bringing the transistor count to 4 (52). The signal matching and cascading was demonstrated under ambient conditions, with inverters fabricated from CVD graphene (54).

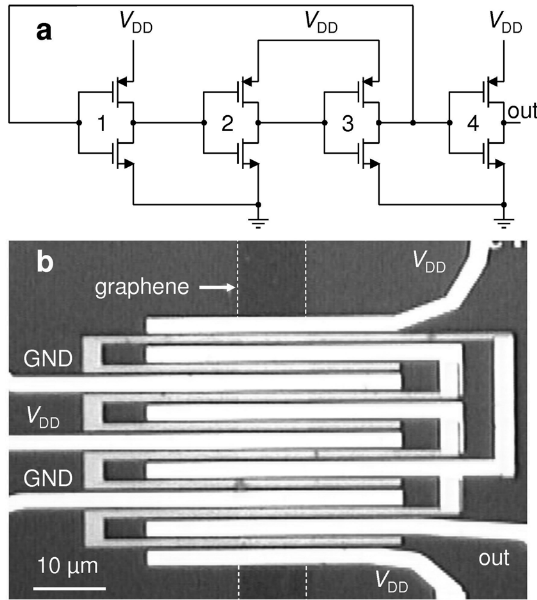

Figure 2: Integrated graphene ring oscillator (RO). (a) Circuit diagram of a three-stage RO. The RO comprises three inverters (1-3) cascaded in a loop with a fourth inverter (4) decoupling the RO from the measurement equipment connected to the output (out). (b) Optical microscope image of a RO with gate length L=1 µm integrated on CVD graphene channel. The drain contacts of inverters 1-3 (Au) overlap with the gate contacts (Al/Ti/Au) in order to form internal connections between the inverters.

The good $|A|_v$~5, crucial in achieving cascaded operation (52), was obtained due to a combination of factors including full-channel gating, thin (~4 nm) gate oxide (leading to good control of the top-gate over the channel), good extrinsic mobility (μ~500 $cm^2V^{-1}s^{-1}$), low output conductance (g_d~50 µS/µm), and manageable [not very small, but small enough to obtain $|A|_v$>1] contact resistance (~9 kΩ·µm). Although these inverters pave the way to realistic multi-stage graphene circuits, they also suffer from large parasitics, limiting the clock rate to 200 kHz(52).

Multi-stage circuits must operate at high (>1 GHz) technologically-relevant frequencies to be useful. High-frequency graphene circuits have been developed over the past few years, but they are all single-transistor and single-stage circuits (17). E.g., the first wafer-scale graphene integrated circuit was a 10 GHz frequency mixer, but it consisted of a single GFET integrated with two inductors (56). Similarly, high-frequency graphene voltage amplifiers were reported with $|A_v|$>1, up to 6 GHz, but comprising a single GFET connected to two off-chip bias tees (49).

Elimination of parasitics in inverters integrated on wafer-scale graphene pave the way to high-frequency multi-stage integrated circuits. Ref (14) demonstrated high-frequency graphene ring oscillators (GROs), consisting of 4 cascaded stages and 8 GFETs. GROs were also realized with 12 GFETs (57), however running below 50 MHz.

Graphene ring oscillators

GROs are an extension of the cascaded graphene inverters. They consist of an odd number of inverters cascaded in a loop which makes the RO unstable, therefore induces oscillation. Each inverter in the loop must be identical, with $|A_v|$>1 and in/out signal matching. The two FETs in each inverter must also have very low on-state resistance to be able to quickly charge/discharge the gate capacitance of the next stage in order to reach high-frequency operation. Since the oscillation frequency f_o is a direct measure of delays in realistic scenarios [because a realistic electronic circuit is both driven and loaded by other electronic circuits, exactly what exists in a RO; in contrast, the cutoff frequency f_T is measured on a single FET which is driven by an ideal current source and having a shorted output (zero load impedance)], ROs are the standard test-beds for evaluating ultimate performance limits and the highest possible clock rates of digital logic families (58).

The ROs in Figure 2 were fully integrated on CVD graphene (14). Complementary operation of the inverters within a RO is obtained between the Dirac points of the two FET, as in early graphene inverters (23). These inverters have $|A_v|$>4, enough to enable oscillations under signal matching. The oscillation frequency of a RO with n stages cascaded in a loop is inversely proportional to the inverter rise/fall delays τ as $f_o \propto 1/(2n\tau) = f_{o1}$ (59), where f_{o1} is a fan-out of one (FO1) oscillation frequency. Since $\tau \sim C\, G_D^{-1}$ (14), where G_D is the sum of the extrinsic drain conductances of the FETs in the inverter and C is the parasitic capacitive load of the inverter, reduction of parasitics leads to high-frequency operation.

The speed of electronic circuits is typically increased by downscaling their dimensions (60), which also reduces parasitics (because parasitic capacitances are proportional to the surface area of the corresponding device parts). This is demonstrated in Figure 3, plotting the maximum oscillation frequency of 26 GROs as a function of gate length L. The highest is f_o = 1.28 GHz at L = 1 µm, corresponding to a FO1 inverter delay τ~100ps. This is similar to that of conventional Si CMOS ROs (61), and smaller than polycrystalline Si CMOS thin-film ROs (62) for

the same L. This is the first operating frequency above 1GHz in digital circuits based on any type of novel low-dimensional materials (e.g. nanotubes, nanowires, graphene, MoS_2). By comparison, the highest frequency of nanotube ROs was ~50 MHz (63), and 1.6 MHz in bilayer MoS_2 ROs (64).

Applications of graphene ring oscillators

The dependence of the oscillation frequency of conventional ROs on the supply voltage represents a serious problem in complex digital circuits, since increased power consumption places strong demand on the supply voltage causing it to fluctuate (65). Such fluctuations degrade the operation of logic gates and their noise performance (65). In contrast to other types of ROs, GROs are much less sensitive to fluctuations in the supply voltage, as a consequence of their reduced voltage swing (14). Insensitivity to power supply noise could be a disadvantage in applications in which dynamic frequency and voltage scaling are used to slow the clock rate of digital circuits during periods of reduced workload. However, such insensitivity represents an important advantage in applications in which frequency stability is important, e.g. for clock generation and recovery in high-speed digital systems.

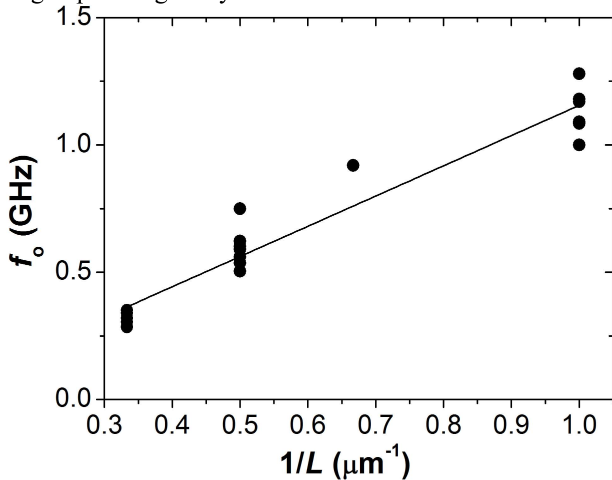

Figure 3: Scaling of oscillation frequency with $1/L$. The plot shows the values obtained from the measurements performed on 26 GROs (only the highest frequencies for each GRO are shown).

GROs and inverters could find applications in digital circuits operating at extremely high frequency (EHF; f>100 GHz) in which high operating speed could be traded off against power dissipation, reduced voltage swing, and circuit complexity (66-69). These ultra-high speed digital circuits were developed to perform data conversion at the transmitting/receiving side of serial EHF lines (70), such that information carried by EHF digital signals can be processed at lower clock rates by low-power, highly integrated, and parallel Si CMOS logic (70). The EHF digital circuits are used in wireless, fiber-optic, and space communications (9).

GROs can find applications in analog electronics. Oscillators are one of the main building blocks of analog electronics (71), e.g., RF (microwave) electronics is built on voltage amplifiers, oscillators, and mixers (72). Graphene amplifiers (49,50), mixers (56,73), and oscillators (14) allow realization of all-graphene microwave circuits.

GROs can also be used to mix analog signals. Graphene analog mixers (56,73) so far require an external local oscillator (LO) for frequency conversion. GROs can overcome this limitation and perform both modulation and generation of oscillating signals to form stand-alone graphene mixers, i.e. mixers with a built-in LO. To this end, the GRO in Fig. 2 was modified by superimposing a RF signal over the dc supply of the buffering inverter 4 (without affecting the supplies of the other three inverters). As the other inverters forming a ring are not affected by the addition of the RF signal, the buffering inverter mixes the RF signal with the unaltered ac component of the oscillating voltage. Figure 4 shows the power spectrum of the up-converted RF signal around the LO signal. The conversion loss is 19.6dB at an LO power of -18.5dBm and RF power of -34.3dBm, better than in early graphene mixers (56,73), and comparable to recent graphene mixers (74,75).

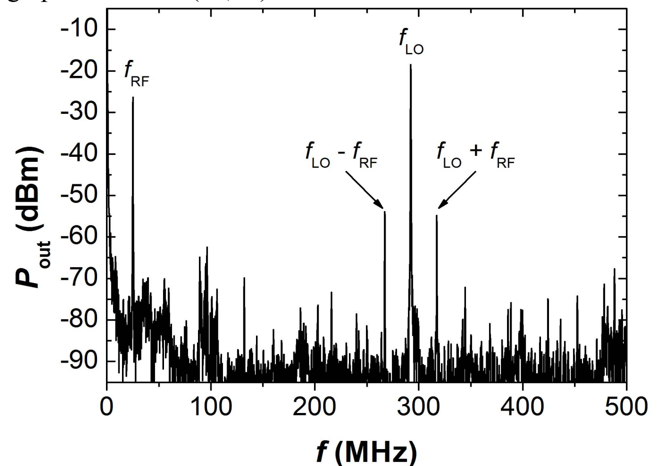

Figure 4: Power spectrum of the output signal of stand-alone graphene mixer at V_{DD} = 2.5 V. The signal frequencies are f_{LO} = 292 MHz and f_{RF} = 25 MHz. Apart from the signals discussed in the main text, the output signal also contains a frequency component at f_{RF}, from the amplification of the RF signal by inverter 4.

Outlook

There are several figures of merit that should be considered before GFETs can be used in realistic multi-stage electronic circuits, instead of InP heterojunction bipolar transistors. First, the lack of a bandgap not only increases power dissipation, but also reduces the voltage swing, thus reducing their noise margin. Second, in order to reach $|A_v|$>1, the gate oxide thickness must be more aggressively scaled than gate length and supply voltage, breaking conventional scaling laws. The oxide thickness in GROs (t_{ox}~4nm) is similar to the 22-nm node Si FETs (15). In both cases further scaling benefits can be obtained only at the expense of other advances. Third, the complementary logic is currently realized through electrostatic doping (14, 44, 45, 50, 52),

which imposes limits on supply voltages in graphene logic gates. In order to lift this restriction, graphene should be doped (21, 76, 77), but without introducing additional scattering centers, in order to maintain high-mobility.

The inverter delay in GROs is similar to Si CMOS inverters at the same gate length (61). This is a consequence of similar extrinsic [i.e. including contact resistance] charge carrier mobilities ($\mu\sim500\ cm^2V^{-1}s^{-1}$) in these two cases (14). Such low extrinsic mobility of graphene (compared to its intrinsic mobility which is much larger than Si and InP) is a consequence of a large contact resistance (here 2.1 kΩ·μm (14)) and scattering from charged impurities in the top and back oxide (78). Both contact resistance and impurity scattering must be reduced if graphene is to replace InP in future EHF circuits. Higher mobility will also allow lower supply voltages thus reestablishing conventional scaling laws.

Radical new device concepts, like ballistic or vertically stacked devices, will need to be developed and their potential investigated. A continuous extension of the work to the circuit and system level needs to be carried out, so that not only single demonstrator circuits will be realized, but also their performance will be optimized towards the requirements of specific applications in different systems. The performance of graphene based devices needs to be continuously evaluated with respect to the state-of-the-art and key specifications will need to be defined in order to warrant industrial relevance.

Heterostructures based on two dimensional (2d) crystals could decouple the performance of particular devices from the properties of naturally available materials (11,79-82). 2d crystals have a number of exciting properties, often unique and very different from those of their 3d counterparts (11,79). However, it is the combinations of such 2d crystals in 3d stacks that offer significant opportunities in designing the functionalities of such heterostructures. One can combine conductive, insulating, probably superconducting and magnetic 2d materials in one stack with atomic precision, fine-tuning the performance of the resulting material. Furthermore, the functionality of such stacks is ”embedded” in the design of such heterostructures. Heterostructures have already played a crucial role in technology, giving us semiconductor lasers and high mobility FETs. However, thus far the choice of materials has been limited to those which can be grown (typically by MBE) one on top of another, thus limiting the types of structures which can be prepared. Instead, 2d crystals of very different nature can be combined in one stack with atomic precision, with control on the properties and functionalities of the resulting 2d-based heterostructures (11,79). 2d materials with very different properties can be combined in one 3d structure, producing novel, multi-functional materials. Most importantly, the functionality of such heterostructures will not simply be given by the combined properties of the individual layers. Interactions and transport between the layers allow one to go beyond simple incremental improvements in performance. By carefully choosing and arranging the individual components one can tune the parameters, creating materials with tailored properties, or ”materials on demand”. Following this novel approach, part of the functionality is brought to the level of the design of the material itself.

Field effect vertical tunneling transistors based on graphene heterostructures with atomically thin BN acting as a tunnel barrier, were reported (81). The device operation relies on the voltage tunability of the tunnel density of states in graphene and of the effective height of the tunnel barrier adjacent to the graphene electrode (81). More recently, Ref. (82) proposed WS_2 as an atomically thin barrier between two layers of graphene, allowing switching between tunneling and thermionic transport, resulting in much better transistor characteristics with respect to the MoS_2 analogue (81), thus allowing for higher on/off ratios ($\sim10^6$). A ”barristor”, a graphene-Si hybrid three-terminal device that mimics a triode operation, was developed by Ref. (83). The electrostatically gated graphene/Si interface induces a tunable Schottky barrier that controls charge transport across a vertically stacked structure. Rapid response and ultra-small sizes can may also be achieved in vertical transistors. Indeed, electron transfer through nm thick barriers can be extremely fast (possibly coherent). Ballistic tunneling transistors may allow us to overcome the most significant drawback of the present approach to graphene electronics, its low on/off ratios. Tunneling devices would have a highly insulated off state with no dissipation, which should allow not only individual transistors, but integrated circuits at RT.

Summary

The development of graphene circuits exhibiting over-unity voltage gain allows realization of realistic multi-stage integrated circuits which can be operated at high, technologically-relevant frequencies. An important example of such circuits is ring oscillators integrated on CVD graphene (14). They oscillate at frequencies above 1 GHz in air, and can be used in a wide range of applications in digital and analog electronics, when ultra-fast operation is favored over static power dissipation. The oscillation frequency could be increased through further advances, e.g. by reducing the gate length, contact resistance, and parasitic capacitances. Even static power dissipation could be reduced by increasing the voltage swing through the use of AB-stacked BLG (45,54,85,86). In the longer term, new devices architectures exploiting the combination of graphene and other layered materials are expected to further widen the scope for integrated circuits at RT.

Acknowledgments

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