## 24.4 Design of CMOS for 60GHz Applications

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Recently, 7GHz of unlicensed bandwidth around 60GHz was opened allowing for a variety of applications including Gb/s point-to-point links, wireless local area networks with extraordinary capacity, and vehicular radar at nearby frequencies. Presently, the exploitation of this band is minimal because of the high cost of the compound semiconductor technology needed to process the mm-wave signals. However, as the high-frequency capabilities of CMOS improve through scaling, the question is not if, but when will CMOS become a viable alternative for mm-wave applications.

 $0.25\mu$ m CMOS technology allows for low-cost radio solutions up to nearly 6GHz, using relatively conventional circuit design and modeling techniques. However, increasing the operating frequency by a factor of 10 requires a new design methodology since the wavelength is now on the order of the dimensions of the chip components (on-chip  $\lambda$ =2.5mm at 60GHz). Although mm-wave CMOS circuits have been demonstrated [1], the optimal device design, performance, and appropriate models are unclear from these circuit experiments. The results presented here indicate that through careful optimization and modeling of the active and passive components, a standard 0.13 $\mu$ m CMOS process is capable of 60GHz operation, and subsequent generations will simply provide higher performance at lower power levels.

A die micrograph of a single transistor is shown in Fig. 24.4.1, with the associated circuit model of a single finger in Fig. 24.4.2. While distributed effects must often be taken into account in the design of passives, it is found that a lumped device model with appropriate parasitics is adequate for the active devices, due to their small dimensions. The most significant parasitics are the series source, drain, and gate resistances (Rs, RD, RG), non-quasistatic channel resistance  $(r_{\mbox{\tiny nqs}}),$  and the resistive substrate network [2]. Terminal inductances  $(L_s, L_D, L_G)$  model the delay effects associated with interconnect wiring. Due to the high sheet resistance of silicided gates (~10 $\Omega/\Box$ ), the gate resistance can be a limitation of CMOS transistors at high frequencies. However, by reducing the finger width, the effect of R<sub>G</sub> is made negligible compared to the other resistive parasitics. Using narrow fingers also allows substrate contacts to be placed more closely to the device, minimizing the substrate losses.

To determine the optimum finger width for a 0.13µm, 1P6M CMOS process, multi-fingered common-source NMOS transistors with  $W_F$ =1–8µm and  $N_F$ =40–100, are fabricated and measured on-wafer to 65GHz. Small-signal transistor models are extracted for each device at numerous bias points ( $I_{DS}/W$ =20–300µA/µm,  $V_{DS}$ =1.2V). Reducing  $W_F$  from 2µm to 1µm results in an increase in f<sub>max</sub> of 15%. The measured and modeled unilateral gain, maximum stable gain (MSG), maximum available gain (MAG), and current gain for a 100×1/0.13 NMOS transistor are shown in Fig. 24.4.3. The close fit between the measured and modeled unilateral gain, in particular, verifies that all critical losses are included. The measured f<sub>max</sub> is 135GHz, and at 60GHz, the unilateral gain is 8.6dB while the MSG is 6.3dB.

For 60GHz circuit design, the reactive component values are very small, requiring inductance values on the order of 50–150pH. Direct implementation of these elements using spiral inductors do not have the required accuracy, so transmission lines are used with the appropriate length and termination. Another benefit of using transmission lines is that the well-defined ground return path confines the fields and significantly reduces coupling to adjacent structures.

If a transmission line is characterized by its equivalent RLGC distributed model, two quality factors can be defined as

$$Q_L = \frac{\omega L}{R}, \ Q_C = \frac{\omega C}{G} \tag{1}$$

Transmission lines store mostly magnetic energy in order to resonate with the intrinsic capacitance of the transistors. Thus, the loss in the line is primarily determined by  $Q_L$ .

There are two basic approaches for implementing transmission lines: microstrips and coplanar waveguides (CPWs). A major advantage of microstrip lines is the intrinsic shielding they provide from the lossy silicon substrate. In addition to reducing the shunt loss, the isolation provided by the ground plane also makes microstrip lines less sensitive to the processing details of the substrate. The biggest drawback to microstrip lines in CMOS is the close proximity of the ground plane to the signal line (~4µm) that results in a very small distributed inductance. Consequently, CMOS microstrip lines typically have low inductive quality factors (Fig. 24.4.4).

CPWs are designed to be more inductive than microstrips. A CPW with conductor width, W, of 10µm and signal-to-ground spacing, S, of 7µm has a  $Q_{\rm L}$  which is nearly double that of the microstrip (Fig. 24.4.4). CPW is also less sensitive to process variation, since the dimensions are determined by lithography and not oxide thicknesses. Furthermore, the coupling to the substrate manifests itself as a reduction in  $Q_c$ , which is not as critical. Another important issue for CPWs is the parasitic odd CPW mode, which can be effectively suppressed by placing underpasses at all discontinuities.

Distributed transmission line models are extracted from measured data for 1mm long CPW lines of different  $Z_0$ . The CPW lines are implemented on metal 6, which is 1µm thick copper. Passive circuits composed of these lines (e.g., a 30GHz bandpass filter, Fig. 24.4.5) are designed to verify that the behavior of a complex connection of CPW lines is accurately predicted using simple scalable models. The measured and simulated results for the filter from 0.04–65GHz are shown in Fig. 24.4.5. At 30GHz, the insertion loss is 2dB and the input return loss is better than 25dB. A die photo of the filter is shown in Fig. 24.4.1.

A 60GHz amplifier (Fig. 24.4.6) is designed to explore what can be achieved in a 0.13 $\mu$ m process with the above components. The amplifier consists of three stages of cascode devices with input, output, and interstage reactive matching. Every component used (cascode transistors, CPW lines, capacitors) has been fabricated and characterized up to 65GHz. The expected performance of the amplifier, based upon the measured and modeled devices, is shown in Fig. 24.4.7. At 60GHz, the gain is 11dB with input and output return loss >20dB. The power consumption is 54mW from a 1.5V supply.

The 7GHz of unlicensed bandwidth around 60GHz offers a unique opportunity to provide a wide range of wireless services. Using a standard digital 0.13 $\mu$ m CMOS process, the basic elements required for operation at 60GHz are demonstrated, thus opening the door for CMOS to become the emerging mm-wave technology solution.

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Figure 24.4.1: Micrograph of mm-wave test structures (80 $\times$ 1/0.13 NMOS and 30GHz CPW filter).



 $(I_{ps}/W=300\mu A/\mu m, V_{ps}=1.2V)$ 













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