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On-chip deposition of carbon nanotubes using CMOS microhotplates

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Abstract
The direct deposition of carbon nanotubes on CMOS microhotplates is demonstrated in this paper. Tungsten microhotplates, fabricated on thin SOI membranes aside CMOS control circuitry, are used to locally grow carbon nanotubes by chemical vapour deposition. Unlike bulk heating of the entire chip, which could cause degradation to CMOS devices and interconnects due to high growth temperatures in excess of 500 °C, this novel technique allows carbon nanotubes to be grown on-chip in localized regions. The microfabricated heaters are thermally isolated from the rest of the CMOS chip as they are on the membranes. This allows carbon nanotubes to be grown alongside CMOS circuitry on the same wafer without any external heating, thus enabling new applications (e.g. smart gas sensing) where the integration of CMOS and carbon nanotubes is required.

1. Introduction

Nanostructured materials for gas sensing have been of great interest because of their high surface to volume ratio. Conventionally, bulk materials such as tin oxide (SnO_2) [1] are widely applied as the sensing material, but in comparison to nanostructured alternatives, bulk materials have a smaller reactive area and hence typically lower sensitivities. The combination of microelectronic circuits, such as silicon CMOS devices, with nanostructured gas sensing materials enables ‘smart’ sensors to be made which are both smaller and cheaper to manufacture in a wafer-scale production environment [2]. The integration of nanostructured sensing material with thermally isolated, low thermal mass on-chip heaters allows cycling of the sensing material at multiple temperatures to perform detection. As different gases have characteristic responses at different temperatures, such a device may be used like an electronic nose which not only has high sensitivity, but selectivity as well.

Carbon nanotubes (CNTs) [3–12] are one of the most studied nanostructured materials being investigated for gas sensors [13–18]. The advantageous properties of CNTs include their small size, high strength, relative chemical inertness, high electrical and thermal conductivity, and high specific area. There are various reports in the literature of CNTs being used for NO_2, NH_3, CO, and O_2 detection [15–18]. Such sensors have relatively fast response and high sensitivity compared with conventional bulk material sensors. It is thus advantageous to couple CNT sensors with CMOS circuitry to build smart sensors. Although chemical vapour deposition (CVD) and plasma enhanced CVD (PECVD) are wafer-scale production techniques for CNTs, these have not been applied for this purpose because of the high temperatures involved in CNT growth which destroy the CMOS circuits. Chemical vapour deposition (CVD) is a common technique for depositing CNTs [19–22], and in this process, the substrates, coated with metal catalyst (Fe, Ni, Co), are heated to form islands at around 500 °C on a heater or furnace. Growth is typically initiated at an elevated temperature (750–850 °C) under a constant flow of hydrocarbon gas. It is exposure to this high temperature, in excess of 500 °C, that damages CMOS transistors and causes interlayer breakdown between different levels of the circuit.

Here, we report a novel growth technique which uses an on-chip (i.e. *in situ*) microheater to grow CNTs locally on the chip, without the need to bulk heat the entire chip to elevated temperatures. As the microheaters used are located on membranes, they are thermally isolated from the SOI CMOS

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circuits which are fabricated on the active silicon of the chip. The microheaters themselves are low in power, which makes this process attractive compared with bulk heating of the silicon wafer. Note that this concept can also be applied to growth of other nanostructured materials for CMOS sensing devices.

2. Fabrication and experimental details

In the literature, several different materials have been used as heaters in microhotplates, and also different designs of membranes have been reported [24–27]. The heaters are usually based on platinum, aluminium and polysilicon resistors, each with their specific advantages and disadvantages. We have reported on the use of other CMOS materials/devices such as silicon heaters [35], silicon MOSFETs [23] or tungsten [25]. Aluminium and polysilicon are both CMOS compatible and are used in standard CMOS fabrication. Although platinum has a high melting point and possesses advantageous material properties for a heater (e.g. chemical stability, linear coefficient of resistance with temperature), its use in a post-CMOS process in a commercial CMOS foundry is unlikely due to incompatibility with other standard CMOS materials. Aluminium on the other hand has a relatively low melting point (660 °C) and is prone to electromigration, especially if operated at high temperature. Polysilicon suffers from poor stability at high temperatures, which makes it not the ideal choice for microheaters. MOSFET heaters using SOI technology [23] cannot operate reliably at high temperature above 500 °C [24] due to parasitic bipolar effects. For our high temperature growth application ($\sim$700 °C), tungsten is the obvious choice. It has a melting point of approximately 3140 °C, and at the CNT growth temperatures, it is mechanically strong and can operate reliably without degradation due to electromigration. It is also CMOS compatible, and standard SOI CMOS processes exist for tungsten deposition and etching. Tungsten also has an electrical resistivity which is high enough to be used as a heater, but at the same time low enough to be used as the interconnect in CMOS circuits. Thus, with tungsten interconnects, it is possible to integrate both the control circuitry with the microhotplate on the same chip. All these aspects make tungsten [25] an ideal material for the design and fabrication of a microhotplate (MHP) [25–27, 36] for gas sensors, which utilize the heater to assist in the promotion of reaction between the sensing material and the exposed gas.

The fabrication of our wafers containing microhotplates and CMOS control circuitry was performed at XFAB (Germany) and Silex (Sweden). A standard CMOS SOI process was used, starting with 'smart cut wafers' [28], which then used tungsten as the metal layers for CMOS interconnects, microhotplate (i.e. heater meander) and contacts for the sensing material (i.e. interdigitated electrodes). This was followed by deep reactive ion etching (DRIE), which formed the membranes to thermally isolate the microhotplates from the rest of the CMOS circuits. Finally, nanotubes were grown on the microhotplates using an on-chip local growth technique. Other groups have previously shown similar methods [29–31] of growing CNTs on localized regions but tungsten offers more promising solutions in a CMOS compatible platform. The process proposed here, incorporating tungsten heaters and interconnects, is the only CMOS process today which offers high operating temperature capability, and is an ideal platform for CNT–CMOS integration. The cross section of our device is illustrated in figure 1(a). The sensor area contains the microheater with back-etched substrate to provide thermal isolation. The control CMOS circuits, comprising 1.0 μm technology processed NMOS and PMOS transistors, are located on the same wafer. Figure 1(b) shows an optical micrograph of one such device. Two different diameter (560 and 300 μm) membranes were used, incorporating tungsten heaters having diameters of 150 and 24 μm respectively.

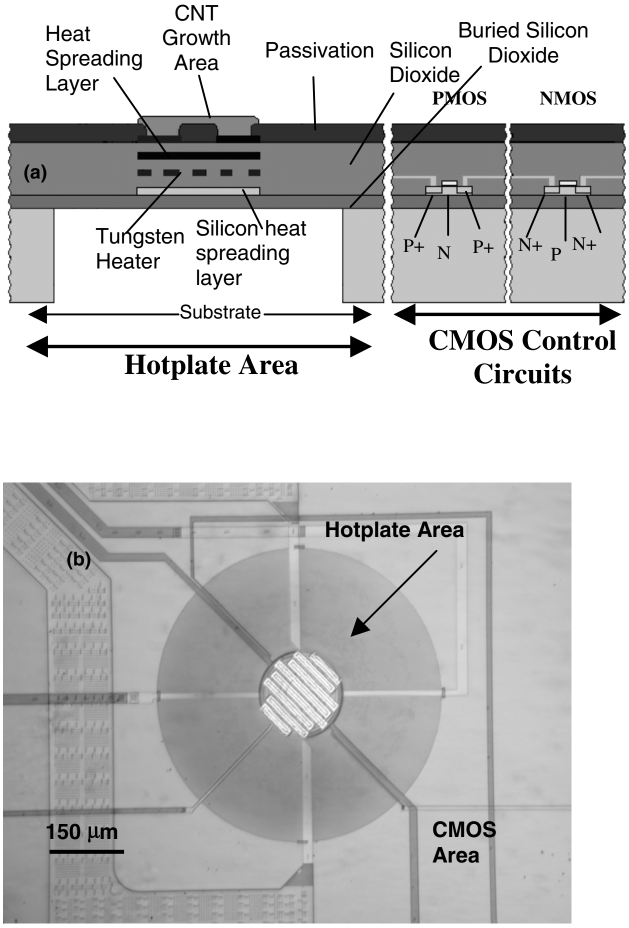

Figure 1. (a) Structural cross-sectional layout of the chip. (b) Optical microscope view of the device, showing larger membranes with interdigitated electrodes, heater radius = 75 μm, membrane radius = 280 μm.

For thermal characterization the tungsten heaters were calibrated using a high temperature chuck (Signatone S-1060R-6TG) using unetched wafers because etched wafers were difficult to measure at high temperatures due to larger bowing. The microhotplates were then subsequently characterized by using a constant current source and measuring the voltage across the heater. The temperature coefficient of resistance (TCR) was extracted using the change in resistance during calibration. As the resistance of tungsten changes with

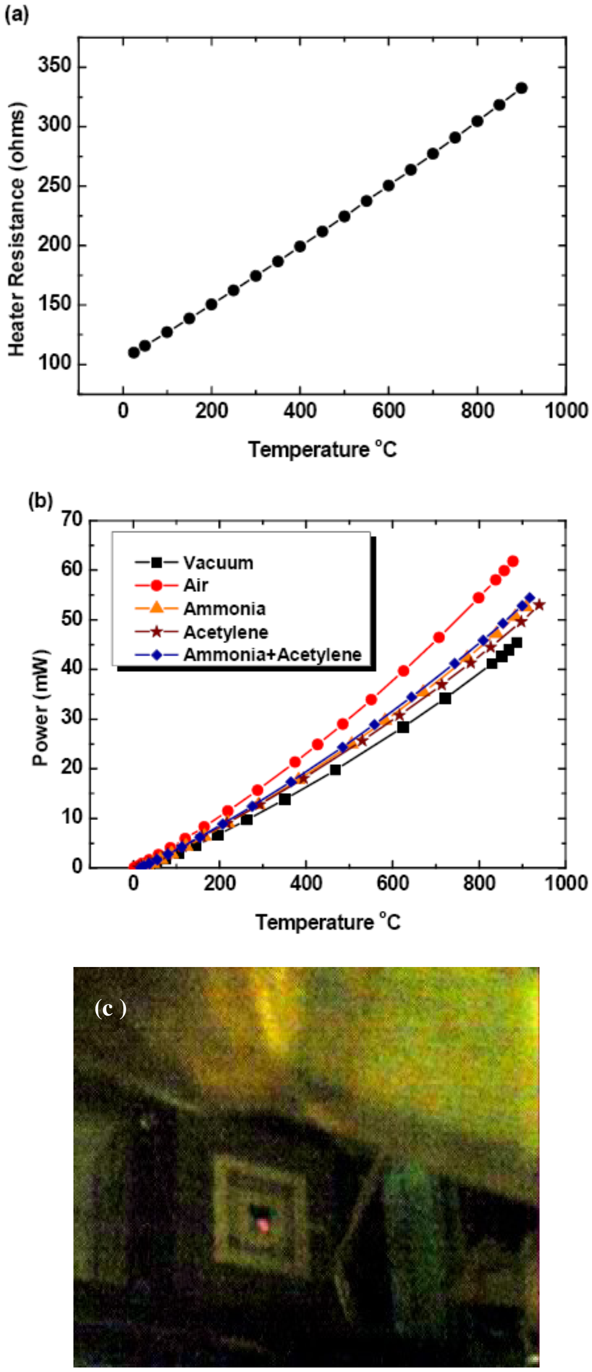

Figure 2. (a) The temperature calibration curve for the tungsten heater. (b) The variation of power consumption of the large microhotplates with temperature when exposed to different gases. (c) A picture of a glowing heater during deposition of CNTs.

temperature with a known coefficient of $2.05 \times 10^{-3}\ \Omega\,°\mathrm{C}^{-1}$, it is possible to use the heater's resistance as a direct measure of the heater temperature. A temperature calibration curve, which plots a 150 μm diameter heater's resistance with temperature, is shown in figure 2(a). It can be noted from the graph that the temperature has an almost linear relationship with the resistance of the tungsten heater, characteristic of metals. This calibration curve is then used to determine the heater's temperature under different gas environments, and the measured voltage and current are used to determine the power used by the heater. As shown in figure 2(b), the 150 μm heaters typically require 50 mW to reach a temperature in excess of 750 °C in the presence of various gases, and for the 24 μm heater (not shown) the power required was around 20 mW. This electrical data were then used to operate the heater at the correct temperature during CNT growth.

The growth of multiwalled CNTs on the microheater membranes was performed using thermal CVD [32]. Note that the tungsten heaters are coated with a passivation/isolation layer of Si_3N_4. 2–4 nm of Fe catalyst was then locally deposited on the microheaters by sputter coating. The devices were packaged (CPG06864 Spectrum Semi Ceramic model) and connected within a PCB to supply power. The devices were then loaded into a vacuum chamber and a base pressure of 0.2 mbar was attained on the devices. Using an external Keithley power supply (model 2400), a constant current was applied to the microhotplates to heat them up to 750 °C. The corresponding voltage was then measured to extract the resistance and then this was compared with the calibration curve to determine the operating temperature. Within milliseconds, the heater reaches a high temperature and can be seen visibly to be glowing (see figure 2(c)). The transient electrical response of the heaters (not shown) was used to verify that the heater indeed reaches temperature within milliseconds. Acetylene and ammonia, at a ratio of 1:4 (50 sccm: 200 sccm) and a partial pressure of 6.5 mbar, were then introduced. As the gases were released into the chamber, more power was required to keep the heaters at the specific temperature required for the growth due to convective cooling. The current was thus increased until the resistance of the tungsten heater indicated that it was operating at 750 °C. The growth time used was typically from 2 to 4 min, after which the gases were turned off and the device allowed to cool.

3. Results

This process produced multiwalled CNTs with a diameter of 30–80 nm. There was a 100% yield over the tungsten heaters on the chip, and, after processing, electrical measurements of the control PMOS and NMOS transistors confirmed that there was no degradation to the CMOS circuits. Figure 3(a) shows a chip with locally grown CNTs on microheaters. Figures 3(b) and (c) are SEM observations of the CNTs. In figures 3(b) and (c), the CNTs were grown onto interdigitated electrodes which have a buried microhotplate underneath them. The density and length of the tubes were high and long enough to breach the electrodes and fully cover the area. The resistance between the electrodes was measured to be in the range 0.50–2.0 kΩ (kiloohms) for various devices. By changing the thickness of the catalyst (Fe) [19], the diameter of the CNTs can be changed. The length of the CNTs is, in general, controlled by the deposition time. Raman spectroscopy [33] was also used to examine the nanotubes. The two main features from the Raman spectra of figure 3(d) are the D and G peaks at 1350 and 1600 cm^{-1}, respectively, which are similar to published works on multiwalled carbon nanotubes; for

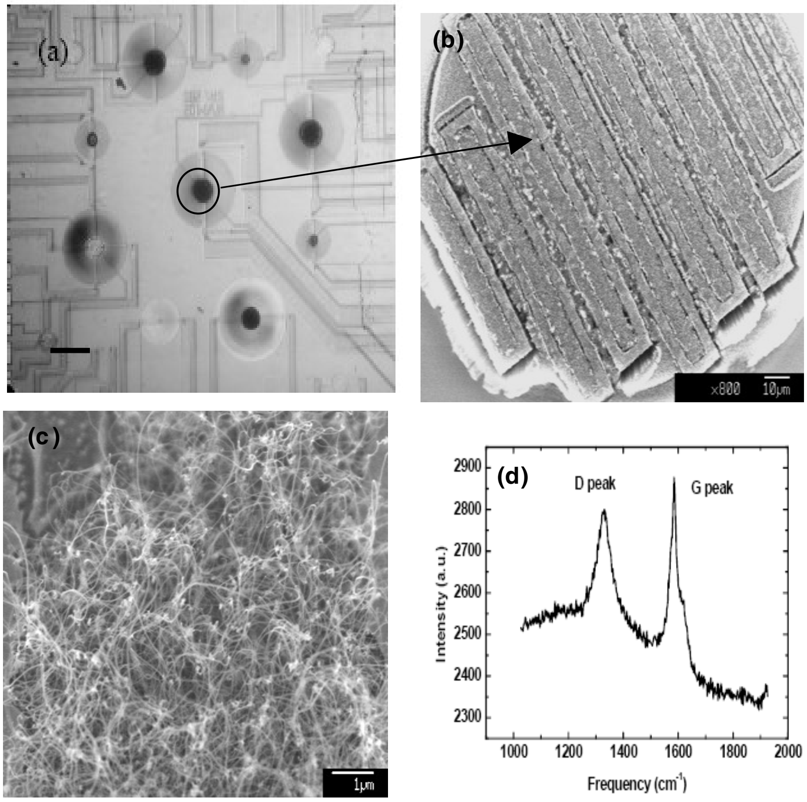

Figure 3. (a) Microscopic images of carbon nanotubes grown locally on ultrathin membranes incorporating a tungsten heater, scale bar = 500 μm. (b) Plan-view FE-SEM images of carbon nanotubes grown locally on ultrathin membranes incorporating tungsten microhotplates with interdigitated electrodes. (c) FE-SEM image of CNTs on the interdigitated electrodes at a higher magnification. The typical diameter is 60–80 nm. (d) Raman spectra of multiwalled carbon nanotubes locally grown on the large microhotplates.

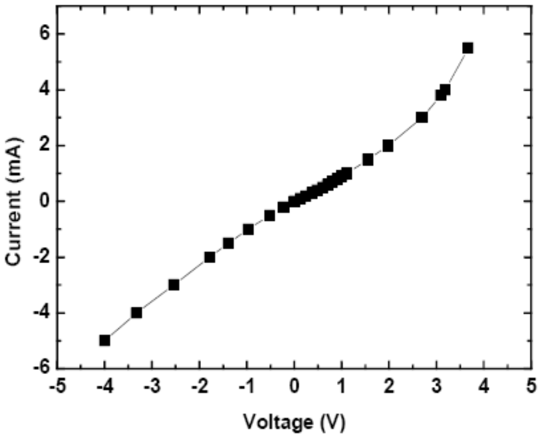

Figure 4. I–V characteristics of the tungsten interdigitated electrodes connected with CNTs.

example, see [33]. The on-chip CMOS circuits were then used to obtain the electrical response of the CNTs grown between the interdigitated electrodes. Figure 4 shows the electrical characteristics of the CNTs on tungsten electrodes. The I–V characteristics show some junction effects characteristic of CNT/metal Schottky contacts [34]. The application to gas sensors of locally grown carbon nanotubes (CNTs) onto CMOS microhotplates is treated elsewhere [37].

4. Conclusion

In this work, a novel local growth process was used to directly integrate carbon nanotubes with CMOS circuits on the same chip. A standard CMOS process was used to fabricate the transistors, which incorporated tungsten metallization for circuit interconnects and the microheaters. The microheaters were deliberately fabricated on membranes for thermal isolation. This also resulted in low-thermal-mass heaters which required very little power (milliwatts) to heat up, which could then be used to grow CNTs locally. CNTs were grown onto interdigitated electrodes and their electrical response determined using on-board CMOS circuits. This technique offers a route to integration of CNTs with CMOS technology, and is an ideal platform for smart gas sensing applications, where it is advantageous to combine CMOS circuitry with CNTs (or other nanostructured material) on a microheater platform.

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