Advantages of top-gate, high-*k* dielectric carbon nanotube field-effect transistors

M. H. Yang, K. B. K. Teo,[a] Laurent Gangloff, and W. I. Milne
Department of Engineering, University of Cambridge, Trumpington Street, Cambridge CB2 1PZ, United Kingdom

D. G. Hasko
Microelectronics Research Center, University of Cambridge, Madingley Road CB3 0HE, United Kingdom

Y. Robert and P. Legagneux
Thales R&T France, Domaine de Corbeville, Orsay 91404, France

(Received 8 August 2005; accepted 7 February 2006; published online 15 March 2006)

The subthreshold slope, transconductance, threshold voltage, and hysteresis of a carbon nanotube field-effect transistor (CNT FET) were examined as its configuration was changed from bottom-gate exposed channel, bottom-gate covered channel to top-gate FET. An individual single wall CNT was grown by chemical vapor deposition and its gate configuration was changed while determining its transistor characteristics to ensure that the measurements were not a function of different chirality or diameter CNTs. The bottom-gate exposed CNT FET utilized 900 nm SiO_2 as the gate insulator. This CNT FET was then covered with TiO_2 to form the bottom-gate covered channel CNT FET. Finally, the top-gate CNT FET was fabricated and the device utilized TiO_2 ($\kappa \sim 80$, equivalent oxide thickness=0.25 nm) as the gate insulator. Of the three configurations investigated, the top-gate device exhibited best subthreshold slope (67–70 mV/dec), highest transconductance (1.3 μS), and negligible hysteresis in terms of threshold voltage shift. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2186100]

The single wall carbon nanotube (SW CNT) is a promising candidate as a building block for future nanoelectronic devices. Carbon nanotube field-effect transistors (CNT FET) consisting of SW CNT channels have been successfully fabricated and operated. These devices typically use a gate electrode to control the carrier density of a semiconducting SW CNT.[1–3] The simplest configuration of a CNT FET is the bottom-gate FET, in which, a SW CNT is dispersed or directly grown on a SiO_2/Si substrate, source drain contacts formed at the ends of the CNT, and its transport properties controlled by applying a substrate voltage. Top-gate CNT FETs in which the gate electrode and gate insulator are located on top of the SW CNT, have several advantages for integrated circuit applications. Top-gated CNT FETs allow local gate biasing at low voltage, high speed switching, and high integration density. In the literature, top-gated CNT FETs have been fabricated using 15–20 nm thick SiO_2 as the gate insulator.[4] To improve the device performance further, a thinner gate insulator with a higher dielectric constant can be used. Recently, high κ materials, such as, TiO_2,[5] ZrO_2,[6] and HfO_2 (Ref. 7) thin films have also been employed as the insulator in top-gate CNT FETs.

This work investigates the effect of the CNT FET configuration on its subthreshold slope, transconductance, and threshold voltage shift (or hysteresis), using the same SW CNT. The first structure fabricated was the substrate (i.e., back) gated CNT FET. Degenerately *n*-doped Si substrate was used as the bottom-gate electrode with 900 nm SiO_2 of thermal oxide as the insulating dielectric. The SW CNT was deposited by chemical vapor deposition of C_2H_2 at 1000 °C for 5 s on a triple-layer metal thin film (Al 10 nm/Fe 1 nm/Mo 0.2 nm), with Fe as the active catalyst for CNT growth, as described in previous work.[14] By prepatterning the metal thin film, prior to CNT deposition, site selective CNT growth is achieved. The CNT diameters were about 1.3 nm, on average, as measured by transmission electron microscopy and atomic force microscopy. By controlling the catalyst island size and its spacing, it is possible, on average, to obtain one CNT growing between the catalyst islands. The CNT diameters were about 1.3 nm on average, as measured by transmission electron microscopy and atomic force microscopy. Source and drain electrodes (20 nm thick Pd) were then fabricated using electron beam lithography, sputtering and a lift-off technique. It has been reported that Pd forms an Ohmic contact or low barrier Schottky contact on CNTs.[15] The structure of the CNT FET and its fabrication process are shown schematically in Fig. 1(a) with a scanning electron micrograph of the device in Fig. 1(b). The source to drain distance of the device was 1.2 μm.

Electrical measurements were carried out on the bottom-gated CNT FET at room temperature in air using an Agilent 4040B semiconductor parameter analyzer. Note that the CNT channel is exposed in this configuration. The gate transfer characteristics are presented in Fig. 2. At $V_{ds}=200$ mV, the threshold voltage V_{th} is 0 V, on-current $I_{on}=1\times10^{-7}$ A, and off-current $I_{off}=1\times10^{-12}$ A, giving this device an on/off ratio=10^5. The subthreshold slope is 1000 mV/dec and transconductance $0.04\ \mu S|_{V_{ds}=200\ mV}$; this corresponds to the normalized transconductance (assuming 1.3 nm diameter CNT) of $30\ \mu S/\mu m|_{V_{ds}=200\ mV}$ Note that the gate transfer characteristics of Fig. 2 clearly shows a large $V_{threshold}$ hysteresis of 7 V depending on the direction the gate voltage was cycled.

[a]Electronic mail: kbkt2@cam.ac.uk

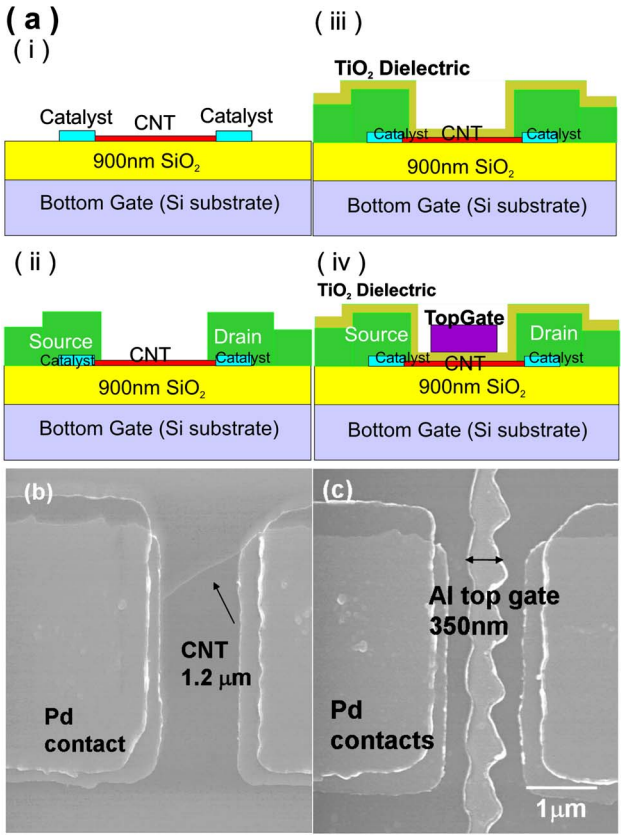

FIG. 1. (Color online) (a) Fabrication process for the CNT FET. First, the CNT is grown from prepatterned catalyst islands (i), followed by the fabrication of source-drain contacts (ii). This completes the bottom-gate exposed channel CNT FET. The CNT is then covered with TiO_2 (iii) to form the bottom-gate covered channel CNT FET. Finally, an Al gate electrode is fabricated on top of the TiO_2 (iv) to form the top-gate CNT FET. (b) Scanning electron micrograph of the bottom-gated CNT FET. (c) Scanning electron micrograph of the same device after fabricating the top-gate.

Next, 5 nm TiO_2 was deposited on top of the structure using electron (e)-beam lithography, e-beam evaporation and lift-off. The TiO_2 deposition was performed using the DENTON VACUUM Infinity-22 tool by ion assisted evaporation. The gate transfer characteristics were determined again as shown in Fig. 3. At $V_{ds}=200$ mV, the threshold voltage V_{th} is 0 V, on-current $I_{on}=5\times10^{-7}$ A, and off-current $I_{off}=4\times10^{-11}$ A. The on/off ratio is 10^4 and the subthreshold slope improved to 320 mV/deg. The transconductance also increased to $0.38\ \mu S|_{V_{ds}=200\ mV}$ corresponding to a normalized transconductance (assuming again a 1.3 nm diameter CNT) of $300\ \mu S/\mu m|_{V_{ds}=200\ mV}$ By simply covering the CNT but still maintaining the bottom-gate operation, we observed that the hysteresis in $V_{threshold}$ was reduced to 2 V.

Finally, a 50 nm thick Al gate electrode was deposited on top of the TiO_2 by e-beam lithography, sputtering, and lift-off, as shown in Fig. 1(c). The gate length was 350 nm and the source drain distance was 1.2 μm. Note that the equivalent oxide thickness of the 5 nm TiO_2 high κ dielectric (dielectric constant $\kappa\sim80$) was merely 0.25 nm. No current leakage (down to our measurement limit of 10^{-13} A) was observed from the gate electrode to either the source or drain contacts through the thin high-κ dielectric. The gate transfer characteristics of the top-gated device are shown in Fig. 4. The on/off ratio is $\sim10^4$. At $V_{ds}=50$ mV, the subthreshold slope is 67–70 mV/dec. Note that this is near the theoretical minimum of $\sim$60 mV/dec, calculated at room temperature

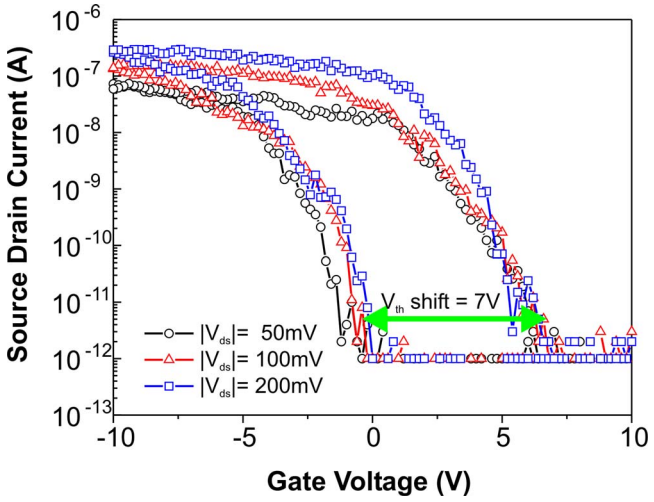

FIG. 2. (Color online) Gate transfer characteristics of the bottom-gate exposed channel CNT FET using $V_{ds}=50$, 100, and 200 mV.

using $(k_BT/e)\ln(10)$, where k_B is the Boltzman constant, T is the temperature, and e is the elemental charge.[12] The transconductance of this device was $0.4\ \mu S|_{V_{ds}=50\ mV}$, which corresponded to a normalized transconductance of $300\ \mu S/\mu m|_{V_{ds}=50\ mV}$, taking again the nanotube diameter (1.3 nm) as the channel width. When using higher source drain voltages $V_{ds}=200$ mV, the CNT FET threshold voltage V_{th} is at 0.25 V, on-current $I_{on}=5\times10^{-11}$ A and off-current $I_{off}=5\times10^{-11}$ A. The subthreshold slope remained at 70 mV/dec. The measured transconductance is $1.3\ \mu S|_{V_{ds}=200\ mV}$ which corresponds to a normalized transconductance of $1000\ \mu S/\mu m|_{V_{ds}=200\ mV}$. Last, note that there is negligible hysteresis in the gate transfer characteristics in this configuration. With highest transconductance and best subthreshold slope, the top-gate configuration has the highest performance with respect to the previous two configurations studied on the same CNT.

Our results can be explained using the classical model for field-effect transistors. In field-effect transistors, the transconductance g_m is given by $g_m=\mu(C/L)(V_{ds}/L)$, where μ is the carrier mobility, C is the gate capacitance, and L is the gate length. A larger transconductance can thus be obtained by increasing μ, C, or decreasing L. Note that in the

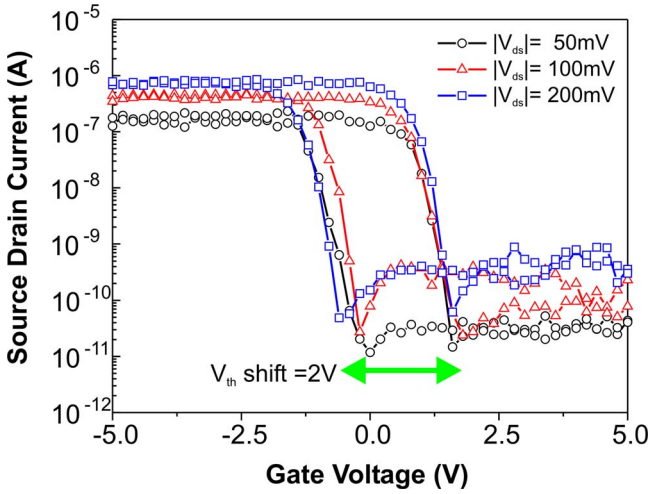

FIG. 3. (Color online) Gate transfer characteristics of the bottom-gate covered channel CNT FET using $V_{ds}=50$, 100, and 200 mV.

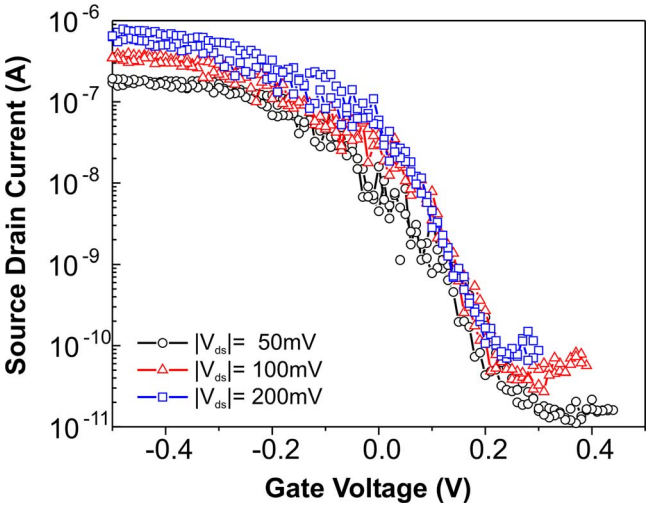

FIG. 4. (Color online) Gate transfer characteristics of the top-gate CNT FET using $V_{ds}=50$, 100, and 200 mV.

two bottom-gate configurations, μ and L are constant since the same CNT has been used and the gate length fixed at 1.2 μm. In the top-gate configuration, the same CNT was retained but the gate length was 350 nm. The electrostatic gate capacitance per length may be approximated by $C_{g1}=2\pi\kappa\varepsilon_0/\ln(4t/d)$, where t is the dielectric thickness and d is the CNT diameter. The first structure investigated, namely the bottom-gate exposed CNT FET, is electrostatically unfavorable as its gate insulator (SiO_2, $\kappa=4$) capacitance is diluted by the lower dielectric constant of the air surrounding the CNT. When the CNT is covered with TiO_2, the gate capacitance marginally improves because the high-k TiO_2 provides electrostatic coupling to the CNT, however, most of the coupling is still via the 900 nm thick SiO_2. In the top-gate geometry, the electrostatic coupling to the CNT is now via the very thin, high-k TiO_2. The gate capacitance ratio of the three cases considered here is approximately top-gate TiO_2: bottom-gate TiO_2: bottom-gate air=20:1.7:1 using the approximation of $C_{g1}=2\pi\kappa\varepsilon_0/\ln(4t/d)$ without considering the fringe effects.

Note that the transconductance of these three device structures are $1.3\ \mu S|_{V_{ds}=200\ mV}$ (top-gate), $0.38\ \mu S|_{V_{ds}=200\ mV}$ (bottom-gate covered CNT), $0.04\ \mu S|_{V_{ds}=200\ mV}$ (bottom-gate exposed CNT). Their corresponding ratio of 32:10:1 follows the trend in gate capacitances, although there are some deviations in the actual numbers. These results suggest that another factor is improving the transconductance of the CNT FET, perhaps the interaction of the CNT/contact barrier with the electrostatic field. The transconductance of the CNT FET devices is known to be affected by lowering or elimination of the Schottky barrier at the nanotube-metal interface by the high electric field at the dielectric-metal interface.[4,10–12]

Hysteresis effects in the gate transfer characteristics are due to charge traps. The $V_{threshold}$ shifts observed are 7 V for the bottom-gated exposed CNT FET, 2 V for the bottom-gate covered-CNT FET, and <10 mV for the 5 nm TiO_2 top-gate CNT FET. Several groups reported SW CNT FETs fabricated on SiO_2/Si substrates exhibiting hysteresis in current versus gate-voltage (Si as bottom-gate) characteristics and attributed the hysteresis to charge traps in bulk SiO_2, oxygen-related defect trap sites near nanotubes, or traps at the SiO_2/Si interface.[13–15] The top-gate CNT does not show much hysteresis because the voltage swing of the gate is small, causing less charge to be stored in the insulators both above and below the CNT. Hence, we can also expect that the bottom-gated exposed CNT has the most hysteresis because of the large gate voltage swing required, which stores charge in the insulators. Furthermore, it is also possible to store charge in the molecules adsorbed to the exposed CNT.[16]

In conclusion, the top-gated CNT FET with a TiO_2 high-κ gate dielectric exhibits the highest transconductance (1.3 μS or 1000 μS/μm), a subthreshold swing (67–70 mV/dec) which approaches the room temperature theoretical limit, and negligible hysteresis in the gate transfer characteristics, of the three different configurations of CNT FET studied here using the same CNT. Further improvements in the device characteristics can be expected by using a higher band gap CNT and/or shorter channel length. A higher band gap (i.e., smaller diameter CNT) will result in lower off current, higher on/off ratio and improve the subthreshold slope at the same C_g. Additionally, shortening the channel length will additionally improve the on-current and it has been reported that 1.1 μA at $V_{ds}=100$ mV has been obtained from a CNT FET with 20 nm channel length.[17]

K.B.K.T. acknowledges the support of the Royal Academy of Engineering and Christ's College Cambridge. This work was also supported by the EPSRC.

[1] S. J. Tans, A. R. M. Verschueren, and C. Dekker, Nature (London) **393**, 49 (1998).
[2] R. Martel, T. Schmidt, H. R. Shea, T. Hertel, and Ph. Avouris, Appl. Phys. Lett. **73**, 2447 (1998).
[3] C. Zhou, J. Kong, and H. Dai, Appl. Phys. Lett. **76**, 1597 (2000).
[4] S. J. Wind, J. Appenzeller, R. Martel, V. Derycke, and Ph. Avouris, Appl. Phys. Lett. **80**, 3817 (2002).
[5] F. Nihey, H. Hongo, M. Yudasaka, and S. Iijima, Jpn. J. Appl. Phys., Part 1 **41**, 1049 (2002).
[6] A. Javey, H. Kim, M. Brink, Q. Wang, A. Ural, J. Guo, P. McIntyre, P. McEuen, M. Lundstrom, and H. Dai, Nat. Mater. **1**, 141 (2002).
[7] A. Javey, J. Guo, D. B. Farmer, Q. Wang, D. Wang, R. G. Gordon, M. Lundstrom, and H. Dai, Nano Lett. **4**, 447 (2004).
[8] R. G. Lacerda, A. S. Teh, M. H. Yang, K. B. K. Teo, N. L. Rupesinghe, S. H. Dalal, K. K. K. Koziol, D. Roy, G. A. J. Amaratunga, W. I. Milne, M. Chhowalla, D. G. Hasko, F. Wyczisk, and P. Legagneux, Appl. Phys. Lett. **84**, 269 (2004).
[9] A. Javey, J. Guo, Q. Wang, M. Lundstrom, and H. Dai, Nature (London) **424**, 654 (2003).
[10] B. M. Kim, T. Brintlinger, E. Cobasm, M. S. Fuhrer, H. Zheng, Z. Yu, R. Droopad, J. Ramdani, and K. Eisenbeiser, Appl. Phys. Lett. **84**, 1946 (2004).
[11] S. Heinze, J. Tersoff, R. Martel, V. Derycke, J. Appenzeller, and Ph. Avouris, Phys. Rev. Lett. **89**, 106801 (2002).
[12] S. Heinze, M. Radosavljevic, J. Tersoff, and Ph. Avouris, Phys. Rev. B **68**, 235418 (2003).
[13] M. S. Fuhrer, B. M. Kim, T. Durkop, and T. Brintlinger, Nano Lett. **2**, 755 (2002).
[14] M. Radosavljevi, M. Freitag, K. V. Thadani, and A. T. Johnson, Nano Lett. **2**, 761 (2002).
[15] J. B. Cui, R. Sordan, M. Burghard, K. Kern, Appl. Phys. Lett. **81**, 3260 (2002).
[16] W. Kim, A. Javey, O. Vermesh, Q. Wang, Y. Li, and H. Dai, Nano Lett. **3**, 193 (2003).
[17] R. V. Seidel, A. P. Graham, J. Kretz, B. Rajasekharan, G. S. Duesberg, M. Liebau, E. Unger, F. Kreupl, and W. Hoenlein, Nano Lett. **5**, 147 (2005).