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Self-Aligned, Gated Arrays of Individual Nanotube and Nanowire Emitters

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ABSTRACT

We demonstrate the production of integrated-gate nanocathodes which have a single carbon nanotube or silicon nanowire/whisker per gate aperture. The fabrication is based on a technologically scalable, self-alignment process in which a single lithographic step is used to define the gate, insulator, and emitter. The nanotube-based gated nanocathode array has a low turn-on voltage of 25 V and a peak current of 5 μA at 46 V, with a gate current of 10 nA (i.e., 99% transparency). These low operating voltage cathodes are potentially useful as electron sources for field emission displays or miniaturizing electron-based instrumentation.

One-dimensional structures, such as carbon nanotubes and nanowires, exhibit excellent field emission properties[1−4] and thus are the subject of intense research into their application as potential electron sources in various vacuum electronic applications. Their favorable field emission characteristics arise from the fact that nanotubes and nanowires are both high in aspect ratio and whisker-like in shape; this is the most effective tip structure for maximizing the geometrical field enhancement when compared with common conical tip shapes such as sharpened, spheroidal, and pyramidal.[5] Recently, it has been demonstrated that nanotube electron sources can in fact deliver high brightness electron beams (10^9 Am^{-2} sr^{-1} V^{-1} s, one order better than today's state-of-the-art Schottky or field emission sources) with a small energy spread (0.2−0.3 eV);[6] these are very desirable properties indeed for sources employed in electron optic/microscopy applications. This paper investigates carbon nanotubes prepared by plasma-enhanced chemical vapor deposition (PECVD)[7−9] and silicon nanowires prepared by the vapor−liquid−solid method,[10] and their integration into gated cathodes. The key advantages of these two techniques, compared with other deposited or etched tips, is that (1) the diameter of the structures is controlled by the catalyst size,[11,12] (2) the height is controlled by synthesis time,[9] (3) the growth orientation can be controlled to be perpendicular to the substrate surface, and (4) the location of the nanotube/nanowire can be controlled by catalyst placement through lithographic means. In our previous work, we showed that carbon nanotubes can be deterministically fabricated with typical standard deviation in the diameter and height of 4.1% and 6.3%, respectively, leading to excellent emitter uniformity as determined by electrical measurements.[11,13]

In applications such as field emission lamps[14] and gas discharge tubes,[15] electron emission is used in a diode-type configuration where high voltage (approximately +1000 V) is applied at the anode to extract the electrons from the emitter. However, for field emission displays (FEDs), microwave amplifiers, and microelectron source instruments (e.g., parallel electron beam lithography, miniature scanning electron microscope), a "triode" type arrangement with an additional integrated extraction gate electrode is preferred. By integrating the gate, the gate-to-emitter distance can be substantially reduced and hence the voltage required for controlling electron emission is also reduced to few tens of volts. This subsequently reduces the power, complexity, and cost of the gate drive/modulation circuitry. Various integrated gate cathodes using *multiple* carbon nanotubes per aperture have been demonstrated.[16−17,18,19] For some applications, such as microelectron beams for lithography and microscopy, the fabrication of *individual* emitter gated cathodes is required. The feasibility of a single, conical-shaped carbon nanofiber cathode has been demonstrated,[20] but no fabrication yield

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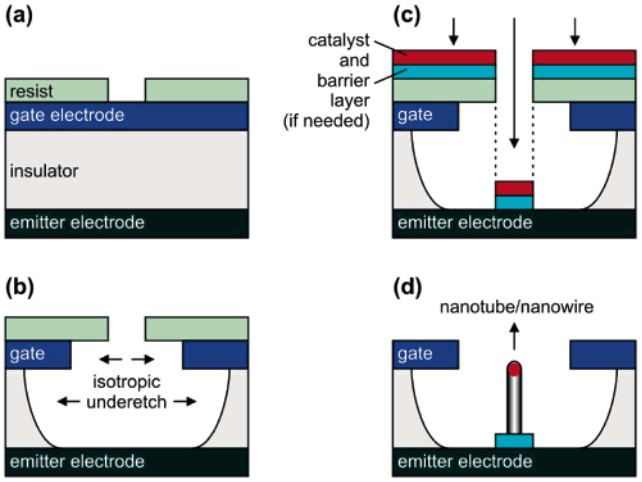

Figure 1. The self-aligned process for fabricating integrated gate, individual nanotube/nanowire cathodes. (a) A resist hole is first patterned on a gate electrode/insulator/emitter electrode sandwich. (b) The gate and insulator material are then isotropically etched. (c) A thin film of catalyst, and diffusion barrier (if required), are deposited on the structure. (d) A lift-off is then performed to remove the unwanted catalyst on top of the gate followed by the nanotube/nanowire growth inside the gate cavity.

or emission properties for an array of such emitters has been reported. In nanowire literature, the fabrication of vertical silicon nanowire arrays has been achieved,[21] but the integration of nanowires into a cathode has not yet been demonstrated. Hence, it is the aim of this work to show the direct integration of arrays of ideal, whisker-shaped, emitters of carbon nanotubes or silicon nanowires into gated cathodes using a simple self-aligned process that is technologically scalable.

The self-aligned process, for the carbon nanotube cathode, begins with the fabrication of a sandwich structure containing gate electrode (250 nm n-doped polysilicon), on insulator (1 μm silicon dioxide), on emitter electrode (100 nm TiW/Mo/TiW metal). An array of 300 nm diameter holes (20 000 in total), with a pitch of 5 μm, is then patterned using e-beam lithography (Figure 1a showing a single resist hole) on top of the sandwich. A reactive ion etching step using SF_6 gas at 40 mTorr is used to isotropically etch the polysilicon gate to form an 800 nm aperture. The silicon dioxide insulator is then isotropically etched in buffered hydrofluoric acid (Figure 1b). Both gate and insulator are overetched to produce an undercut so as to prevent emitters from touching the gate and the silicon dioxide from being charged during field emission. A 15 nm thick conductive TiN layer is then deposited by sputtering, followed by 7 nm of Ni, which acts as a catalyst for carbon nanotube growth (Figure 1c). The role of the TiN is to prevent Ni diffusion into the back metal electrode during carbon nanotube growth. It must be pointed out that the resist hole defines the gate, insulator, and emitter position and thus these features are "self-aligned". The unwanted TiN and Ni over the gate are then removed by lifting off the e-beam resist. Carbon nanotubes are then grown by PECVD using a mixture of C_2H_2 and NH_3 (54:200 sccm, respectively) at 5 mbar, 675 °C, with −600 V sample bias (Figure 1d). This process typically produces

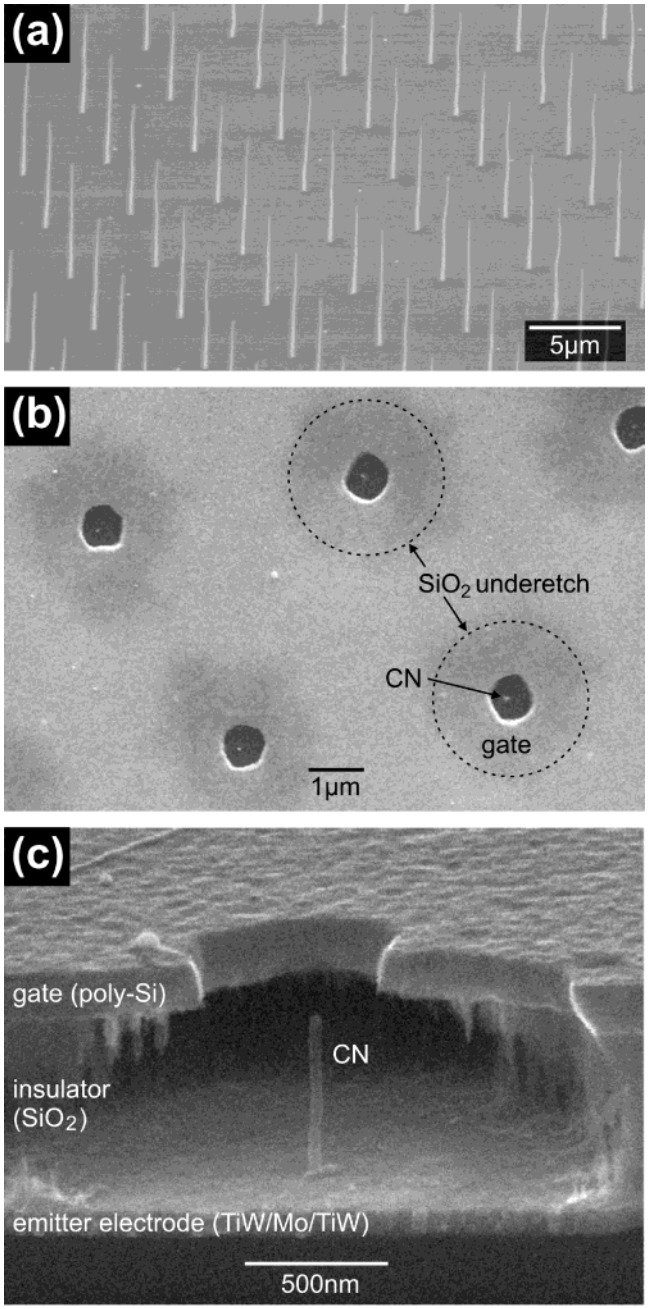

Figure 2. (a) Array of carbon nanotubes, with 5 μm pitch, deposited by PECVD of C_2H_2:NH_3 at 675 °C for 15 min. (b) Top view of the integrated gate carbon nanotube cathode. The pitch of the gate apertures is 5 μm. The nanotube appears as a bright dot in each gate aperture. The dark contrast around the gate (within the dotted circle) arises from absence of the underlying SiO_2 insulator which has isotropically underetched. (c) Cross section SEM view of the integrated gate carbon nanotube cathode, showing the gate electrode, insulator, emitter electrode, and vertically standing nanotube (CN). The isotropic etching of the gate and the insulator prevent short circuits between the gate and emitter.

straight, vertically aligned carbon nanotubes (Figure 2a, deposition time 15 min). Structurally, these nanotubes have multiple graphitic walls (20−40) but are not completely hollow and have bamboo-like periodic closures along the stem[11] and hence are also termed multiwalled carbon nanofibers in the literature. Figures 2b and c show the carbon nanotubes selectively grown inside the self-aligned gated

structure (deposition time 3 min). The deposition time was chosen to grow carbon nanotubes with their apex approximately equal in height to the extraction gate (i.e., 1 μm) as this is the optimal configuration for gated cathodes.[22]

The number of carbon nanotubes per aperture depends directly on the Ni catalyst dot size, and previous work has shown that 7 nm thick Ni dots from 100 to 300 nm have a single nanotube yield of 100%−88%, respectively,[11] The single nanotube yield decreases as the Ni dot size increases because the probability of a Ni cluster splitting to form multiple nanotubes is higher for larger clusters. Note also in the self-aligned process, both the TiN diffusion barrier (under the catalyst) and the Ni catalyst are patterned simultaneously. The nanotube can be formed only on the TiN diffusion barrier since any Ni outside the TiN area would alloy with Ti/W electrode, which yields no nanotube growth. This means that the nanotube will essentially be confined within the patterned diffusion barrier. As a 300 nm diameter resist hole is used here, the maximum misalignment within the diffusion barrier area is thus ±150 nm. Figure 2c shows the tilted view of a carbon nanotube nanocathode after growth. One can see that the individual nanotubes are well centered with respect to the gate aperture. Statistical study over 100 emitters on the sample showed that individual growth occurred in 90% of the apertures (cf. 88% obtained for individual growth from 300 nm dots on flat surfaces[11]) with the remaining 10% of the apertures containing double/multiple nanotubes. Furthermore, the maximum misalignment between gate and emitter did not exceed the expected 150 nm for 80% of the emitters (Figure 2b). Key advantages of this process are that no post-processing of the emitters is required and that the carbon nanotubes inside the gated cathode are essentially identical to those grown on a flat substrate.

To realize the gated device integrating silicon nanowires, essentially the same self-aligned procedure is performed, except the emitter electrode is now silicon ⟨111⟩ substrate (cf. TiW/Mo/TiW for nanotube cathode), 50 nm thick gold dots are used as the catalyst (cf. TiN/Ni for nanotube cathode), and no diffusion barrier layer is needed. After the self-aligned process, the silicon nanowires are grown by the vapor−liquid−solid method[10] using a mixture of SiH_4 and HCl (40:600 sccm, respectively) in 100 L/min H_2 flow, at 800 °C and 1000 mbar. Figure 3a shows an array of silicon whiskers from the growth process (deposition time 4 min). This process produces vertically aligned arrays of silicon nanowires that are relatively homogeneous in terms of height and diameter but, as our current growth conditions are not fully optimized yet, some wires exhibit kinks due to a crystallographic change in direction during growth. As demonstrated in Figure 3b, this self-aligned process is indeed capable of producing integrated gate silicon nanowire-based cathodes (deposition time 1 min) with also a good uniformity in height and diameter. Although a large proportion of these integrated gate cathodes contain a single nanowire, some kinked nanowires are seen to short circuit the gate and instances of multiple nanowires per gate aperture have been

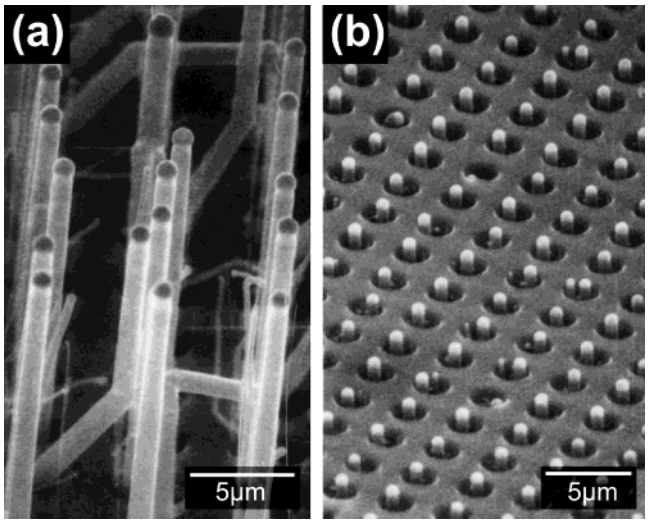

Figure 3. (a) Array of silicon nanowires, with 5 μm pitch, deposited by CVD of SiH_4:HCl:H_2 at 800 °C. (b) Array of integrated gate silicon nanowire cathodes fabricated using the self-aligned process.

observed. As our current nanowire process does not use any dopant gases, the silicon nanowires deposited were intrinsic/nonconductive and thus were not suitable for further electrical characterization.

Using a scanning anode field emission microscope (SAFEM), field emission measurements were performed on an integrated gate carbon nanotube cathode containing 100 × 100 apertures with 5 μm pitch. As shown in Figure 4, the gate electrode was grounded and, during field emission, the emitter electrode was driven negatively using a dc voltage (V_G) to extract electrons from the carbon nanotube emitters. A 250 μm diameter Pt−Ir scanning probe ball, attached to a 5-degree of liberty (X,Y,Z,θ,ϕ) piezo-driven mechanical displacement system, was moved 100 μm directly above the gated array and biased at a constant +100 V dc to provide a small external field (1 V/μm) to collect the emitted electrons (measured as anode current, I_A). The base pressure of the analysis chamber was 10^{-8} to 10^{-9} Torr. Further details on performing emission measurements using this scanning probe ball system is described in ref 23. As shown in Figure 5a, the initial turn-on voltage (the V_G required to produce 1 nA detectable emission at the anode) was 8 V; however, this characteristic showed current saturation (∼1 μA) at ∼50 V. This characteristic is typical for emitters that have surface adsorbates present at their tips. Field emission with an adsorbate-covered emitter begins at small localized areas that have the smallest work function or through adsorbates' resonant tunneling states as discussed by Dean et al.[24] and Bonard et al.,[25] hence giving rise to the low turn-on voltage. During field emission, these adsorbates constantly rearrange themselves due to electric field-driven surface diffusion which cause current instability, as is observed in the $I-V$ characteristics of Figure 5a. The emission current saturates as these adsorbates do not support high current emission. By applying further $I-V$ cycles at a maximum of 90 V applied/10 μA drawn, these surface adsorbates are field evaporated and the measurements exhibit stable, classical

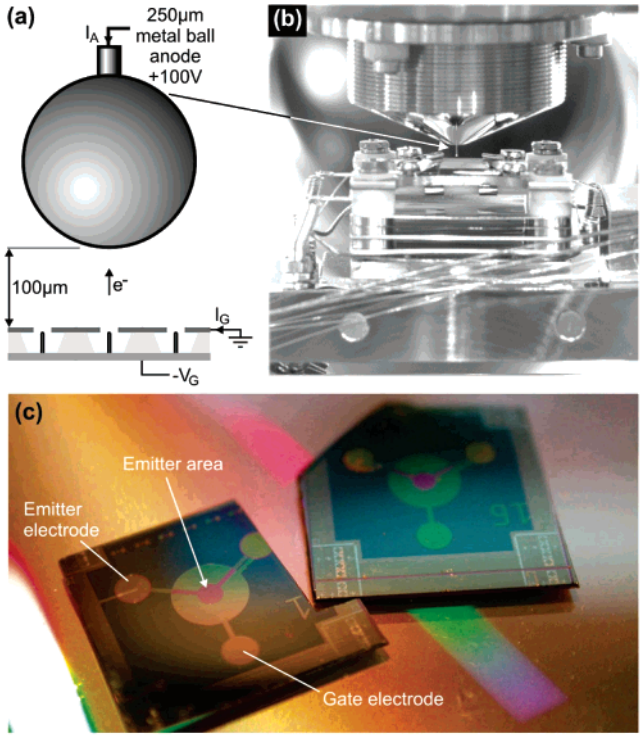

Figure 4. Field emission measurement apparatus. (a) Schematic of the system showing the electrical connections and the measured/varied quantities in the experiment. On the cathode, the gate electrode is grounded and the emitter electrode is varied negatively (0−90 V dc). A ball shaped anode, positioned directly above the integrated gate carbon nanotube cathode, is biased positively to generate a small, attractive field to collect emitted electrons and measure them as the anode current. (b) Photograph of the apparatus showing the ball shape anode directly above the cathode. (c) Photograph of two integrated gate carbon nanotube cathodes, fabricated on 10 × 10 mm silicon chips, with the active emitting area in the center.

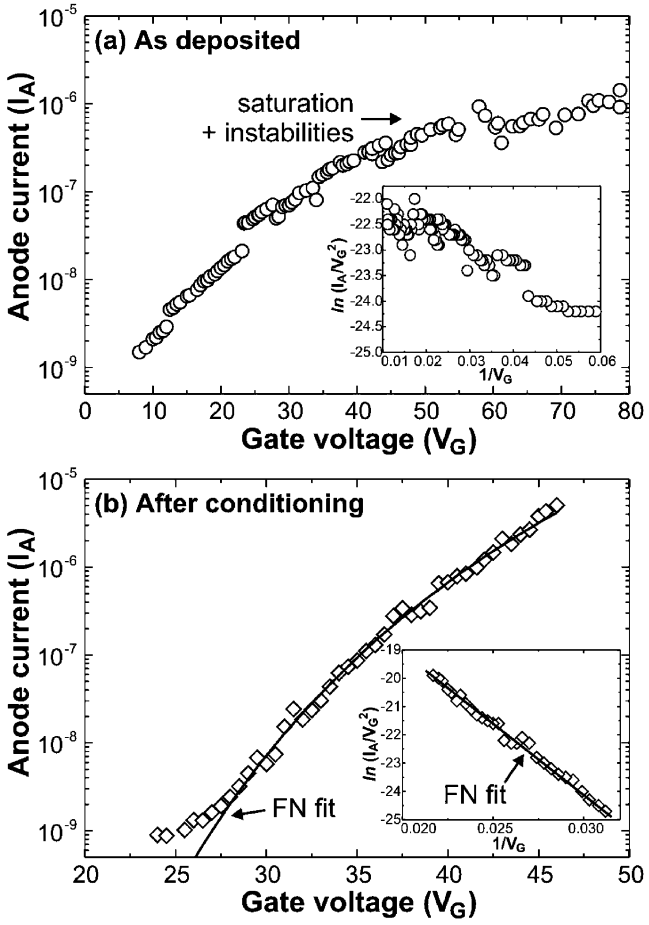

Figure 5. (a) Field emission measurements of the as-deposited integrated gate carbon nanotube cathode. A very low turn-on voltage is observed (8 V) but the current exhibits saturation and instabilities at high voltages. Such characteristics are indicative of emitters affected by adsorbates as discussed in the text. The inset shows the $I-V$ curve plotted in Fowler−Nordheim coordinates, but no fit can be derived from adsorbate-affected emission characteristics. (b) After several $I-V$ cycles, the adsorbates on the emitters have been field evaporated and the cathode has a stable characteristic with a turn-on of 25 V and a maximum current of 5 μA at 46 V. As shown in the inset, the $I-V$ characteristic can be well fitted to a straight line in Fowler−Nordheim coordinates, indicating classical Fowler−Nordheim field emission behavior.

Fowler−Nordheim field emission behavior with a turn-on at 25 V and peak current of 5 μA at 46 V applied (Figure 5b). The measured gate current (I_G) at 40−50 V gate voltage was only 40 nA; this corresponds to a gate transparency of ~99%.

To obtain the straight Fowler−Nordheim fit shown in the inset of Figure 5b, we used the modified Fowler−Nordheim equation developed by Spindt and Brodie to describe gated cathodes,[26] $I = aV^2 \exp(-b/V)$, with $a = 6 \times 10^{-5}$ Amps V^{-2} and $b = 475$ V. Using the relation $b = 6.44 \times 10^7/\gamma\phi^{1.5}$ and assuming a work function ϕ of 4.9 eV[27] for multiwall nanotubes, the geometrical field forming factor of the cathode, γ, is determined to be 1.47×10^6 cm^{-1} (= 147 μm^{-1}). This value is comparable to other types of integrated gate cathodes[26] and physically means that for every 1 V applied to the gate, the apex of the emitter experiences a local electric field of 147 V/μm. It is this large geometrical field forming factor that enables electron emission at low gate voltages; this allows lower complexity/cost driver electronics to be used for modulating the electron beam in applications.

In conclusion, we have fabricated and tested a gated array of individual carbon nanotubes. Using 300 nm lithography for the carbon nanotube process, the emitter misalignment to the central axis was below 150 nm for 80% of the emitters. A low turn-on voltage of 25 V and a peak current of 5 μA at 46 V were measured for a carbon nanotube gated cathode (10 000 apertures). The self-aligned process was also used to integrate silicon nanowires into a gated structure. Thus, the self-aligned process presented here is flexible and indeed can be generalized and applied to new and emerging whisker-like nanomaterials (e.g., ZnO, InP) to construct low-voltage gated cathodes. Note that the self-aligned process essentially uses an array of holes in resist, which can be relatively easily fabricated on a large scale today using either nanoimprint[28] or laser interferometry.[29] Coupling these lithography techniques with conventional etching processes for forming the gate aperture, sputter deposition for catalyst deposition, and chemical vapor deposition processes for nanotube/nanowire deposition, this self-aligned process is indeed promising for

wafer/large-scale manufacturing of low-voltage individual nanotube/nanowire electron sources.

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