Nanoscale memory cell based on a nanoelectromechanical switched capacitor

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The demand for increased information storage densities has pushed silicon technology to its limits and led to a focus on research on novel materials and device structures, such as magnetoresistive random access memory[1–3] and carbon nanotube field-effect transistors[4–9], for ultra-large-scale integrated memory[10]. Electromechanical devices are suitable for memory applications because of their excellent 'ON–OFF' ratios and fast switching characteristics, but they involve larger cells and more complex fabrication processes than silicon-based arrangements[11–13]. Nanoelectromechanical devices based on carbon nanotubes have been reported previously[14–17], but it is still not possible to control the number and spatial location of nanotubes over large areas with the precision needed for the production of integrated circuits. Here we report a novel nanoelectromechanical switched capacitor structure based on vertically aligned multiwalled carbon nanotubes in which the mechanical movement of a nanotube relative to a carbon nanotube based capacitor defines 'ON' and 'OFF' states. The carbon nanotubes are grown with controlled dimensions at pre-defined locations on a silicon substrate in a process that could be made compatible with existing silicon technology, and the vertical orientation allows for a significant decrease in cell area over conventional devices. We have written data to the structure and it should be possible to read data with standard dynamic random access memory sensing circuitry. Simulations suggest that the use of high-*k* dielectrics in the capacitors will increase the capacitance to the levels needed for dynamic random access memory applications.

We consider a nanoelectromechanical (NEM) device consisting of a source, a drain and a gate electrode (Fig. 1). A vertically aligned multiwalled carbon nanotube (MWCNT) with a diameter of ~60 nm was grown from the source electrode and was coated with a dielectric layer (~40 nm of SiN_x) and a metal layer (~30 nm of Cr) to form a CNT–insulator–metal (CIM) capacitor with a diameter of ~200 nm. This CIM structure is similar to the stacked capacitor structures formed around silicon pillars in traditional high-density dynamic random access memory (DRAM)[18,19]. The MWCNT grown on the drain electrode is the mechanically active element of the cell; electrostatic forces cause it to bend and make contact with the CIM structure on the source. (Note, there is no nanotube on the gate electrode.) A selective CNT growth process[20,21] allows the electrode for the capacitor and the mechanical element (which both have high aspect ratios) to be fabricated in one step, thus avoiding the demanding etching processes needed to scale silicon nanopillar structures to below 100 nm.

In operation, the source is electrically connected to ground, the drain is connected to the bit line, which has a constant positive voltage applied to it, and the gate is connected to the word line. When this word line is positively biased (to a value higher than the bit line voltage), the nanotube on the drain experiences a repulsive electrostatic force from the gate electrode and an attractive electrostatic force from the source electrode, causing it to deflect until it makes contact with the metal electrode on the capacitor (Fig. 1c). On contact, a transient current flows to charge the CIM capacitor. This charge is used to represent a bit of stored information. When the gate bias is removed, the electrostatic force giving rise to the deflection of the drain MWCNT is also removed, and the nanotube springs back to the non-contact 'OFF' position. The length of the drain nanotube and the source–drain and drain–gate separations have to be chosen carefully to ensure that the switch works as intended (see Methods).

The switching characteristics of the device are shown in Fig. 2. It can be seen that the current between the source and the drain increases sharply above the threshold voltage and becomes saturated. This very sharp sub-threshold slope means that a very small difference in bias can switch between 'ON' or 'OFF' states, which leads to low power consumption. This is a major advantage of the NEM switch compared to a Si nanotransistor, where the sub-threshold slope is limited and the leakage current in the 'OFF' state is high. The switching speed, which is limited by the natural oscillating frequency of the nanotube on the drain, is estimated to be in the range 62–750 MHz (see Methods). This implies that the switching speed of a NEM-based DRAM cell in a practical memory is likely to be limited by the parasitic resistances and capacitances in the connecting tracks and contacts, rather than the NEM switch itself.

The electrical characteristics of the CIM capacitor were estimated through the fabrication of 40,000 CIM structures

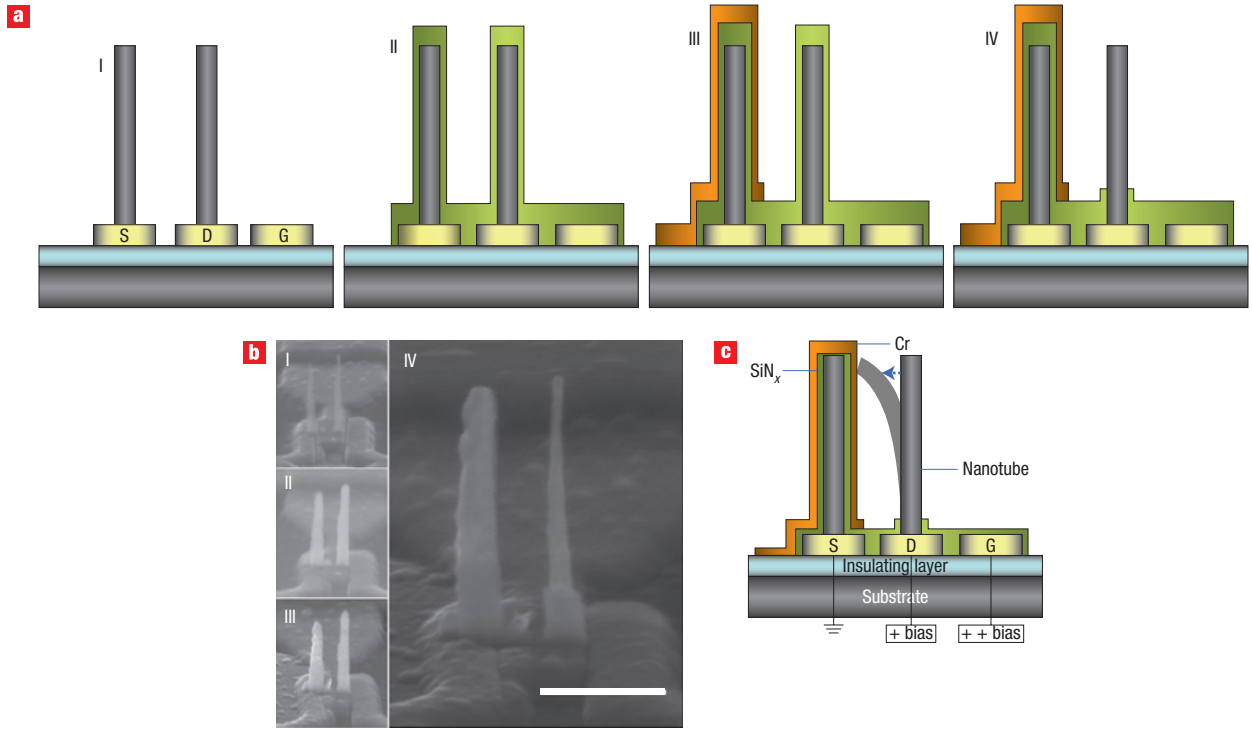

Figure 1 A NEM switch based on vertically aligned multiwalled carbon nanotubes. Schematic diagram (**a**) and scanning electron micrographs (**b**) showing the fabrication process (see main text and Methods). Source S is connected to ground, and the drain D and gate G are connected to the bit line and the word line, respectively, to receive electrical signals. The substrate is Si and the insulating layer is SiO_2 (300 nm thick). Nb is used for the source, drain and gate electrodes and access lines. The nanotube (grey) in the capacitor (on the left) has diameter ~60 nm, the dielectric layer (green) is ~40 nm thick, and the metal layer (orange) is ~30 nm thick. The diameter of the capacitor structure is 200 nm and the scale bar in the micrograph corresponds to 500 nm. **c**, When positive bias voltages are applied to the drain and gate, electrostatic forces act to deflect the nanotube on the drain to make contact with the top metal of the capacitor on the source, causing it become charged. On removal of the gate bias voltage, if the combined electrostatic and van der Waals forces acting on the drain nanotube are weaker than the elastostatic force pulling it to the vertical, it will spring back to its original position, as shown in **b**, IV, leaving the nanoscale capacitor on the source in a charged state.

(CNT diameter, ~70 nm; length, ~3.5 μm; SiN_x, ~65 nm). The total capacitance of this array was approximately 42 pF, giving an estimated capacitance 1.05 fF for a single CIM structure[22], which is in good agreement with theoretical estimates (see Methods). This result also indicates indirectly that there is no detrimental interaction between the MWCNT electrode and the insulator layer.

Applying the same model for the capacitance in the NEM-DRAM cell (Fig. 1b), which differs slightly from those just described (CNT diameter, ~60 nm; length, ~1.6 μm; SiN_x, ~40 nm), gives a value of 0.59 fF, which would give an available potential of 2.4 mV for bit line sensing in a conventional DRAM design[23]. However, the minimum acceptable values of capacitance and bias difference for gigabit-level DRAMs are ~10–15 fF and ~60–80 mV, respectively[18,24]. It could be possible to reach these values in the NEM-DRAM cell by replacing the SiN_x dielectric layer with ultra-thin (~10 nm) layers of high-k dielectric materials such as Ta_2O_5, $SrTiO_3$ or $(Ba,Sr)TiO_3$ (refs 24, 25). The use of these materials is already being actively pursued in the development of Si-based gigabit-level DRAM.

Because the leakage current of the NEM switch is very low, the refresh time depends mainly on the leakage current of the cell capacitor, which is 6.2 fA at 1 V. However, any estimate of a practical refresh time should be based on the use of a high-k dielectric. The overall working speed of a NEM-based memory cell would be determined mainly by the RC delay due to the capacitances of the cell and bit line, similar to a conventional DRAM. For a cell capacitance of 10 fF, the RC time delay would be 10 ns.

The performance of the NEM memory structure with varying drain and gate bias conditions is shown in Fig. 3. The parallel loading of the cell introduced by the measurement system is of the order of pF, compared with a capacitance of 0.59 fF for the CIM structure, which makes it impossible to detect switching by observing an increase in cell capacitance. To solve this problem the metal layer was extended over the adjacent SiO_2 substrate to increase the capacitance of the CIM structure. Figure 3 therefore shows the switching of this augmented capacitor (which has a capacitance of the order of pF).

There is no capacitance change below 70 mV drain voltage with 20 V gate bias. When the drain bias is increased above the threshold voltage (70 mV), the nanotube on the drain makes contact with the capacitor, causing a sharp change in measured capacitance (Fig. 3a). Contact effectively removes the low air-gap capacitance existing in series between the drain and source before contact. Therefore, the drain bias determines the stored charge on the capacitor for a defined positive gate voltage, in the same way as the bias of the bit line determines if a '0' or a '1' is stored in a traditional Si-based DRAM cell. The change in capacitance also corresponds well to the pulsing of the gate voltage between 20 V and 0 V at 100 mV drain voltage, as shown in Fig. 3b.

The results in Fig. 3 mimic a 'write' operation. In other words, if the bit line is positively biased with respect to the source, and

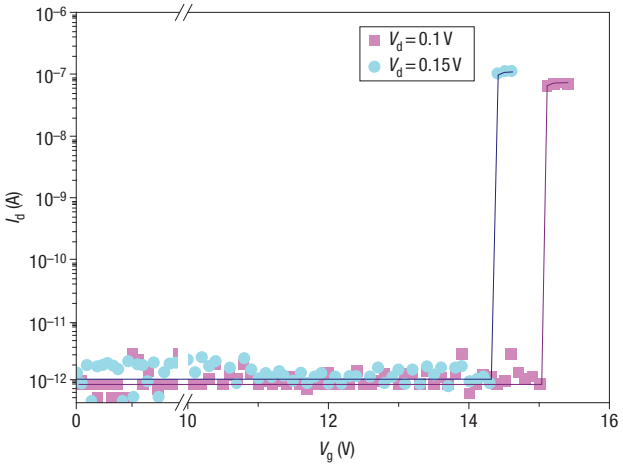

Figure 2 NEM switching characteristics. The current between the source and drain, I_d, as a function of V_g, the voltage between the gate and drain, for two values of V_d, the voltage between the drain and the source (with the source electrode connected to ground). Below a threshold gate voltage, I_d is effectively zero. This is the 'OFF' state of the NEM switch. At the threshold gate voltage, the electrostatic force acting on the nanotube is strong enough to bend it to such an extent that it makes contact with the capacitor, which allows current to flow between the drain and the source. This is the 'ON' state of the NEM switch. The threshold voltage depends on V_d.

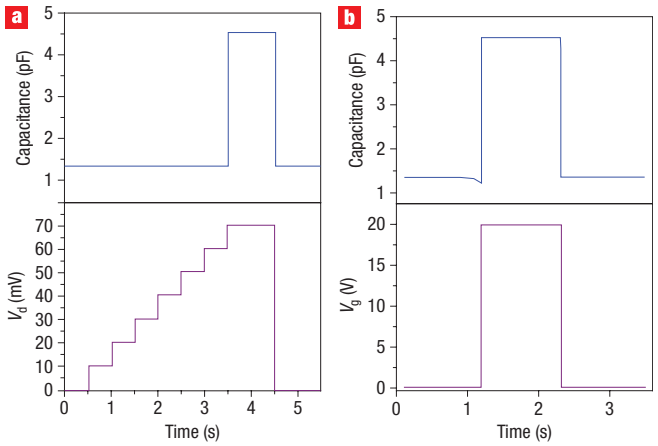

Figure 3 The capacitance of a NEM switch. a, For $V_g = 20$ V, the capacitance between the source and drain (top) increases significantly (to the value of the effective DRAM capacitor) when V_d reaches 70 mV (bottom) and the nanotube makes contact with the source. The capacitance drops again when V_d is reduced. **b**, When V_g is pulsed between 0 V and 20 V (bottom), with $V_d = 0.1$ V, the capacitance between the source and drain follows a similar pattern (top).

the word line is positively biased with respect to the bit line, the nanotube on the drain will deflect and make contact with the capacitor, allowing charge to accumulate on the capacitor, thus writing a '1' or 'ON' state. This process may be propagated through the cells in a memory array to store data (Fig. 4a). In the present experiments it was not possible to mimic a read operation because there were no sensing circuits. However, the read process is similar to that used for conventional DRAM (Fig. 4b). As the read process leaves all the capacitors fully charged (that is, in the 'ON' state), they must be discharged (that is, reset to the 'OFF' state) before re-writing. This can be done by connecting the outer electrode of the capacitor to ground through a switch or transistor after reading.

Computer simulations of the potential distributions in the structure are shown in Fig. 4c–e. If the capacitor is uncharged ('OFF'), there is a potential gradient between the capacitor and the nanotube (Fig. 4c), and the nanotube is pulled towards the capacitor by an electrostatic force until it makes contact (Fig. 4d) with the capacitor metal. When the capacitor is charged to the same potential as the drain, the potential distribution exists across the capacitor dielectric, rather than between the outer electrode of the capacitor and the nanotube on the drain (Fig. 4e). Although the nanotube still deflects to reduce the energy density of the field between the gate and the drain, there is no contact. However, if charge leaks from the capacitor, there can be contact. If this happens, the leakage current should be kept small enough so that the sensing circuitry can distinguish between the 'ON' and 'OFF' states. Refresh cycles can be carried out to avoid this, as occurs in conventional DRAM.

The device reported here differs in important ways from previous proposals for CNT-based memory in that a single growth step allows for deterministic height and population control with defined spatial positioning of the MWCNTs. Previous proposals[15] involve lateral rather than vertical growth, but various technical obstacles remain, such as placing defined numbers of nanotubes at selected locations and achieving *in situ* deterministic growth of crossed nanotubes[5,26]. Arrays of vertically grown MWCNTs on Si wafers have demonstrated nominal heights of 2 μm and diameters of 50 nm controlled to within standard deviations of 6.3% and 4.1%, respectively[21]. The growth temperature used in this work (~600–650 °C) is too high for integration with CMOS technology, but it should be possible to reduce this to ~350–400 °C, which would make it compatible with standard CMOS (ref. 27). Moreover, due to the three-terminal structure of the device, the bias between source and drain can be changed, allowing for more flexible electromechanical drive conditions as well as random access. Furthermore, the mechanical switching approach means that the ultra-shallow n- or p-type junctions and thin-gate dielectrics associated with nanoscale Si transistors are not required. This removes the requirement for the complicated processing steps, high material purity and low contamination levels associated with Si-based DRAM cells.

We have demonstrated a viable structure and fabrication process for a NEM memory cell for ultra-large-scale integrated memory applications. The proposed write–read scheme is similar to that of a conventional DRAM, so conventional sensing schemes and CMOS circuits could be used, while taking advantage of the vertical nature of the NEM capacitor structure to achieve high integration densities.

METHODS

EXPERIMENTAL

Vertically grown MWCNTs were used as the switch element and as the bottom electrode of the capacitor (Fig. 1). The nanotubes (diameter ~60 nm) were vertically grown at ~600–650 °C, using a C_2H_2 and NH_3 gas mixture, from the Ni catalyst dots using a direct-current plasma-enhanced chemical vapour deposition system (PECVD). The single MWCNT growth step allows for deterministic control of the height, number and spatial positioning of the

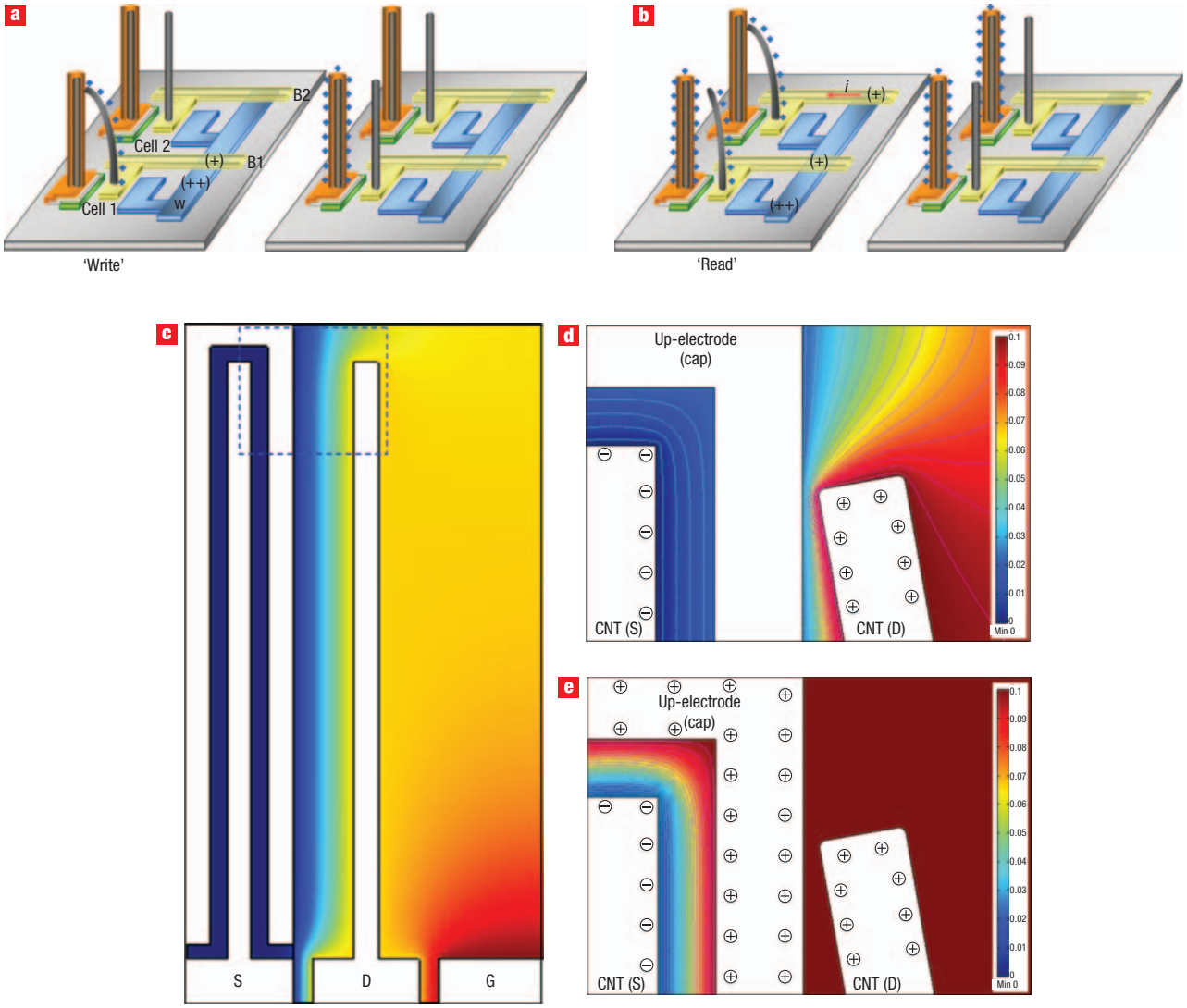

Figure 4 Writing and reading data to a NEM memory cell. a, Data is written through the voltage levels of the bit lines (the yellow lines B1 and B2) and the word lines (blue). If a bit line for a particular cell has the correct bias voltage, the nanotube (grey) in that cell deflects and makes contact with the capacitor (orange and purple), allowing charge to accumulate on the latter. When the write voltage is removed, the nanotube returns to a vertical position. Cell 1 now stores a '1' and cell 2 stores a '0'. **b**, To read data the same bias voltage that was used to write the data to cell 1 is applied to both bit lines. The mutual repulsion between the positive charges on the capacitor and the nanotube in cell 1 prevents the nanotube from making contact with the capacitor, so no current flows, unlike the situation in cell 2, where the nanotube does make contact with the cell. This current difference is used to read the data. After the read process, the capacitors in both cells have accumulated charge, and must therefore be reset to '0' to allow further data to be written. **c**, Details of the potential distribution when the nanotube on the drain is in the upright position and the capacitor is in a '0' state (that is, it contains no charge). Regions of high potential are shown in red (see colour bar). The gap between the nanotube and capacitor is 100 nm: $V_S = 0$ V, $V_D = 0.1$ V, $V_G = 15$ V. **d**,**e**, Detail of the area within the blue dotted rectangle in **c** (with the drain nanotube tip positioned 10 nm from the capacitor). When a voltage is applied to the nanotube (**d**), there is a potential gradient between the nanotube and the uncharged outer electrode of the capacitor. This potential gradient gives rise to an attractive electrostatic force that pulls the nanotube into contact. However, when the capacitor is charged (**e**), there is no potential gradient between the capacitor and the nanotube, and therefore no force to pull the latter into contact. Instead, the potential gradient is in the dielectric of the capacitor (that is, between the inner and outer electrodes).

MWCNTs. A detailed description of MWCNT growth by this technique can be found elsewhere[20,21]. Silicon nitride (SiN_x) was deposited by PECVD using a SiH_4 and NH_3 gas mixture; the dielectric constant of the film was 5.54 (Fig. 1a, II). After the electron beam lithography step, chromium (Cr) was deposited, first by sputtering and then by angular evaporation, to form the capacitor structure (Fig. 1a, III). The SiN_x deposited on the drain MWCNT was removed by a wet etching process after coating with 200 nm PMMA and ashing (Fig. 1a, IV). The SiN_x remaining at the bottom of the MWCNT enhances the working reliability of the device by strengthening the interface between the MWCNT and the bottom electrode. The present success rate (in a university laboratory) of unit cell fabrication is about 50% (from about 50 unit cells). The main cause of failure is misalignment in the lithography process due to manual handling. The single MWCNT growth step at the selected site has a very high success rate (>95%).

CALCULATING THE FORCE ON THE DRAIN CNT

The repulsive force on the drain CNT can be viewed within the context of the increase in energy density of the field (proportional to the square of the electric flux density) in the gap between the gate electrode and the drain CNT. The electrostatic force will act to reduce the energy density in the field, $F_e = -(\partial W_e/\partial x) + V(\partial Q/\partial x)$, where F_e is the electrostatic force, W_e is the energy stored in the field, V is the voltage, Q is the charge, and x is the displacement parallel to F_e. The second term in the electrostatic force expression

is zero between two positively charged electrodes, as no charge of opposite polarity is induced by capacitive action (the balancing charge for both electrodes is from the earth electrode). In the electrostatic force acting between the source and the drain MWCNT, both terms are active, with the second being dominant (as in the case of a parallel plate capacitor). The combination of forces acts to deflect the drain MWCNT until it contacts the metal electrode on the source CIM capacitor. There is the possibility that van der Waals interaction between the drain MWCNT and the CIM structure after first contact would cause them to stick together even after the voltage bias giving rise to the deflecting electrostatic force is removed, effectively forming a permanent 'ON' state[14,15]. This can be avoided by controlling the MWCNT mechanical properties through straightforward optimization of the growth conditions to determine its length and diameter, thus ensuring that the drain MWCNT will return to its original position when the gate bias is removed. It can also be seen from Fig. 2 that increasing the drain bias lowers the threshold voltage of the device, as expected.

ESTIMATING THE SWITCHING SPEED

The switching speed, limited by the natural oscillating frequency of the MWCNT, can be estimated using the cylindrical cantilever model, $f = (1/\sqrt{2}\pi)(r/L^2)\sqrt{(E/\rho)}$, where E is Young's modulus, ρ is density, r is radius (30 nm), and L is length (1.6 μm)[15,17,28]. Using this model, with parameters set in a range typical for an MWCNT, a bandwidth limitation in the megahertz to gigahertz range is predicted. A range of values for Young's modulus (~1–1.2 TPa) and the density (~0.015–1.8 g cm^{-3}) are given in the literature, suggesting that the switching frequency can lie in the range 62–750 MHz .

CALCULATING THE CAPACITANCE

The capacitance of a single CIM structure was approximated by a cylindrical capacitor model, $C = 2\pi\varepsilon_0\varepsilon_r l/\ln(b/a)$, where ε_0 is permittivity in a vacuum, ε_r is the dielectric constant of SiN_x, l is nanotube length, a is nanotube diameter, and b is the coaxial diameter of the SiN_x. Using this model with $\varepsilon_0 = 8.85 \times 10^{-14}$ F cm^{-1}, $\varepsilon_r = 5.54$ (measured from a simple metal–insulator (SiN_x)–metal capacitor), $l \cong 3.5$ μm, $a = 70$ nm and $b = 200$ nm, the capacitance of one CIM structure is calculated to be 1.027 fF. This value is in very good agreement with the experimentally measured values.

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Author contributions

J.E.J. was involved in project conception, planning, experimental work and data analysis, S.N.C. in project conception, experimental work and data analysis, Y.J.C., T.B., D.J.K. and J.E. Jung in experimental work, D.G.H. in experimental guidance and direction, J.M.K. in project conception and data analysis, G.A.J.A. in project conception and guidance, data analysis and interpretation.

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