

Zinc oxide nanowire networks for macroelectronic devices

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(Received 6 January 2009; accepted 25 March 2009; published online 20 April 2009)

Highly transparent zinc oxide (ZnO) nanowire networks have been used as the active material in thin film transistors (TFTs) and complementary inverter devices. A systematic study on a range of networks of variable density and TFT channel length was performed. ZnO nanowire networks provide a less lithographically intense alternative to individual nanowire devices, are always semiconducting, and yield significantly higher mobilities than those achieved from currently used amorphous Si and organic TFTs. These results suggest that ZnO nanowire networks could be ideal for inexpensive large area electronics. © 2009 American Institute of Physics.

[DOI: 10.1063/1.3120561]

The large scale synthesis of wide ranging one-dimensional nanowires (NWs)/tubes with extraordinary properties are advancing optical and electronic devices.¹⁻⁸ The challenges of large scale integration of individual NWs/tubes has shifted the research focus to large area electronics based on ensemble of these materials which collectively yield sufficiently good device characteristics but can be fabricated by bottom up approaches such as transfer printing or stamping.⁹⁻¹⁵

Among semiconducting NWs, ZnO is promising for optoelectronic devices because of its direct wide bandgap of 3.37 eV (at 300 K) and a relatively large exciton binding energy of 60 meV. ZnO NWs can be readily synthesized using gas phase deposition¹⁶ or via hydrothermal route.¹⁷ Optoelectronic devices such as UV nanolasers,³ field effect transistors,¹⁸ solar cell electrodes,¹⁹ and piezoelectric nanogenerators⁵ utilizing ZnO NWs have been reported.

In addition to individual NW devices, networks of ZnO NWs grown at low temperatures through hydrothermal routes have shown promising thin film transistor (TFT) characteristics.^{20,21} The defective NWs led to high operating voltages in these devices and no information on the transparency of the active material was provided. Here, we report on a fabrication scheme for transparent ZnO NW networks that utilizes a less lithographically intense alternative to individual NW devices and demonstrate basic electronic devices with large channel lengths based on these networks.

Highly crystalline and high aspect ratio ZnO NWs were obtained on gold catalyzed silicon (100) substrates by the carbothermal reduction of ZnO powder at 950 °C.²² In order to achieve reproducible ZnO NW networks with a controllable density, we used contact printing method which involves bringing NW substrate in mechanical contact with a receiver substrate. Growth substrate consists of dense “lawn” of ZnO NWs and the receiver substrate is functionalized by poly-L-lysine.¹¹ For the stamping process, surface of both the receiving and the growth substrates were cleaned to en-

sure proper overlapping. The growth substrate was then placed on the receiver substrate at the desired location and a pressure of ~200 g/cm² was applied on the growth substrate. Transfer process was finalized by lifting the growth substrate without any shear on the receiver substrate. During contact, NWs are detached from the growth substrate and attached to the receiver substrate through van der Waals interactions. Size of the deposited network area can be controlled by the growth substrate. The yield of the transfer process is independent of the type of the receiver substrate used indicating sufficiently strong cohesive forces are present between the wires and the substrate.

All devices reported here utilized NW densities slightly below or above the percolation threshold. The control of the NW density can be achieved by consecutive stampings. NW density, corresponding to the number of stampings, has been calculated using imaging software. The role of percolation has been investigated in order to understand the transport mechanism in two-dimensional ZnO NW networks. Under the percolation theory, ZnO NWs are assumed as uniform sticks with random alignment. The percolation threshold is defined as the formation of long-range connectivity in random systems. The percolation threshold of ZnO NW network is given by $N_C = [(4.236/l)^2 / \pi]$ for random alignment.²³ The length (l) of the transferred NWs was ~6 μm, therefore, the percolation threshold of ZnO NW network is estimated to be around 0.16 NW/μm².

Planar TFTs were fabricated utilizing conventional photolithographical processes on top of the stamped NW networks on SiO₂/Si substrates. Niobium (Nb) source and drain contacts were sputtered, defining channel lengths ranging from 5 to 50 μm. The transfer characteristics for ZnO NW network TFTs with different channel lengths and the corresponding output characteristics of a 20 μm channel device are shown in Figs. 1(a) and 1(b), respectively, together with a photograph and SEM image of the devices [Fig. 1(c)]. TFTs exhibit n -channel depletion mode behavior; in agreement with the individual ZnO NW field-effect transistors (FETs) using gold catalyzed ZnO NWs with smooth surfaces.²⁴ The ON/OFF ratios ranged from 10³ to 10⁵, de-

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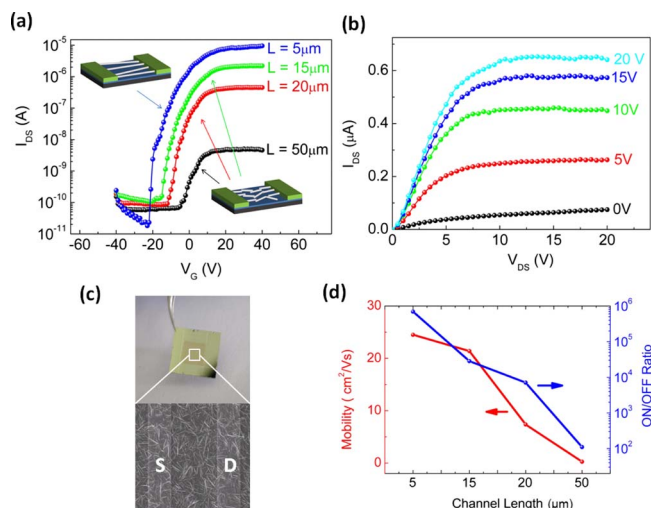


FIG. 1. (Color online) TFT devices based on ZnO NW networks. (a) Transfer characteristics for 5, 15, 20, and 50 μm channel devices ($V_{\text{DS}}=4$ V). 5 μm TFT device consists of arrays of ZnO NWs whereas others are networks as indicated by the schematics inside the figure. (b) Output characteristics of a 20 μm channel ZnO TFT. Gate voltages are marked on the curves. (c) Optical micrograph and SEM image of an actual device. The channel length is 20 μm . (d) Mobility and ON/OFF ratios of TFT devices with respect to the channel length. ZnO NW density is fixed to 0.25 $\text{NW}/\mu\text{m}^2$. All electrical measurements were performed at ambient dark conditions with an Agilent 4156B semiconductor parameter analyzer.

pending on the channel length. The highest ON/OFF ratios are comparable to that of reported best single walled carbon nanotube (SWNT) network devices.^{10,25} To investigate the effect of channel length, ZnO NW density was fixed (0.25 $\text{NW}/\mu\text{m}^2$) and channel lengths were varied from 5, 15, 20, and 50 μm . The effects of channel length on the mobility and the ON/OFF ratios are shown in Fig. 1(d). Considering average NW length, devices with 5 μm channels are arrays rather than networks. The ON current increases with decreasing channel length which may be attributed to the fact that for a given NW network, the number of active current paths between source and drain electrodes increases with decreasing channel length. Meanwhile, the OFF current is almost independent of the channel length (within the same order of magnitude). Thus, the increase of the ON/OFF ratio with the decrease in channel length, as shown in Fig. 1(d), is a result of increasing ON current due to smaller number of nodes in the current path. The mobility of the TFTs calculated from the linear regime of the transfer characteristics was found to be $\mu_{\text{eff}} \sim 25$ $\text{cm}^2/\text{V s}$ for the short channel devices and indeed increases with decreasing channel length, as shown in Fig. 1(d).²⁶ This is due to the increase in channel conductivity with reduced number of nodes in a ZnO NW path. It is worth emphasizing that the mobilities of our ZnO NW TFTs are significantly larger than or comparable to those of organic and a-Si TFTs (<1 $\text{cm}^2/\text{V s}$) even for very long channels. The mobilities are also of the same order as those for nonaligned SWNT networks.²⁷ In particular, the mobility of NW TFTs with a channel length of 20 μm is at least an order of magnitude higher than that of previous ZnO NW TFTs presented by Sun and Sirringhaus²⁰ and Ko *et al.*²¹ The original value for channel width defined by Nb was 100 μm ; however, for mobility calculations effective channel width was taken into account. Effective channel width was estimated as the product of the average of the NW diameter and the number of NWs on the source and drain contacts. For

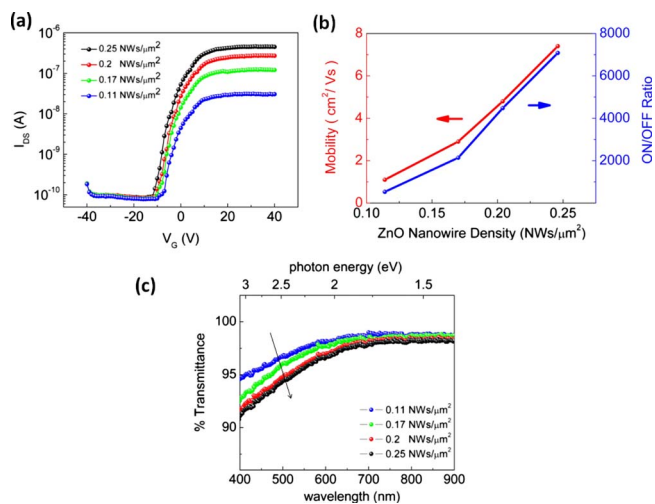


FIG. 2. (Color online) Effect of NW density on the properties of TFT devices. (a) Transfer characteristics for different NW densities of 0.11, 0.17, 0.2, 0.25 $\text{NWs}/\mu\text{m}^2$ for 20 μm channel devices ($V_{\text{DS}}=4$ V). (b) Mobility and ON/OFF ratio of TFT devices with respect to the ZnO NW density in the network. TFT channel length is fixed to 20 μm . (c) Transmittance as a function of wavelength (photon energy) for the different density ZnO NW networks.

comparison, the mobility for the 20 μm channel length ZnO network TFT was 0.59 $\text{cm}^2/\text{V s}$ when the actual width of the channel was taken into account, and 7.4 $\text{cm}^2/\text{V s}$ when effective channel width was used. This indicates that NW nodes are effective in means of charge transport, and highly aligned ZnO NW networks would yield better device performance.

In order to investigate the effect of NW density, channel length was fixed to 20 μm and devices with NW network densities ranging from 0.11, 0.17, 0.2, and 0.25 $\text{NW}/\mu\text{m}^2$ were fabricated. The transfer characteristics for ZnO NW network TFTs and the corresponding ON/OFF ratios and mobility values with different NW densities are shown in Figs. 2(a) and 2(b), respectively. It can be seen in Fig. 2(b) that both the mobility and the ON/OFF ratios increase with the NW density. Higher ON currents for the TFTs are required for a number of applications such as display drivers and microwave circuits. The ON current was found to scale linearly [Fig. 2(a)] with the NW density, keeping the OFF current level almost constant which clearly demonstrates the uniformity and reproducibility of the ZnO NW network TFTs.

NW networks are also highly transparent. The normal incidence transmittance between 1.5–4 eV photon energy with the substrate absorption removed is shown in Fig. 2(c). Transmittance shows a monotonous decrease with increasing photon energy in the measured regime as shown in the figure. NW network densities yielded transmittance values in excess of 95%, scaling almost linearly with NW density, suggesting that the losses due to overlapping NWs is negligible.

To investigate the viability of a fully functioning network inverter device, we have connected SWNT and ZnO NWs in series as *p*-type and *n*-type network TFTs. SWNT networks were prepared using the vacuum filtration method.²⁸ We have used a SWNT concentration which is well below the percolation threshold of the metallic SWNTs. Gold source and drain electrodes were deposited using thermal evaporation. SWNT network TFT used in the inverter device exhibits *p*-type gate transfer and output characteristics as shown in Figs. 3(a) and 3(b). The ON state current of the

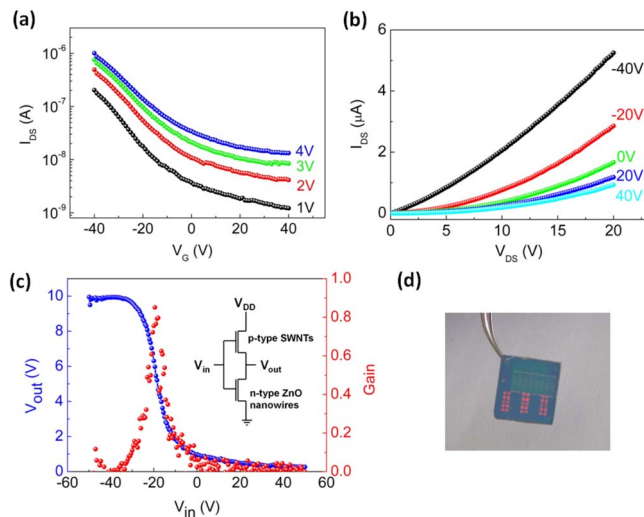


FIG. 3. (Color online) Electrical characteristics of a TFT complementary inverter. (a) Transfer and (b) output characteristics for a $20\ \mu\text{m}$ channel SWNT network TFT. Drain-source voltages and gate voltages are marked on the curves, respectively. (c) Transfer characteristics of a back gated CMOS inverter fabricated by connecting *p*-type SWNT TFT with *n*-type ZnO NW TFT in the back gate geometry ($V_{\text{DD}}=10\ \text{V}$). Inset is the schematic of the CMOS inverter. (d) Optical micrograph of an actual device where Nb contacts of ZnO TFTs are overlapping Au contacts of SWNT TFTs.

device at ambient conditions and under a drain-source voltage of $V_{\text{DS}}=-4\ \text{V}$ was measured to be $I_{\text{ON}}=1.04\times 10^{-6}\ \text{A}$, whereas OFF state current was $I_{\text{OFF}}=1.17\times 10^{-9}\ \text{A}$. This yields ON/OFF ratios of about 10^3 with a threshold voltage of $V_{\text{th}}=-15\ \text{V}$. Using Fig. 3(a), the slope of the source drain current as a function of the gate voltage was measured in the linear region and the field effect mobility is estimated to be $\mu_{\text{eff}}=0.43\ \text{cm}^2/\text{V s}$.

Figure 3(c) shows transfer characteristics of the complementary inverter with a channel length of $20\ \mu\text{m}$ for both SWNTs and ZnO TFTs, with the photograph of the devices [Fig. 3(d)]. A schematic of the inverter is shown in the inset. A $10\ \text{V}$ bias was applied to the V_{DD} terminal and the input voltage of the inverter was applied to the common back gate of both SWNT and ZnO NW TFTs. The output voltage of the inverter was obtained from the common drain terminal. When the input voltage is lower than $-30\ \text{V}$, the *p*-type SWNT TFT is ON, conductance is high, and the *n*-type ZnO NW TFT is OFF, the conductance is low. As a result, the output of the inverter is close to V_{DD} ($10\ \text{V}$). As the input voltage is increased, the conductance of the *p*-type SWNT TFT decreases and the conductance of the *n*-type ZnO NW TFT increases, leading to a decrease in the output voltage. With sufficiently high input voltage ($>10\ \text{V}$), the *p*-type SWNT TFT is turned OFF, and the *n*-type ZnO NW TFT is ON. The combined effect is an output voltage close to the ground ($0\ \text{V}$), as clearly shown in our experiment. Our results show that the output starts to decrease at $V_{\text{in}}=-30\ \text{V}$ and is cutoff at $V_{\text{in}}=10\ \text{V}$, leading to a gain of ~ 1 .

In summary, we have deposited high temperature grown ZnO NWs onto receiver substrates at room temperature in the form of semiconducting random networks. We have fabricated TFTs and complementary inverter devices based on these networks and investigated the effect of channel length and NW density. Our approach opens up the possibility for

fabricating high performance TFTs based on transparent and semiconducting ZnO NWs for applications requiring low-cost and low-temperature manufacturing, potentially on flexible substrates.

This work was funded by the Samsung Advanced Institute of Technology under the Advanced Nanomaterials for Electronics collaboration with the Cambridge University Engineering Department. Y. Zhang acknowledges the support from the EC via the DESGYN-IT and CANDICE projects.

- ¹X. Duan, Y. Huang, R. Agarwal, and C. M. Lieber, *Nature (London)* **421**, 241 (2003).
- ²Y. Cui and C. M. Lieber, *Science* **291**, 851 (2001).
- ³M. H. Huang, S. Mao, H. Feick, H. Yan, Y. Wu, H. Kind, E. Weber, R. Russo, and P. Yang, *Science* **292**, 1897 (2001).
- ⁴R. S. Friedman, M. C. McAlpine, D. S. Ricketts, D. Ham, and C. M. Lieber, *Nature (London)* **434**, 1085 (2005).
- ⁵Y. Qin, X. Wang, and Z. L. Wang, *Nature (London)* **451**, 809 (2008).
- ⁶B. Tian, X. Zheng, T. J. Kempa, Y. Fang, N. Yu, G. Yu, J. Huang, and C. M. Lieber, *Nature (London)* **449**, 885 (2007).
- ⁷X. Duan, C. Niu, V. Sahi, J. Chen, J. W. Parce, S. Empedocles, and J. L. Goldman, *Nature (London)* **425**, 274 (2003).
- ⁸M. C. McAlpine, H. Ahmad, D. Wang, and J. R. Heath, *Nature Mater.* **6**, 379 (2007).
- ⁹A. Javey, S. W. Nam, R. S. Friedman, H. Yan, and C. M. Lieber, *Nano Lett.* **7**, 773 (2007).
- ¹⁰J. H. Ahn, H. S. Kim, K. J. Lee, S. Jeon, S. J. Kang, Y. Sun, R. G. Nuzzo, and J. A. Rogers, *Science* **314**, 1754 (2006).
- ¹¹Z. Fan, J. C. Ho, Z. A. Jacobson, R. Yerushalmi, R. L. Alley, H. Razavi, and A. Javey, *Nano Lett.* **8**, 20 (2008).
- ¹²K. Heo, E. Cho, J. E. Yang, M. H. Kim, M. Lee, B. Y. Lee, S. G. Kwon, M. S. Lee, M. H. Jo, H. J. Choi, T. Hyeon, and S. Hong, *Nano Lett.* **8**, 4523 (2008).
- ¹³J. A. Baca, J. H. Ahn, Y. Sun, M. A. Meitl, E. Menard, H. S. Kim, W. M. Choi, D. H. Kim, Y. Huang, and J. A. Rogers, *Angew. Chem., Int. Ed.* **47**, 5524 (2008).
- ¹⁴J. S. Kang, C. Kocabas, H. S. Kim, Q. Cao, M. A. Meitl, D. Y. Khang, and J. A. Rogers, *Nano Lett.* **7**, 3343 (2007).
- ¹⁵J. S. Kang, C. Kocabas, T. Ozel, M. Shim, N. Pimparkar, M. A. Alam, S. V. Rotkin, and J. A. Rogers, *Nat. Nanotechnol.* **2**, 230 (2007).
- ¹⁶P. Yang, H. Yan, S. Mao, R. Russo, J. Johnson, R. Saykally, N. Morris, J. Pham, R. He, and H. J. Choi, *Adv. Funct. Mater.* **12**, 323 (2002).
- ¹⁷L. E. Greene, M. Law, D. H. Tan, M. Montano, J. Goldberger, G. Somorjai, and P. Yang, *Nano Lett.* **5**, 1231 (2005).
- ¹⁸S. Ju, A. Fachment, Y. Xuan, J. Liu, F. Ishikawa, P. Ye, C. Zhou, T. J. Marks, and D. B. Janes, *Nat. Nanotechnol.* **2**, 378 (2007).
- ¹⁹M. Law, L. E. Greene, J. C. Johnson, R. Saykally, and P. Yang, *Nature Mater.* **4**, 455 (2005).
- ²⁰B. Sun and H. Sirringhaus, *Nano Lett.* **5**, 2408 (2005).
- ²¹S. H. Ko, I. Park, M. N. Heng, M. S. Rogers, C. P. Grigoropoulos, and A. P. Pisano, *Appl. Phys. Lett.* **92**, 154102 (2008).
- ²²S. H. Dalal, D. L. Baptista, K. B. K. Teo, R. G. Lacerda, D. A. Jefferson, and W. I. Milne, *Nanotechnology* **17**, 4811 (2006).
- ²³G. E. Pike and C. H. Seager, *Phys. Rev. B* **10**, 1421 (1974).
- ²⁴W. K. Hong, J. I. Sohn, D. K. Hwang, S. S. Kwon, G. Jo, S. Song, S. M. Kim, H. J. Ko, S. J. Park, M. E. Welland, and T. Lee, *Nano Lett.* **8**, 950 (2008).
- ²⁵C. M. LeMieux, M. Roberts, S. Barman, Y. W. Jin, J. M. Kim, and Z. Bao, *Science* **321**, 101 (2008).
- ²⁶H. E. Unalan, Y. Yang, Y. Zhang, P. Hiralal, D. Kuo, S. Dalal, T. Butler, S. N. Cha, J. E. Jang, K. Chremmou, G. Lentaris, D. Wei, R. Rosentsveig, K. Suzuki, H. Matsumoto, M. Minagawa, Y. Hayashi, M. Chhowalla, A. Tanioka, W. I. Milne, R. Tenne, and G. A. J. Amarantunga, *IEEE Trans. Electron Devices* **55**, 2988 (2008).
- ²⁷E. Artukovic, M. Kaempgen, D. S. Hecht, S. Roth, and G. Gruner, *Nano Lett.* **5**, 757 (2005).
- ²⁸H. E. Unalan, G. Fanchini, A. Kanwal, A. Du Pasquier, and M. Chhowalla, *Nano Lett.* **6**, 677 (2006).