High speed vacuum deposition of organic TFTs in a roll-to-roll facility

Dr Hazel Assender

University of Oxford

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Research Centre

PRIFYSGOL BANGOR UNIVERSITY

Prof Martin Taylor
Eifion Patchett, Aled Williams

UNIVERSITY OF LEEDS

Prof Long Lin

MANCHESTER 1824

Prof Steve Yeates
Dr John Morrison

UNIVERSITY OF OXFORD

Dr Hazel Assender
Dr Gamal Abbas, Ziqian Ding

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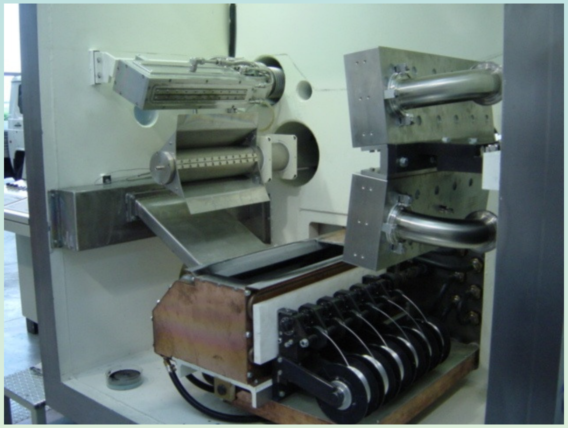
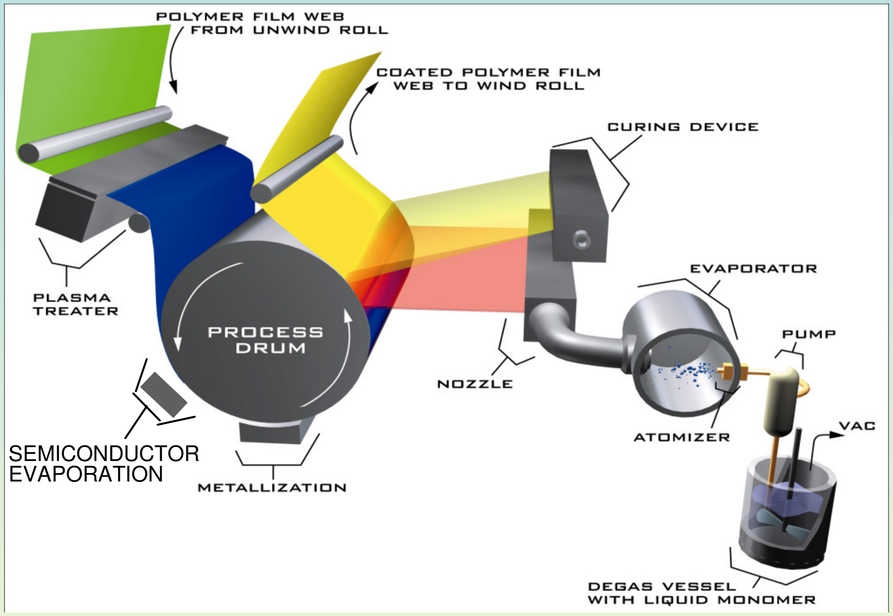
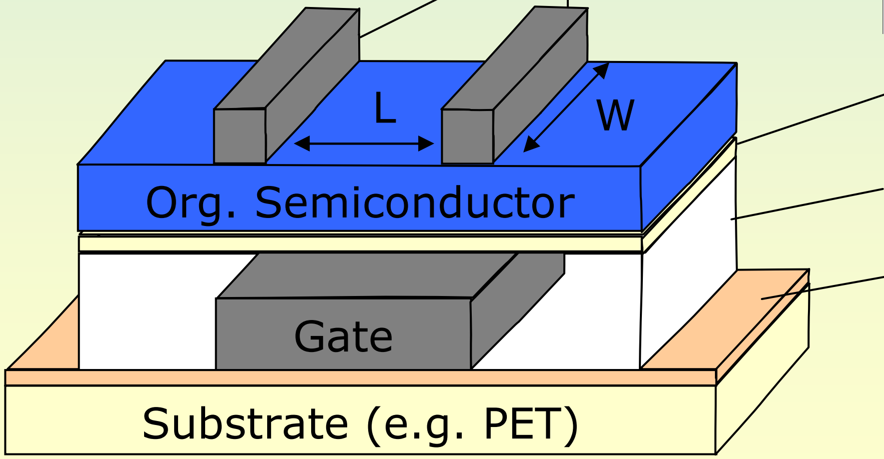
Manufacturing capability







Source and Drain (Metal)

Possible interlayer

Insulator (e.g. acrylic dielectric)

Possible surface modification

Roll-to-roll processing

Camvac

Oxford
Webspeed up to 5 ms^{-1}
Web width 350 mm

vacuum web coating

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Solvent vs. Vacuum deposition

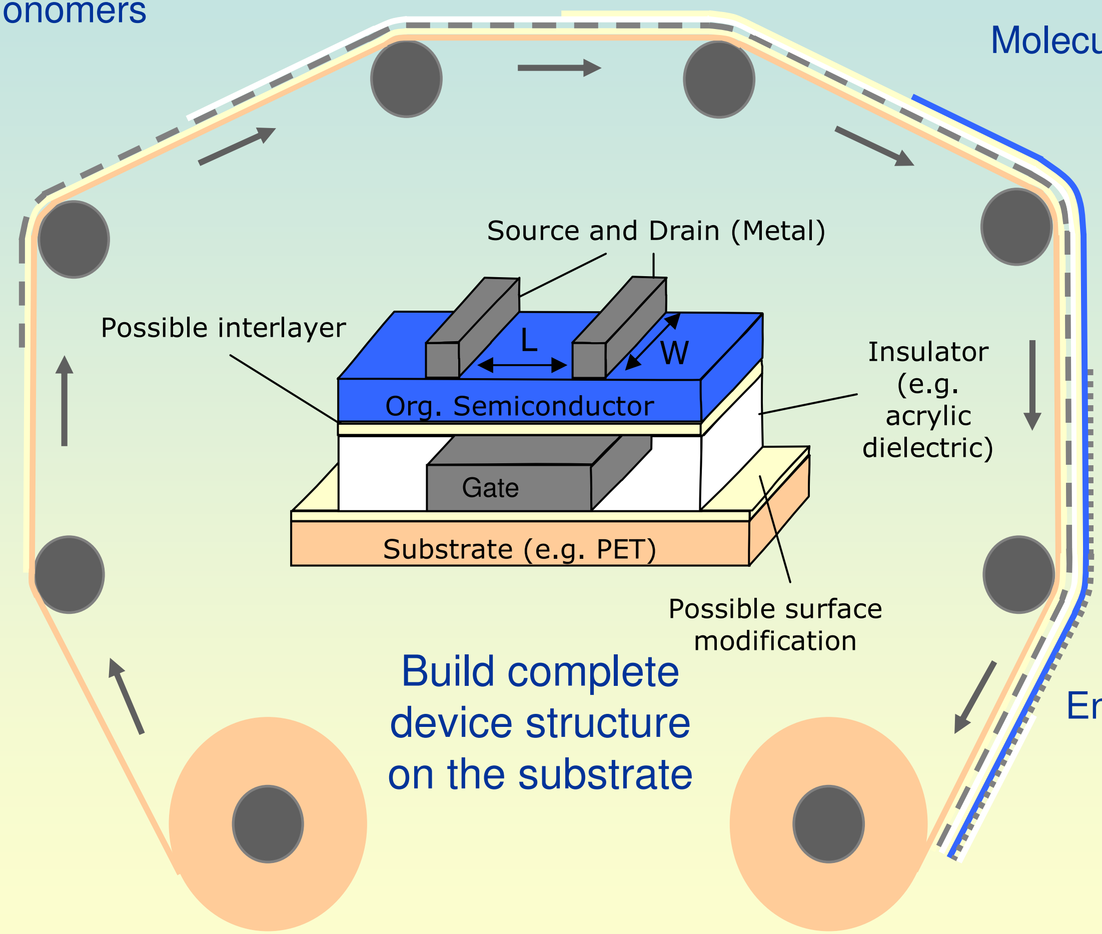
Solvent:

- No pumping
  - Outgassing
- Most development recently
  - Patterning methods relatively established

Vacuum:

- No solvent/low energy
- Rapid process (PVD)
- Multilayers easier
  - High performance metal and ceramic layers
  - No requirement for orthogonal solvents/wettability

Roll-to-roll deposition



Gate insulator layer:
Flash evaporated monomers
then cure

Perhaps surface modification
layer: Various options

Molecular semiconductor:
Evaporation

Gate:
pattern metallization

Source and Drain:
pattern metallization

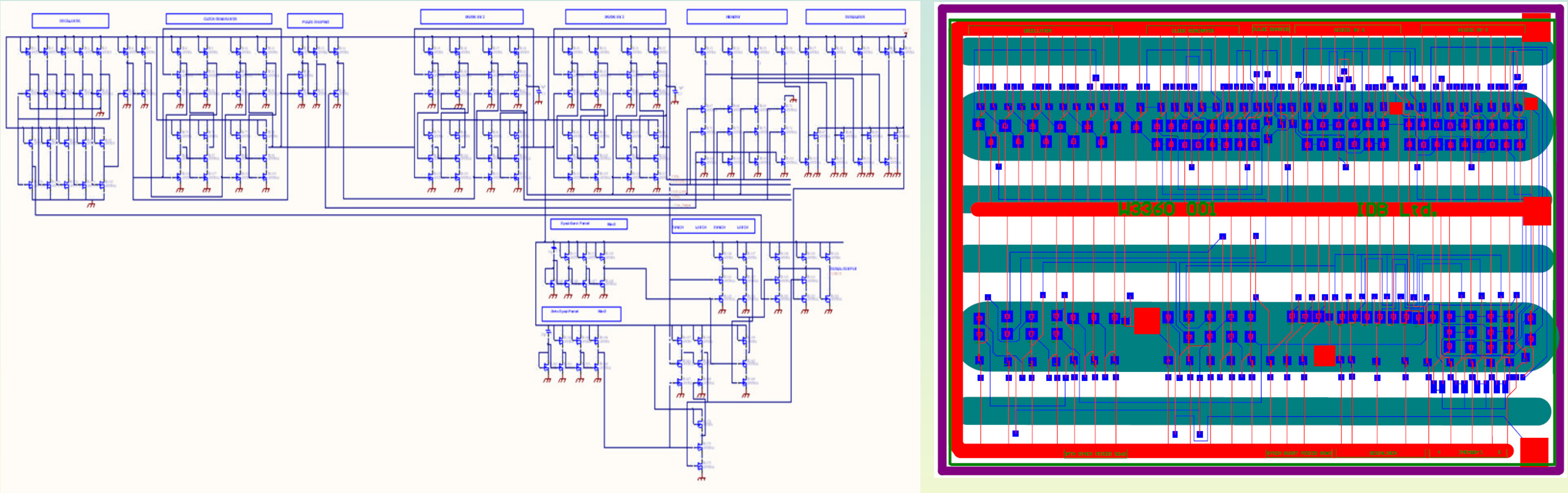
Polymer smoothing
layer:
Flash evaporated
monomers then cure

Build complete
device structure
on the substrate

Encapsulation layer/gas
barrier

Circuit design

- e.g. product tracking tag
- In collaboration with Prof. Martin Taylor, University of Bangor

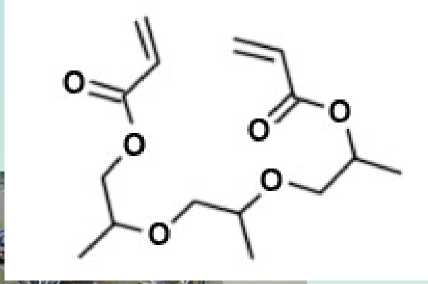


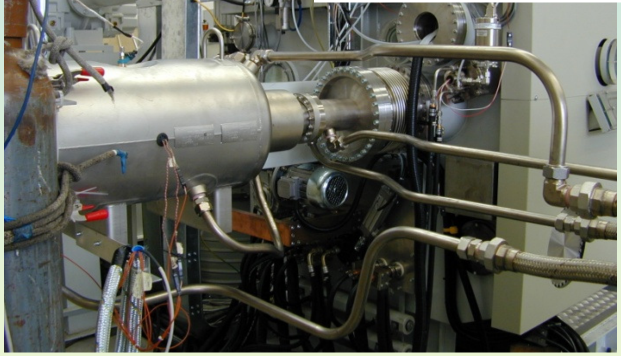
Model circuits based on measured device performances

- Design circuits around transistor performance and patterning capability
- Minimise number of transistors
- Circuit design defines manufacturing priorities

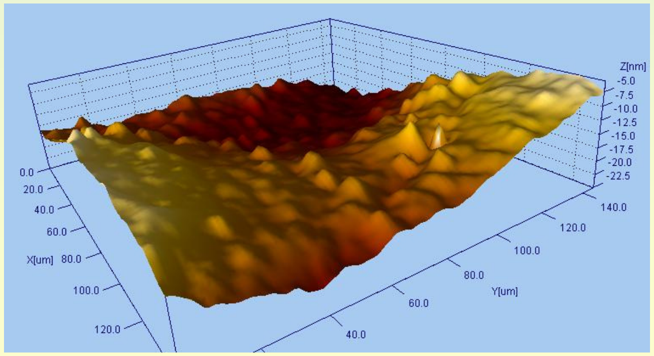
Polymer deposition

- Flash evaporation of a monomer
- Condenses as a liquid on substrate
- Cure (e.g. e-beam) to solid
    - High speed process
    - Already used for capacitor technology
    - Free of pin-holes over large area

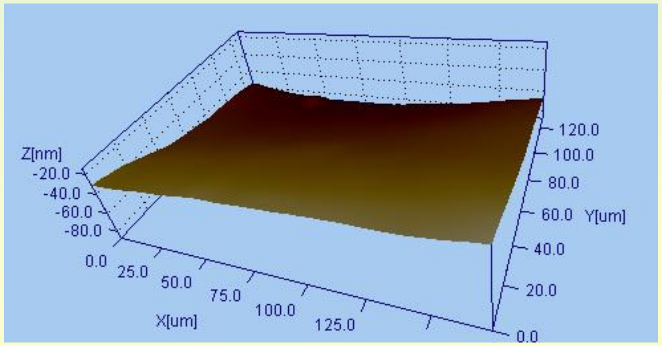




Optical Profilometry

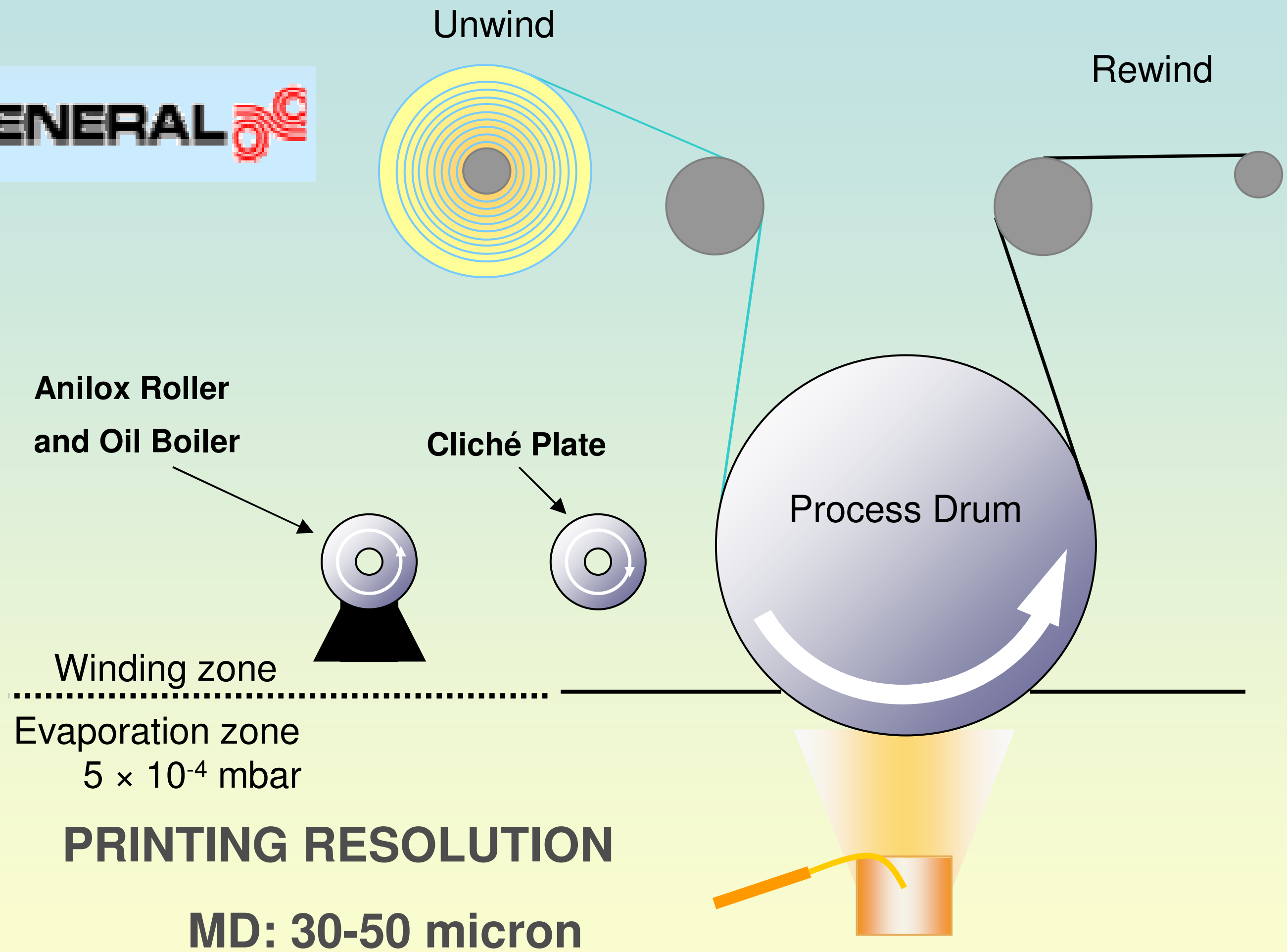


High quality PEN



Acrylic smoothing layer

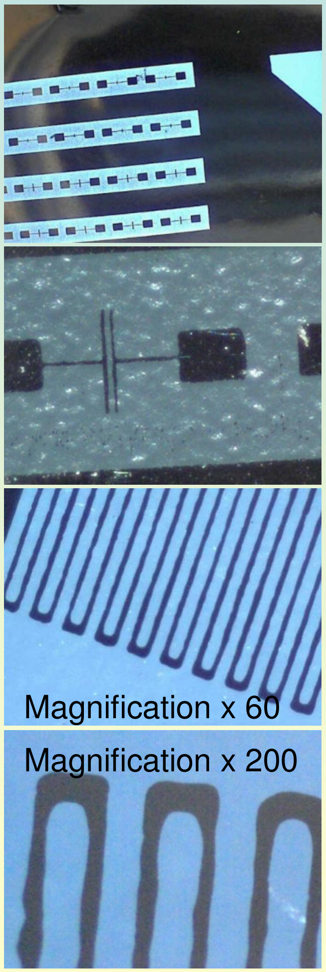
Materials: pattern metallisation



PRINTING RESOLUTION

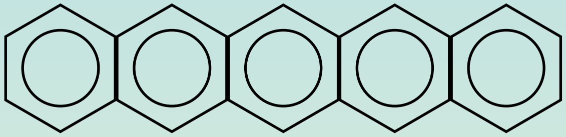
MD: 30-50 micron

TD: 30-50 micron



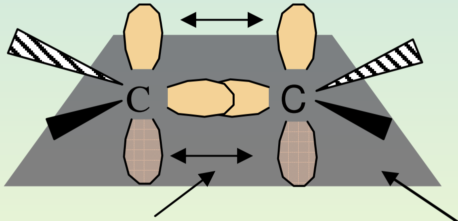
Source/Drain Electrodes

Getting the manufacture right: pentacene deposition



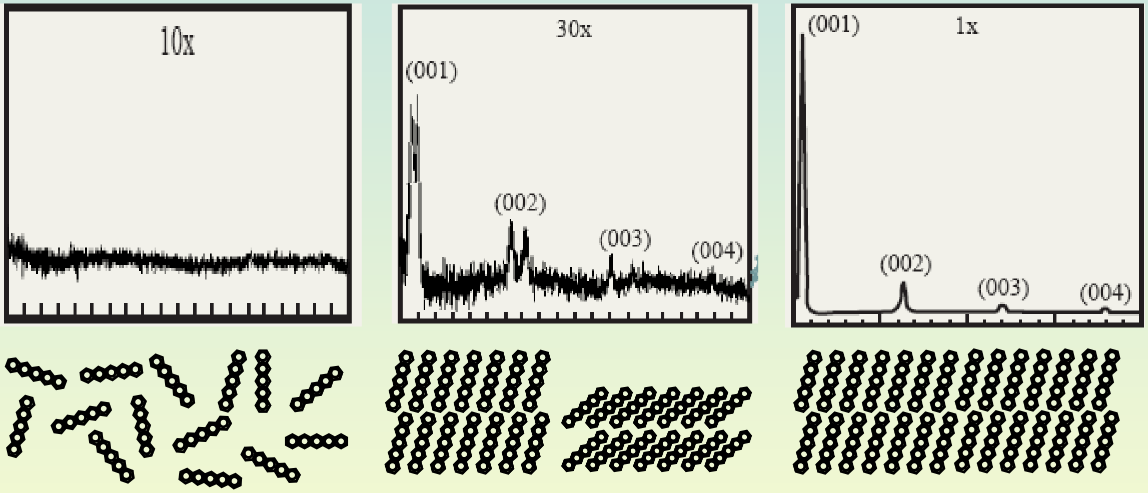
Self-assembling molecules

π -orbital overlap gives good carrier mobility.



p_z orbital overlap:
π bond

plane of sp^2
bonding (rings)



Mobility
~10^{-8} $cm^2V^{-1}s^{-1}$

Mobility
~10^{-6} $cm^2V^{-1}s^{-1}$

Mobility
~10^{0} $cm^2V^{-1}s^{-1}$

- Ordered organic material has higher charge transport mobility

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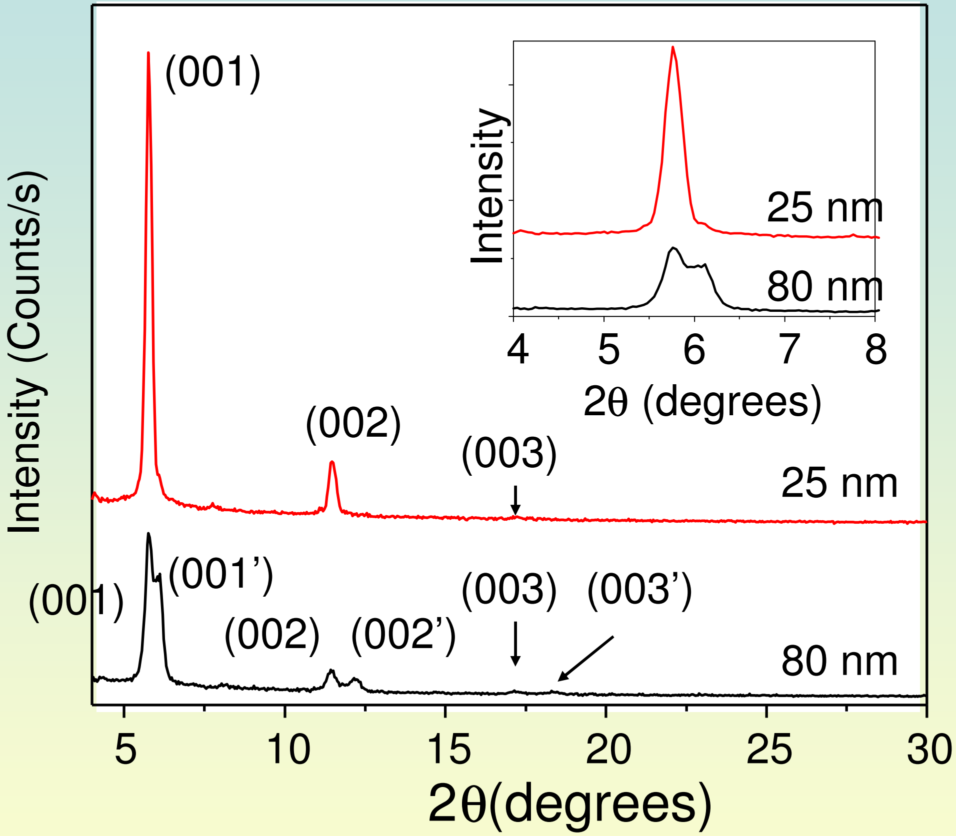
Pentacene Phases

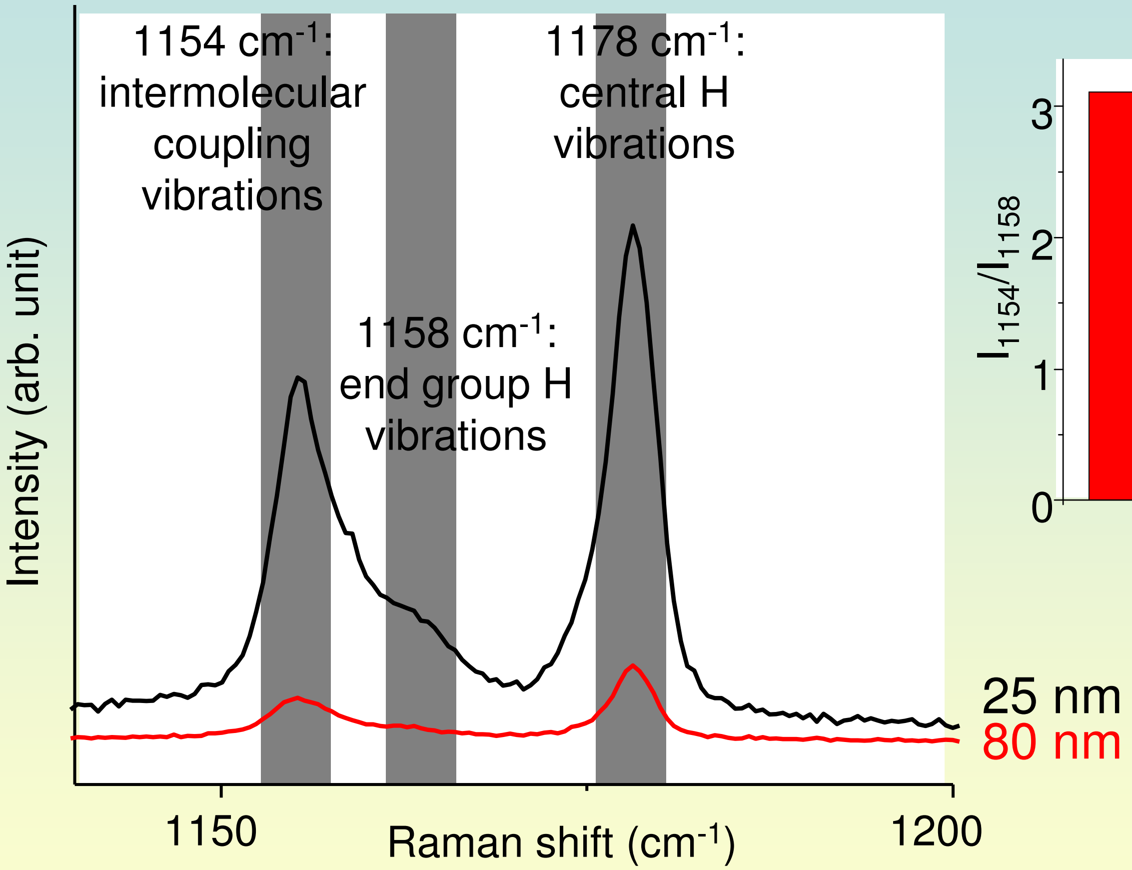


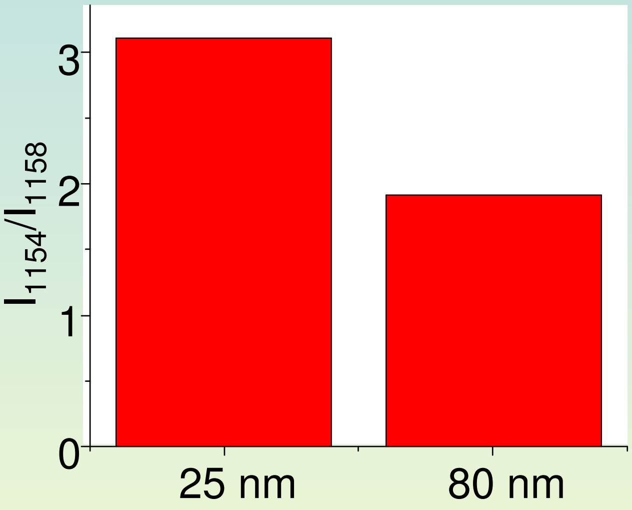
25 nm-thick pentacene on SiO_2
- one crystalline phase
- lattice spacing of 15.4 Å

80 nm-thick pentacene on SiO_2
- two crystalline phases
- lattice spacings 15.4 Å & 14.5 Å

- The 'thin film' phase is believed to be responsible for a high mobility in pentacene thin-films FETs

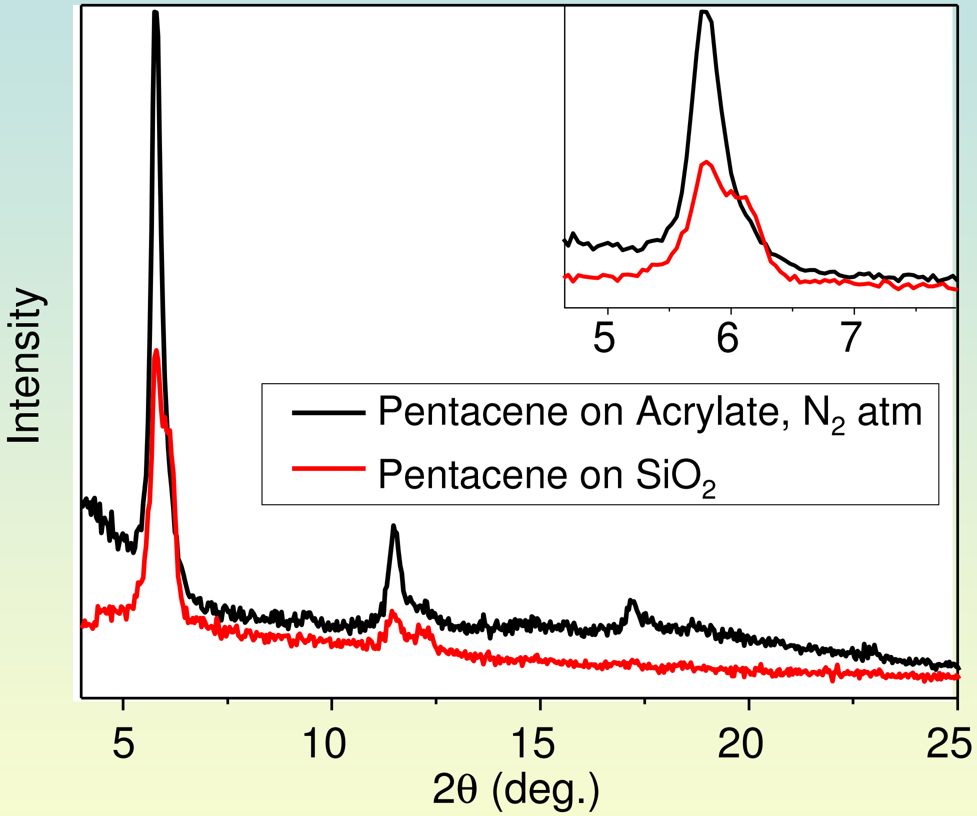
Microfocal Raman Spectroscopy





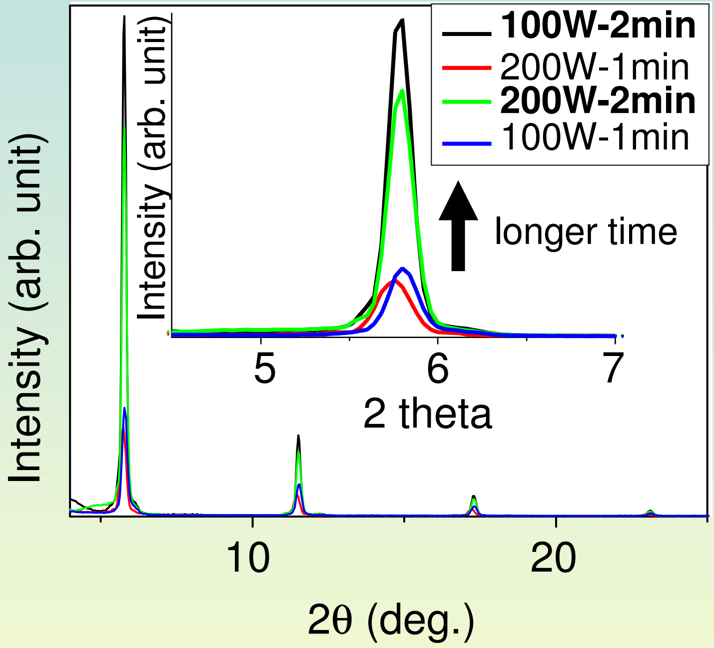
- The optimal π-orbital overlap was obtained in the 25-nm pentacene film.

Deposition onto Acrylate or SiOx



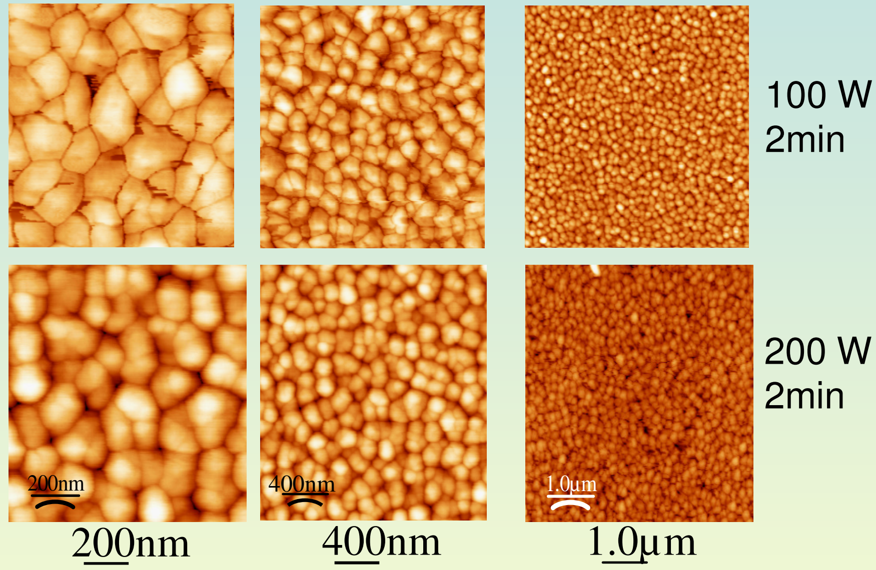
- Pentacene film (90nm-thick) grown on acrylate (1.5 µm-thick) is more single phase compared with that grown onto SiO_2 (300 nm-thick).

Oxygen Plasma Treatment



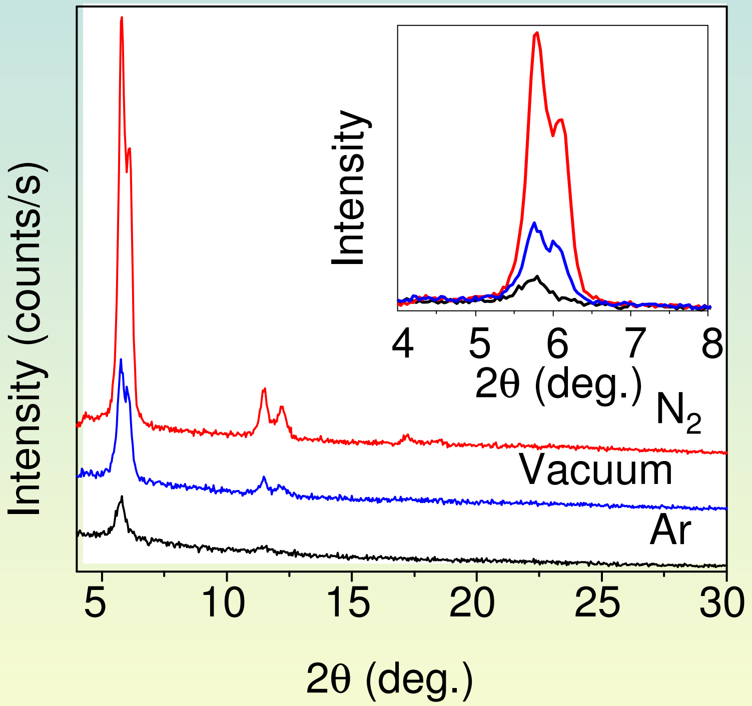
Oxygen-plasma treatment showed a noticeable effect on the diffraction intensities of pentacene films, grown on Si, with longer treatment time.

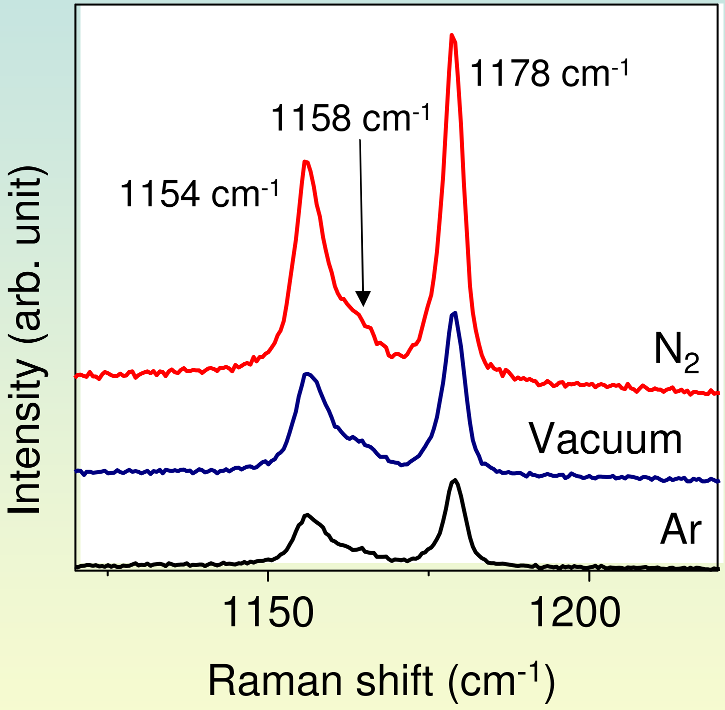
AFM micrographs



larger grain size associated with higher mobility

Effect of Background Gases



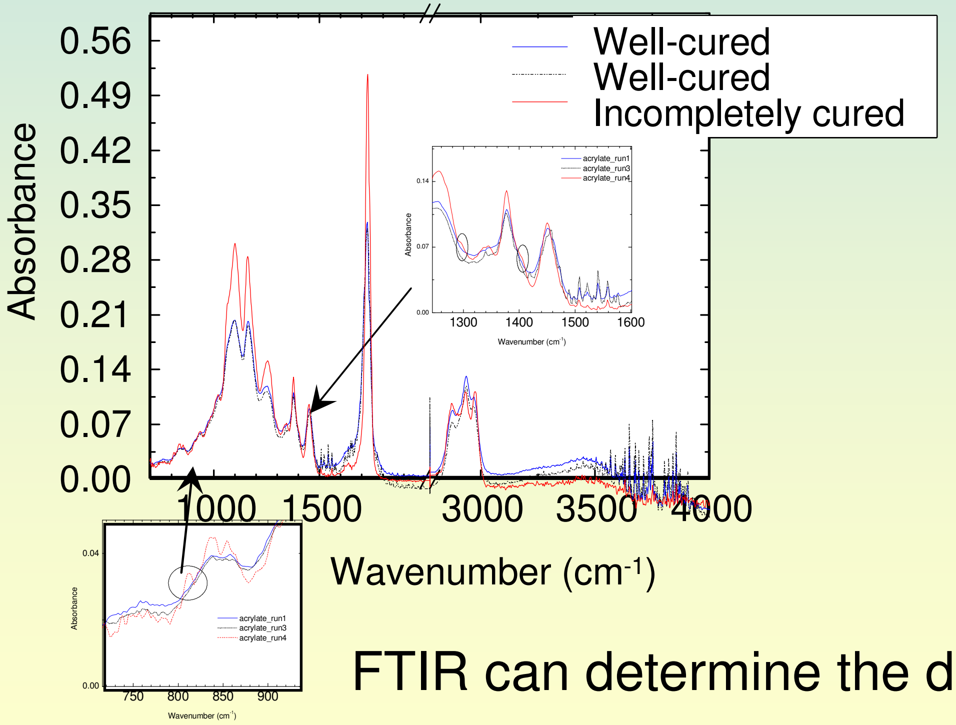


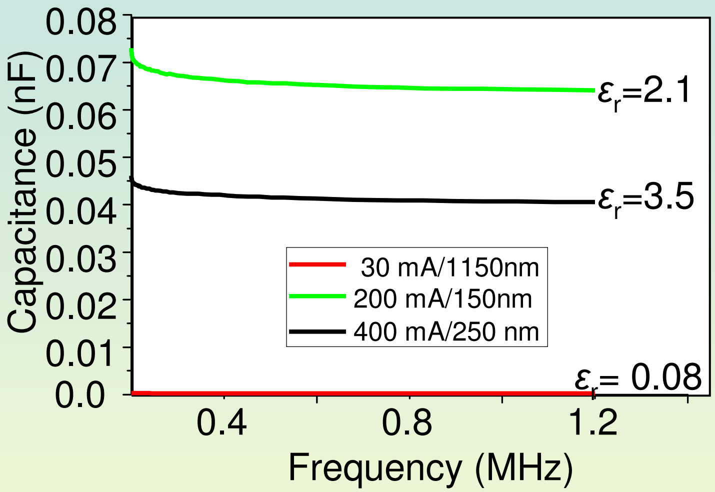
- Pentacene grown in N_2 ambience best crystalline material.

Getting the manufacture right: insulator layer

Smooth, pin-hole free layer

High degree of cure



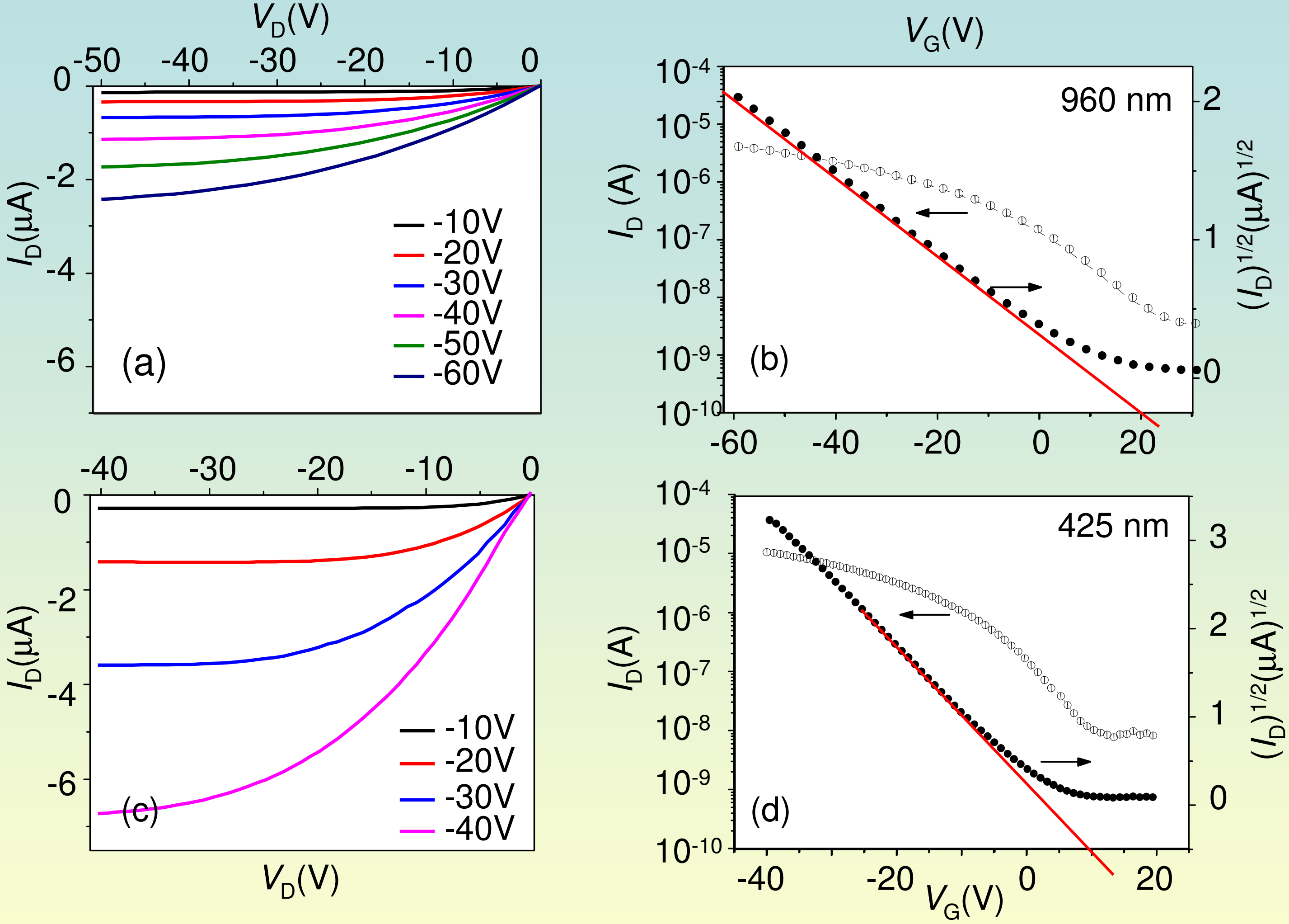


Impedance spectroscopy: Low loss

Can measure dielectric coefficient

FTIR can determine the degree of cure

Insulator thickness

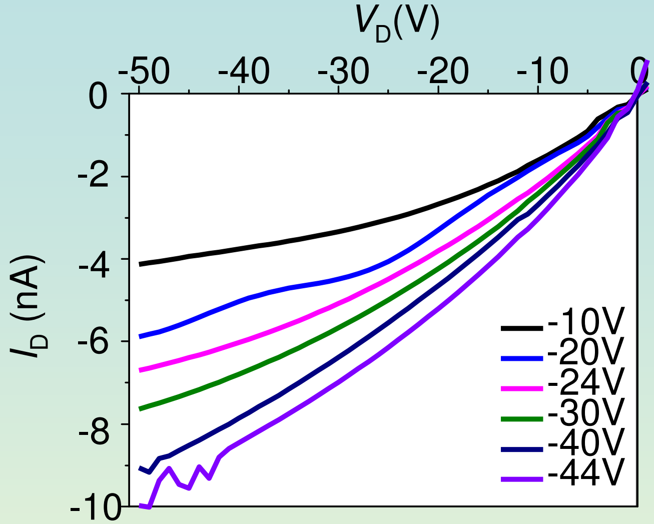


μ= 0.03 cm^2/V.sec
V_{th}=~20V
I_{on}/I_{off}= 1.18x10^3

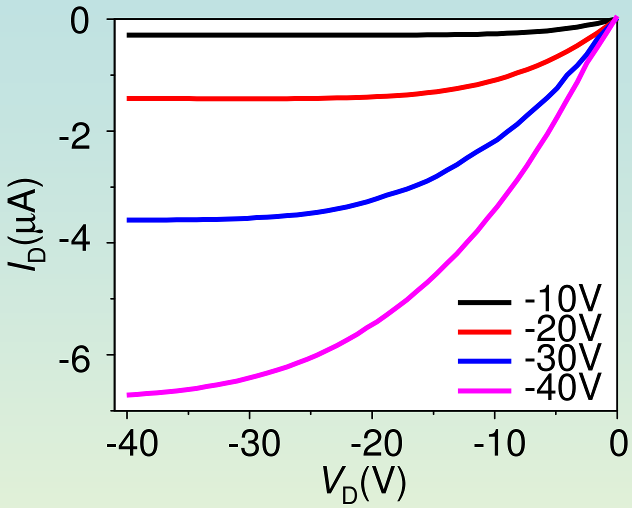
μ=~ 0.1 cm^2/V.sec
V_{th}=~10V
I_{on}/I_{off}= 1.30x10^3

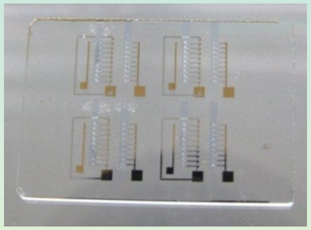
Comparison of I-V and output characteristics of bottom gate pentacene TFT on (a, b) 960 nm and (c, d) 425 nm thick TRPGDA polymeric dielectric with a 250μm channel length and an aspect ratio of 16.

Curing the acrylic

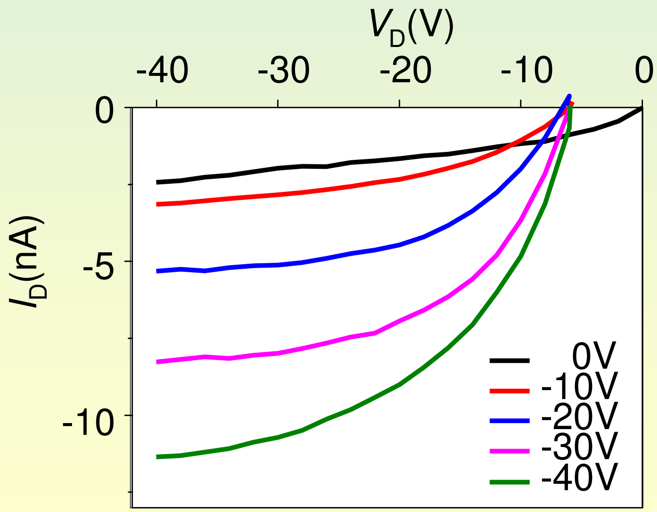


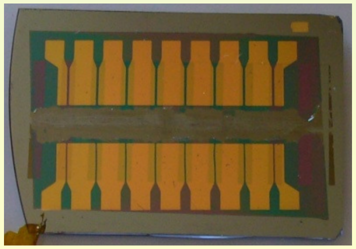
Thermal anneal

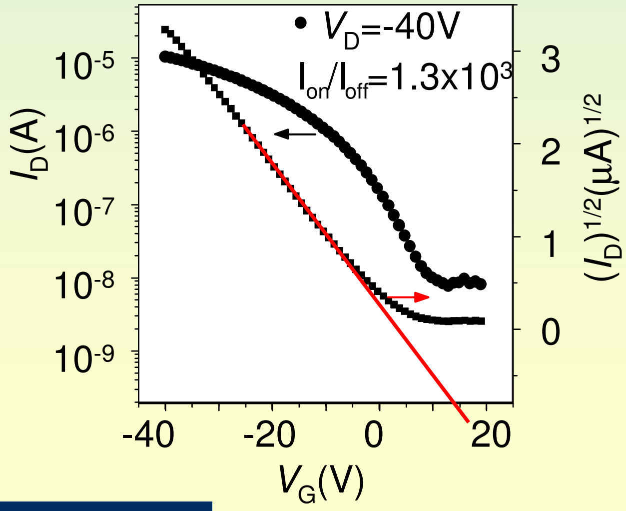




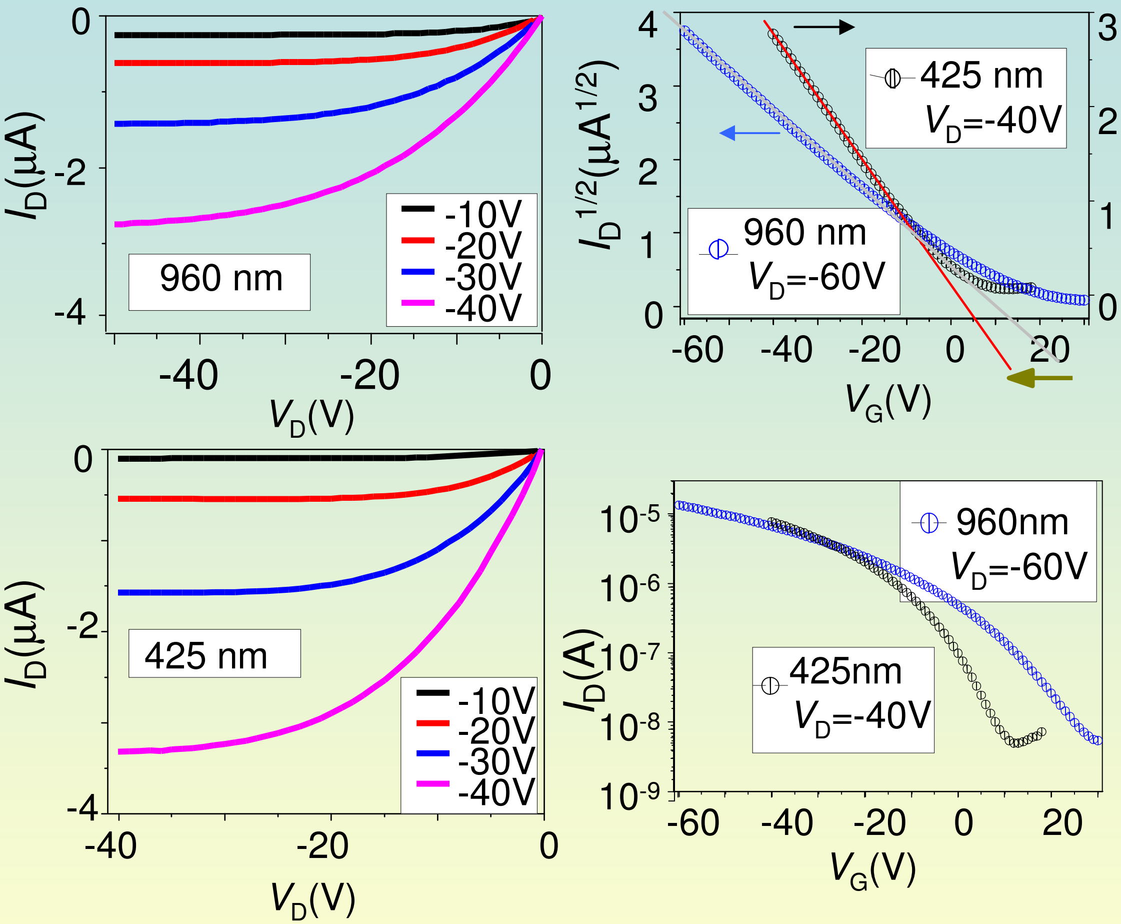
Increase cure current







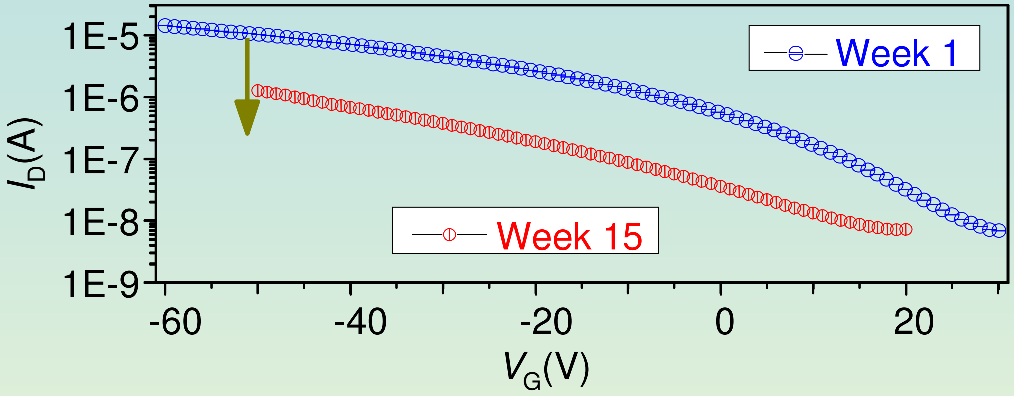
Plasma curing



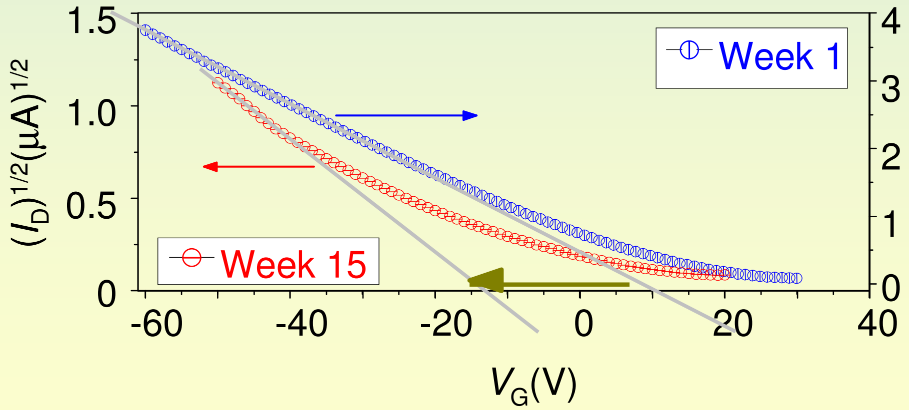
	960 nm	425 nm
I_{on}/I_{off}	2.0x10^3	1.5x10^3
V_{th} (V)	13	5
μ (cm^2/Vs)	0.10	0.06

I-V and output characteristics of bottom gate pentacene TFT on plasma cured TRPGDA dielectric of thickness 960nm and 425nm with a 250µm channel length and an aspect ratio of 16. No interfacial modification.

Shelf-life stability of as-deposited FETs



- Plasma cured
- No encapsulation



Week	1	15
I_{on}/I_{off}	$2.0\text{x}10^3$	$1.8\text{x}10^2$
V_{th} (V)	10	-13
μ (cm^2/Vs)	0.10	0.07

Summary

- Can make organic electronics in a R2R environment
- Vacuum technology uses solventless, high-speed processes
- Build complete devices from multilayers